

CLC420

APPLICATIONS:

- active filters/integrators
- differential amplifiers
- pin diode receivers
- log amplifiers
- D/A converters
- photo multiplier amplifiers

The CLC420 is an operational amplifier designed for applications requiring matched inputs, integration or transimpedance amplification. Utilizing voltage feedback architecture, the CLC420 offers a 300MHz bandwidth, a 1100V/ μ s slew rate and a 4mA supply current (power consumption of 40mW, ± 5 V supplies). Additional benefits of the CLC420B are a 0.5mV input offset voltage and a 4 μ V/ $^{\circ}$ C temperature coefficient.

Applications such as differential amplifiers will benefit from 70dB common mode rejection ratio and an input offset current of 0.2 μ A. With its unity-gain stability, 2pA/ $\sqrt{\text{Hz}}$ current noise and 3 μ A of input bias current, the CLC420 is designed to meet the needs of filter applications and log amplifiers. The low input offset current and current noise, combined with a settling time of 18ns to 0.01% make the CLC420 ideal for D/A converters, pin diode receivers and photo multipliers amplifiers. All applications will find 70dB power supply rejection ratio attractive.

The CLC420 is available in several versions to meet a variety of requirements.

CLC420AJP/BJP	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8-pin plastic DIP
CLC420AJE/BJE	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8-pin plastic SOIC
CLC420AID/BID	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8-pin side-brazed DIP
CLC420A8D/B8D	-55 $^{\circ}$ C to +125 $^{\circ}$ C	8-pin side-brazed DIP, MIL-STD-883, Level B dice
CLC420ALC	-55 $^{\circ}$ C to +125 $^{\circ}$ C	dice qualified to Method 5008, MIL-STD-883, Level B
CLC420AMC	-55 $^{\circ}$ C to +125 $^{\circ}$ C	

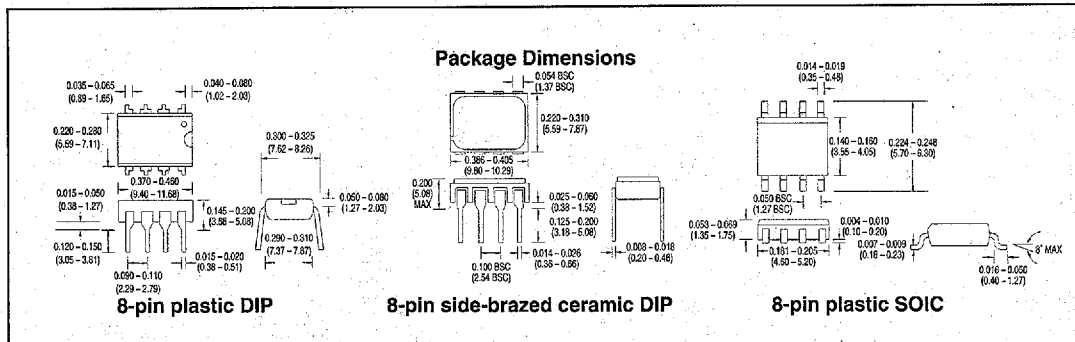
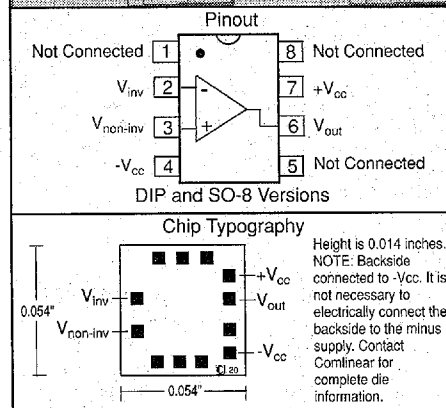
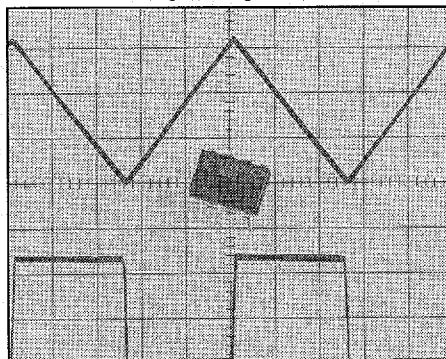
Contact factory for other packages. DESC SMD number, 5962-91758.

FEATURES (typical):

- 300MHz small signal bandwidth
- 1100 V/ μ s slew rate
- unity-gain stability
- 0.01% settling in 18ns
- CLC420B: 0.5mV input offset voltage, 4 μ V/ $^{\circ}$ C
- 0.2 μ A input offset current
- 2pA/ $\sqrt{\text{Hz}}$ current noise
- recommended gain range ± 1 to ± 10

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Electrical Characteristics ($A_V=+1$, $V_{CC}=\pm 5.0V$, $R_L=100\Omega$, $R_f=0\Omega$, unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS				UNITS	SYMBOL
Ambient Temperature	CLC420A8/B8/AL/AM	+25°C	-55°C	+25°C	+125°C			
Ambient Temperature	CLC420AJ/BJ/AL/BI	+25°C	-40°C	+25°C	+85°C			
FREQUENCY DOMAIN RESPONSE								
-3dB bandwidth	$V_{OUT}<0.4V_{pp}$	300	>200	>200	>130		MHz	SSBW
	$V_{OUT}<5V_{pp}$	40	>20	>25	>20		MHz	LSBW
$f_{A_V=-1}$, $R_f=500\Omega$	$V_{OUT}<0.4V_{pp}$	100	>65	>65	>45		MHz	SSBWI
$A_V=-1$, $R_f=500\Omega$	$V_{OUT}<5V_{pp}$	60	>30	>35	>30		MHz	LSBWI
gain flatness	$V_{OUT}<0.4V_{pp}$							
peaking	0.1MHz to 100MHz	0	<1	<0.6	<0.6		dB	GFPL
peaking	>100MHz	0	<5	<3	<3		dB	GFPH
rolloff	0.1MHz to 100MHz	0.2	<1	<1	<2		dB	GFR
rolloff, $A_V=-1$, $R_f=500\Omega$	0.1MHz to 30MHz	0.2	<1.4	<1.4	<1.6		dB	GFRI
linear phase deviation	0.1MHz to 100MHz	0.9	<1.8	<1.8	<2.5		°	LPD
TIME DOMAIN RESPONSE								
rise and fall time	0.4V step	1.2	<2	<2	<3		ns	TRS
	5V step	14	<25	<20	<20		ns	TRL
rise and fall time, $A_V=-1$, $R_f=500\Omega$	0.4V step	3.5	<5.5	<5.5	<7.8		ns	TRSI
	5V step	6	<10	<9.5	<10		ns	TRLI
settling time to $\pm 0.1\%$	2V step	12	<18	<18	<18		ns	TSS
$\pm 0.01\%$	2V step	18	<25	<25	<25		ns	TSP
overshoot	0.4V step	8	<35	<25	<25		%	OS
slew rate	5V step	1100	>600	>750	>600		V/ μ s	SR
slew rate, $A_V=-1$, $R_f=500\Omega$	5V step	750	>430	>500	>430		V/ μ s	SRI
DISTORTION AND NOISE RESPONSE								
2 ND harmonic distortion	$2V_{pp}$, 20MHz	-50	<-40	<-40	<-40		dBc	HD2
3 RD harmonic distortion	$2V_{pp}$, 20MHz	-53	<-45	<-45	<-40		dBc	HD3
\dagger 2 ND harmonic distortion, $A_V=-1$, $2V_{pp}$, 20MHz, $R_f=500\Omega$		-51	<-40	<-40	<-40		dBc	HD2
\dagger 3 RD harmonic distortion, $A_V=-1$, $2V_{pp}$, 20MHz, $R_f=500\Omega$		-51	<-40	<-40	<-35		dBc	HD3
input referred noise								
voltage	1MHz to 200MHz	4.2	<5.3	<5.3	<6		nV/ \sqrt{Hz}	VN
current	1MHz to 200MHz	2	<2.9	<2.6	<2.3		pA/ \sqrt{Hz}	ICN
STATIC DC PERFORMANCE								
*input offset voltage (A version)		1	<3.2	<2	<3.5		mV	VIO
average temperature coefficient		8	<15	—	<15		$\mu V/^\circ C$	DVIO
*input offset voltage (B version)		0.5	<1.6	<0.8	<1.8		mV	VI0B
average temperature coefficient		4	<10	—	<10		$\mu V/^\circ C$	DVI0B
*input bias current		3	<20	<10	<10		μA	IB
average temperature coefficient		45	<120	—	<60		nA/ $^\circ C$	DIB
*input offset current		0.2	<2.6	<1	<2		μA	IIO
average temperature coefficient		2	<20	—	<10		nA/ $^\circ C$	DII0
*open loop gain		65	>52	>56	>56		dB	AOL
\dagger power supply rejection ratio		70	>55	>60	>60		dB	PSRR
*common mode rejection ratio		80	>60	>65	>65		dB	CMRR
*supply current	no load, quiescent	4	<5	<5	<5		mA	ICC
MISCELLANEOUS PERFORMANCE								
differential mode input	resistance	2	>0.5	>1	>1		M Ω	RIND
	capacitance	1	<2	<2	<2		pF	CIND
common mode input	resistance	1	>0.25	>0.5	>0.5		M Ω	RINC
	capacitance	1	<2	<2	<2		pF	CINC
output impedance	at DC	0.02	<0.3	<0.2	<0.2		Ω	RO
output voltage range	no load	± 3.6	± 2.8	± 3	± 3		V	VO
*output voltage range	$R_L=100\Omega$	± 2.9	± 2.5	± 2.5	± 2.5		V	VOL
common mode input range		± 3.2	± 2.5	± 2.8	± 2.8		V	CMIR
output current	(AJ/BJ/AL/BI/AM)	± 70	± 30	± 50	± 50		mA	IO
output current	(A8/B8)	± 70	± 30	± 35	± 35		mA	IO

Absolute Maximum Ratings

V_{CC}	$\pm 7V$
I_{out}	
(is short circuit protected to ground, maximum reliability maintained if I_{out} does not exceed 70mA, except A8D, B8D which should not exceed 35mA over the military temperature range)	
common mode input voltage	$\pm V_{CC}$
differential input voltage	10V
junction temperature	+175°
operating temperature range	
AJ/AJ/BI/BJ:	-40°C to +85°C
A8/B8/AL/AM:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

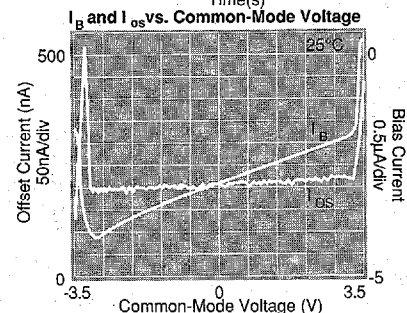
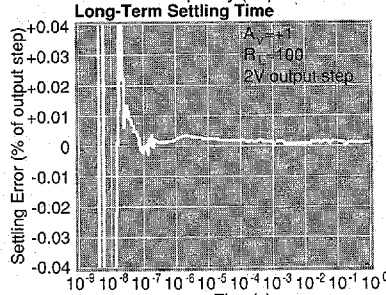
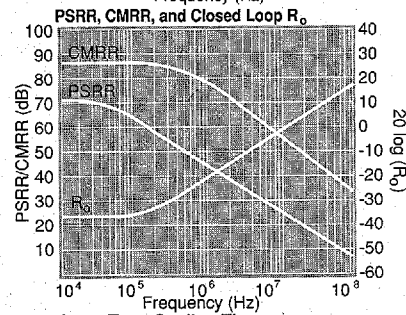
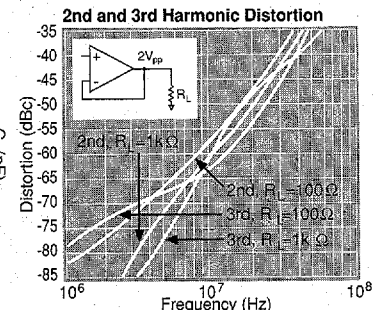
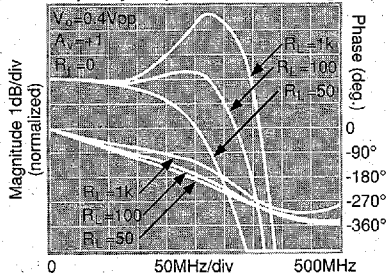
Miscellaneous Ratings

recommended gain range: ± 1 to ± 10

Notes:

- * AJ, AJ, BI, BJ 100% tested at +25°C, sample at +85°C.
- \dagger AJ, BJ Sample tested at +25°C.
- \dagger AI, BI 100% tested at +25°C.
- \dagger A8, B8 100% tested at +25°C, -55°C, +125°C.
- \dagger A8, B8 100% tested at +25°C, sample at -55°C, +125°C.
- * SMD Sample tested at +25°C, -55°C, +125°C.
- * AL, AM 100% water probed at +25°C to +25°C min/max specifications.

Frequency Response for Various R_L s



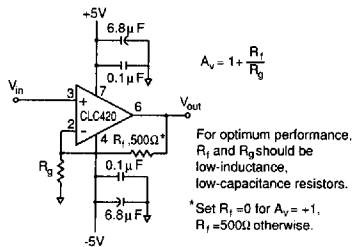


Figure 1: recommended non-inverting gain circuit

Description

The CLC420 is a high-speed, slew-booster, voltage-feedback amplifier with unity-gain stability. These features along with matched inputs, low input bias and noise currents, and excellent CMRR render the CLC420 very attractive for active filters, differential amplifiers, log amplifiers, and transimpedance amplifiers.

DC accuracy

Unlike current-feedback amplifiers, voltage-feedback amplifiers have matched inputs. This means that the non-inverting and inverting input bias currents are well matched and track over temperature, etc. As a result, by matching the resistance looking out of the two inputs, these errors can be reduced to a small offset current term.

Gain bandwidth product

Since the CLC420 is a voltage-feedback op-amp, closed-loop bandwidth is approximately equal to the gain-bandwidth product (typically 100MHz) divided by the noise gain of the circuit (for noise gains greater than 5). At lower noise gains, higher-order amplifier poles contribute to higher closed-loop bandwidth. At low gains use the frequency response performance plots given in the data sheet.

Another point to remember is that the closed-loop bandwidth is determined by the noise gain, not the signal gain of the circuit. Noise gain is the reciprocal of the attenuation in the feedback network enclosing the op amp. For example, a CLC420 setup as a non-inverting amplifier with a closed-loop gain of +1 (a noise gain of 1) has a 300MHz bandwidth. When used as an inverting amplifier with a gain of -1 (a noise gain of 2), the bandwidth is less, typically only 100MHz.

Full-power bandwidth, and slew-rate

The CLC420 combines exceptional full-power bandwidths (40MHz, $V_{O}=5V_{pp}$, $A_v=+1$) and slew rates (1100V/ μs , $A_v=+1$) with low (40mW) power consumption. These attractive results are achieved by using slew-boosting circuitry to keep the slew rates high while consuming very little power.

In non-slew boosted amplifiers, full-power bandwidth can be easily determined from slew-rate measurements, but in slew-boosted amplifiers, such as the CLC420, you can't. For this reason we provide data for both.

Slew rate is also different for inverting and non-inverting configurations. This occurs because common-mode signal voltages are present in non-inverting circuits but absent in inverting circuits. Once again data is provided for both.

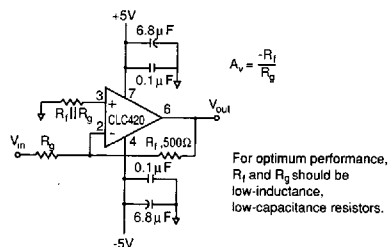


Figure 2: recommended inverting gain circuit

Transimpedance amplifier circuits

Low inverting, input current noise (2pA/ \sqrt{Hz}) makes the CLC420 ideal for high-sensitivity transimpedance amplifier circuits for applications such as pin-diode optical receivers, and detectors in receiver IFs. However, feedback resistors 4k Ω or greater are required if feedback resistor noise current is going to be less than the input current noise contribution of the op-amp.

With feedback resistors this large, shunt capacitance on the inverting input of the op-amp (from the pin-diode, etc.) will unacceptably degrade phase margin causing frequency response peaking or oscillations. A small-valued capacitor shunting the feedback resistor solves this problem (Note: This approach does not work for a current-feedback op-amp configured for transimpedance applications). To determine the value of this capacitor, refer to the "Transimpedance BW vs. R_f and C_f " plot.

For example, let's assume an optical transimpedance receiver is being developed. Total capacitance from the inverting input to ground, including the photodiode and strays is 5pF. A 5k Ω feedback resistor value has been determined to provide best dynamic range based on the responsivity of the photodiode and the range of incident optical powers, etc. From the "Transimpedance BW vs. R_f and C_f " plot, using $C_f = 5pF$ it is determined from the two curves labeled $C_f = 5pF$, that $C_f = 1.5pF$ provides optimal compensation (no more than 0.5dB frequency response peaking) and a -3dB bandwidth of approximately 27MHz.

Printed circuit layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the output and inverting input: Node connections should be small with minimal coupling to the ground plane.

Parasitic or load capacitance directly on the output (pin 6) will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect. The graphs on the preceding page, "Settling Time vs. C_L ", illustrate the required resistor value and resulting performance vs. capacitance.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC420 are available.