

MNDM54LS174-X REV 1B0

 Original Creation Date: 04/15/98
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HEX D FLIP-FLOP with MASTER RESET
General Description

The 'LS174 is a high-speed hex D flip-flop. The device is primarily used as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Industry Part Number

54LS174

NS Part Numbers

 DM54LS174E/883
 DM54LS174J/883
 DM54LS174W/883

Prime Die

L174

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55C to +175C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage	-0.5V to +10.0V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Free Air Ambient Temperature Military	-55 C to +125 C
Supply Voltage Military	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=4.5V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=10.0V, VINH=4.5V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.4V, VINH=4.5V	1, 3	INPUTS	-0.03	-0.4	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIL=0.7V, IOL=4.0mA, VINH=4.5V, VINL=0.0V	1, 3	OUTPUTS		0.4	V	1, 2, 3
VOH	Output HIGH Voltage	VCC= 4.5V, VIH=2.0V, IOH=-0.4mA, VINL=0.0V	1, 3	OUTPUTS	2.5		V	1, 2, 3
IOS	Short Circuit Current	VCC=5.5V, VINH=4.5V, VOUT=0.0V	1, 3	OUTPUTS	-20	-100	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=4.5V	1, 3	INPUTS		-1.5	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINH=4.5V	1, 3	VCC		26	mA	1, 2, 3

AC PARAMETERS - 15pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=15pF, RL=2k ohms Temp range: +25C

tpLH	Propagation Delay	VCC=5.0V	5	CP to Qn		25	ns	9
tpHL	Propagation Delay	VCC=5.0V	5	CP to Qn		22	ns	9
tpHL 2	Propagation Delay	VCC=5.0V	5	MR to Qn		35	ns	9
ts(H/L)	Setup Time	VCC=5.0V	5	Dn to CP	10		ns	9
th(H/L)	Hold Time	VCC=5.0V	5	Dn to CP	5		ns	9
tREC	Recovery Time	VCC=5.0V	5	MR to CP	12		ns	9
tw(H)	Pulse Width	VCC=5.0V	5	CP	18		ns	9
tw(L)	Pulse Width	VCC=5.0V	5	MR	18		ns	9
fMAX	Maximum Clock Frequency	VCC=5.0V	5	CP	30		MHZ	9

Electrical Characteristics

AC PARAMETERS - 50pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: CL=50pF, RL=2k ohms Temp range: -55C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH	Propagation Delay	VCC=5.0V	2, 4	CP to Qn	2	37	ns	9
			2, 4	CP to Qn	2	47	ns	10, 11
tpHL	Propagation Delay	VCC=5.0V	2, 4	CP to Qn	2	40	ns	9
			2, 4	CP to Qn	2	52	ns	10, 11
tpHL 2	Propagation Delay	VCC=5.0V	2, 4	MR to Qn	2	42	ns	9
			2, 4	MR to Qn	2	52	ns	10, 11
Ts (H/L)	Set-up time	VCC=5.0V	2, 4	Dn to CP	20		ns	9, 10, 11
th (H/L)	Hold time	VCC=5.0V	2, 4	Dn to CP	5		ns	9, 10, 11
tREC	Recovery Time	VCC=5.0V	2, 4	MR to CP	20		ns	9, 10, 11
Tw (H)	Pulse width	VCC=5.0V	2, 4	CP	30		ns	9, 10, 11
Tw (L)	Pulse width	VCC=5.0V	2, 4	MR	35		ns	9, 10, 11
Fmax	Maximum clock frequency	VCC=5.0V	2, 4	CP	25		MHZ	9, 10, 11

Note 1: Screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.

Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.

Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, subgroup A9. Subgroups 10 & 11 are guaranteed, not tested.

Note 5: GUARANTEED, NOT TESTED. (Design characterization data)

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B0	M0002954	08/28/98	Linda Collins	New update::MNDM54LS174-X Rev. 1B0. Changed the MDS ID from MNDM54LS174X to MNDM54LS174-X.