HD74HC564,HD74HC574 ● Octal D-type Flip-Flops (with 3-state outputs)

These devices are positive edge triggered flip-flops. The difference between HD74HC564 and HD74HC574 is only that the former has inverting outputs and the latter has non-invertering outputs.

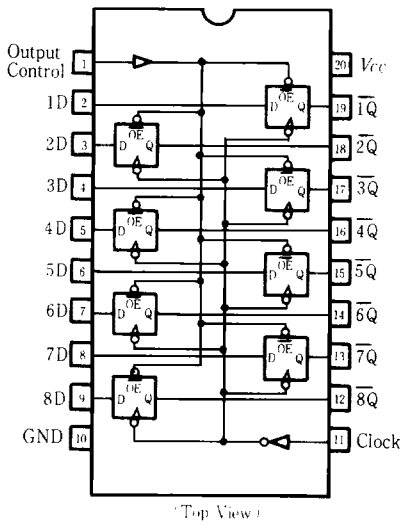
Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q or $\overline{Q}$ outputs on positive going transitions of the clock (CK) input. When a high logic level is applied to the output control (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

■ FEATURES

- High Speed Operation: t_{pd} (Clock to Output)=13ns typ. (C_L=50pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)=4μA max. (Ta=25°C)

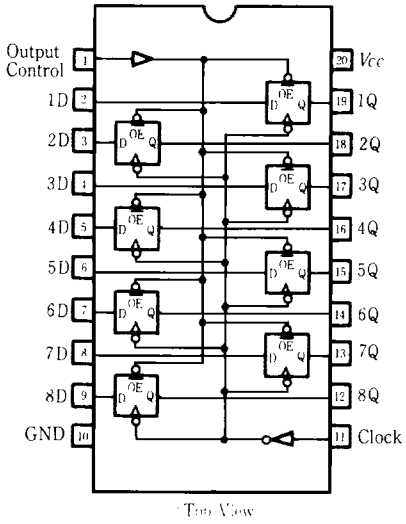
■ PIN ARRANGEMENT

● HD74HC564



(Top View)

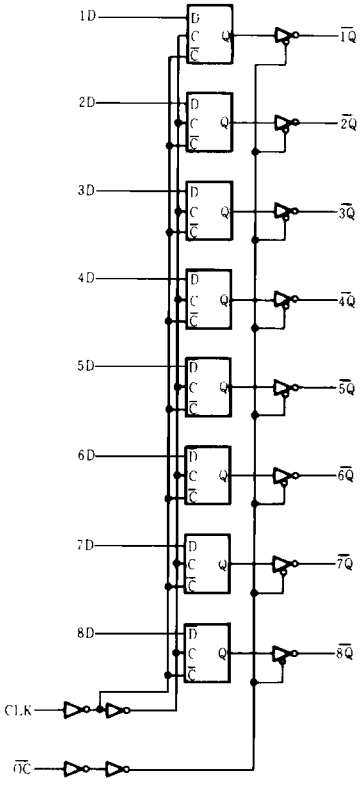
● HD74HC574



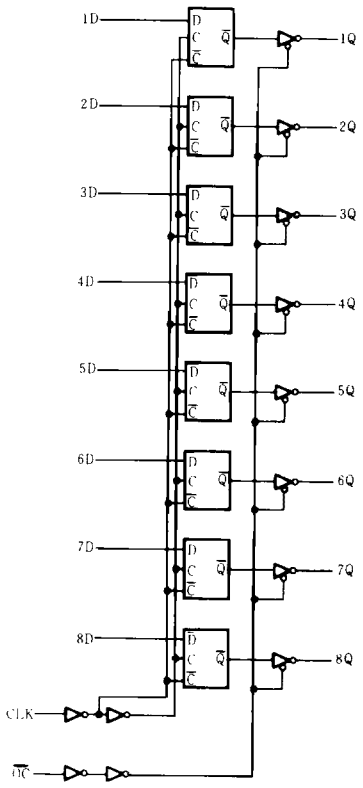
(Top View)

■ BLOCK DIAGRAM

● HD74HC564



● HD74HC574



■ FUNCTION TABLE

Output Control	Clock	Data	Output	
			HD74HC564	HD74HC574
L	↑	H	L	H
L	↑	L	H	L
L	L	×	$\bar{Q}_0$	Q_0
H	×	×	Z	Z

Notes) Q_0: level of Q before the indicated Steady-state input conditions were estadlished.
$\bar{Q}_0$: complement of Q_0 or level of $\bar{Q}$ before the indicated Steady-state input Conditions were established.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	−0.5～+7.0	V
Input Voltage	V_{IN}	−0.5～V_{CC}+0.5	V
Output Voltage	V_{OUT}	−0.5～V_{CC}+0.5	V
Output Current	I_{OUT}	±35	mA
DC Current Drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	−65～+150	°C

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40～+85°C min	Ta=−40～+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−6mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−7.8mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=6mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=7.8mA	—	—	0.26	—	0.33	
Off-state Output Current	I_{OZ}	6.0	V_{in}=V_{IH} or V_{IL}, V_{out}=V_{CC} or GND		—	—	±0.5	—	±5.0	μA
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	6	—	5	MHz
		4.5		—	—	30	—	24	
		6.0		—	—	35	—	28	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	Clock to Output	—	—	155	—	195	ns
		4.5		—	13	31	—	39	
		6.0		—	—	26	—	33	
Output Enable Time	t_{ZH} t_{ZL}	2.0		—	—	150	—	190	ns
		4.5		—	13	30	—	38	
		6.0		—	—	26	—	33	
Output Disable Time	t_{HZ} t_{LZ}	2.0		—	—	150	—	190	ns
		4.5		—	15	30	—	38	
		6.0		—	—	26	—	33	
Setup Time	t_{su}	2.0		—	—	100	—	125	ns
		4.5		—	1	20	—	25	
		6.0		—	—	17	—	21	
Hold Time	t_h	2.0		5	—	—	5	—	ns
		4.5		5	0	—	5	—	
		6.0		5	—	—	5	—	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	4	—	20	—	
		6.0		14	—	—	17	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	60	—	75	ns
		4.5		—	4	12	—	15	
		6.0		—	—	10	—	13	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF