TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518512AF/AFT is a 4,194,304-bit CMOS pseudo static random access memory (PSRAM) organized as 524,288 words by 8 bits. It feature a one-transistor dynamic memory cell using CMOS peripheral circuitry to provide large capacity, high speed and low power. It uses a single 5.0 V ± 10% power supply. An $\overline{OE}$/RFSH input selects either auto or self refresh operation. This device family also features SRAM-like write functions whereby data is written to the memory cell rising edge of R/W signal, for easy interfacing to microprocessors. The TC518512AF/AFT is molded in 32-pin 0.525-inch small-outline plastic packages (SOP), and thin small-outline plastic package (TSOP).

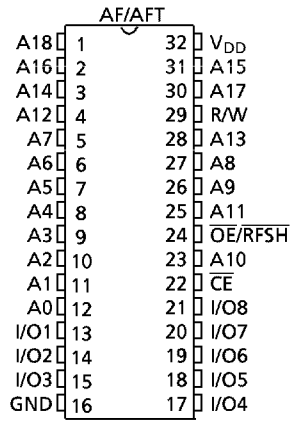
FEATURES

- Organized as 524,288 words by 8 bits (4,194,304 bits).

		TC518512A Family		
		-70	-80	-10
t_{CEA} $\overline{CE}$ Access Time		70 ns	80 ns	100 ns
t_{OEA} $\overline{OE}$ Access Time		30 ns	30 ns	40 ns
t_{RC} Cycle Time		115 ns	130 ns	160 ns
Power Dissipation		385 mW	330 mW	275 mW
Self Refresh Current	5.5 V	100 μA		
	3.6 V	50 μA		
	3.3 V	40 μA		

- Fast access time and low power dissipation.
- Single power supply voltage of 5 V ± 10%.
- Data retention power supply voltage of 2.7 to 5.5 V.
- Internal counter can be used for auto and self refresh operations.
- Internal timer can be used for self refresh operation.
- 2048 refresh cycles per 32 ms.
- All inputs and outputs are TTL compatible.
- Logic compatible with SRAM R/W pin.
- Packages:
  SOP32-P-525-1.27 (AF) (Weight: 1.10 g typ)
  TSOP II 32-P-400-1.27 (AFT) (Weight: 0.51 g typ)

PIN ASSIGNMENT(TOP VIEW)

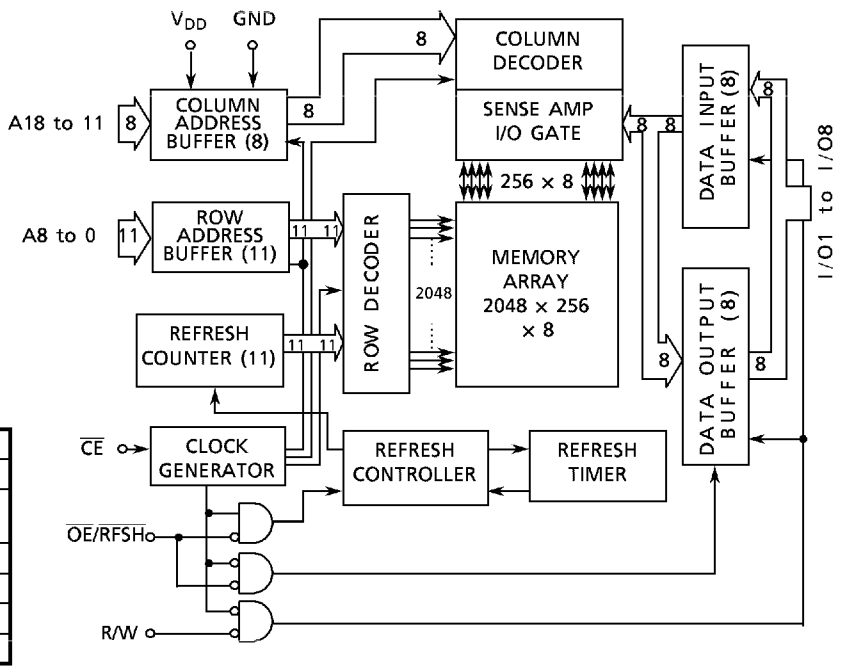


(Normal pinout)

PIN NAMES

A0 to A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$/RFSH	Output Enable Refresh Input
$\overline{CE}$	Chip Enable
I/O1 to I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



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TRUTH TABLE

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	R/W	A0 to A18	I/O1 to 8	CONDITION
L	L	×	××	OUT	Read
L	×	×	××	IN	Write
L	H	×	××	HZ	$\overline{CE}$ Only Refresh
H	L	×	×	HZ	Auto/Self Refresh
H	H	×	×	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5 V to V_{IH} min)
L ··· Low Level Input (V_{IN} = V_{IL} max to − 1.0 V)
× ··· Don't care.
×× ··· At $\overline{CE}$ falling edge, all address are "IN", and at the other condition, the address are "×"
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT	NOTE
V_{IN}	Input Voltage	− 1.0 to 7.0	V	1
V_{OUT}	Output Voltage	− 1.0 to 7.0	V	
V_{DD}	Power Supply Voltage	− 1.0 to 7.0	V	
T_{OPR}	Operating Temperature	0 to 70	°C	
T_{STG}	Storage Temperature	− 55 to 150	°C	
T_{SOLDER}	Soldering Temperature (10 s)	260	°C	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	− 1.0	−	0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	NOTE
I_{DDO}	Operating Current (Average Power Supply) $\overline{CE}$, Address Cycling: t_{RC} = t_{RC} min	70 ns version	–	50	70	mA	3, 4
		80 ns version	–	45	60		
		100 ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{OE/RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} – 0.2 V, $\overline{OE/RFSH}$ = V_{DD} – 0.2 V		–	–	100	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE}$ = V_{IH}, $\overline{OE/RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE}$ = V_{DD} – 0.2 V, $\overline{OE/RFSH}$ = 0.2 V		–	–	100	μA	
I_{DDF3}	Auto Refresh Current (Average) ($\overline{OE/RFSH}$ Cycling: t_{FC} = t_{FC} min)	70 ns version	–	–	70	mA	3
		80 ns version	–	–	60		
		100 ns version	–	–	50		
I_{DDF4}	$\overline{CE}$ Only Refresh Current (Average) ($\overline{CE}$, Address Cycling: t_{RC} = t_{RC} min)	70 ns version	–	–	70	mA	3
		80 ns version	–	–	60		
		100 ns version	–	–	50		
$I_{I(L)}$	Input Leakage Current 0 V ≦ V_{IN} ≦ V_{DD}, All Other Inputs Not Under Test = 0 V		– 10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE/RFSH}$ = V_{IH} or R/W = V_{IL}), 0 V ≦ V_{OUT} ≦ V_{DD}		– 10	–	10	μA	
V_{OH}	Output High Level I_{OH} = – 1.0 mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 2.1 mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 to A18)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE/RFSH}$, R/W)	–	7	pF
C_{I0}	Input/Output Capacitance	–	7	pF

Note: This parameter is periodically sampled and is not 100% tested.

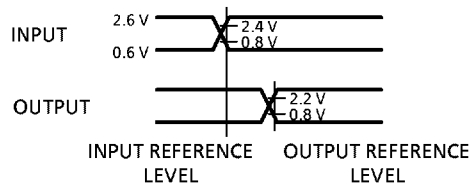
AC CHARACTERISTICS (V_{DD} = 5 V ± 10%, Ta = 0° to 70°C) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	–	130	–	160	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	180	–	220	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	35	–	40	–	50	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	70	–	80	–	100	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	30	–	30	–	40	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	20	–	20	–	20	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OSC}	$\overline{OE}$ Setup Time Referenced to $\overline{CE}$	10	–	10	–	10	–	ns	9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–	ns	9
t_{RCS}	Read Command Setup Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	25	–	25	–	30	–	ns	
t_{WCH}	Write Command Hold Time	40	–	40	–	50	–	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	25	–	25	–	30	–	ns	
t_{DSW}	Data Setup Time from R/W	20	–	20	–	25	–	ns	10
t_{DSC}	Data Setup Time from $\overline{CE}$	20	–	20	–	25	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	0	–	ns	10
t_{ASC}	Address Setup Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	15	–	20	–	25	–	ns	11
t_{FC}	Auto Refresh Cycle Time	130	–	130	–	160	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	–	40	–	50	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	160	–	190	–	ns	12
t_{REF}	Refresh Period (2048 cycles, A0 to A10)	–	32	–	32	–	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

1) Stresses greater than those listed under " Absolute Maximum Ratings " may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO}, I_{DDF3} and I_{DDF4} depend on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100 μs with $\overline{CE}$ High is required after power-up before proper device operation is achieved.
6) AC measurements assume t_T = 5 ns.
7) Timing reference levels

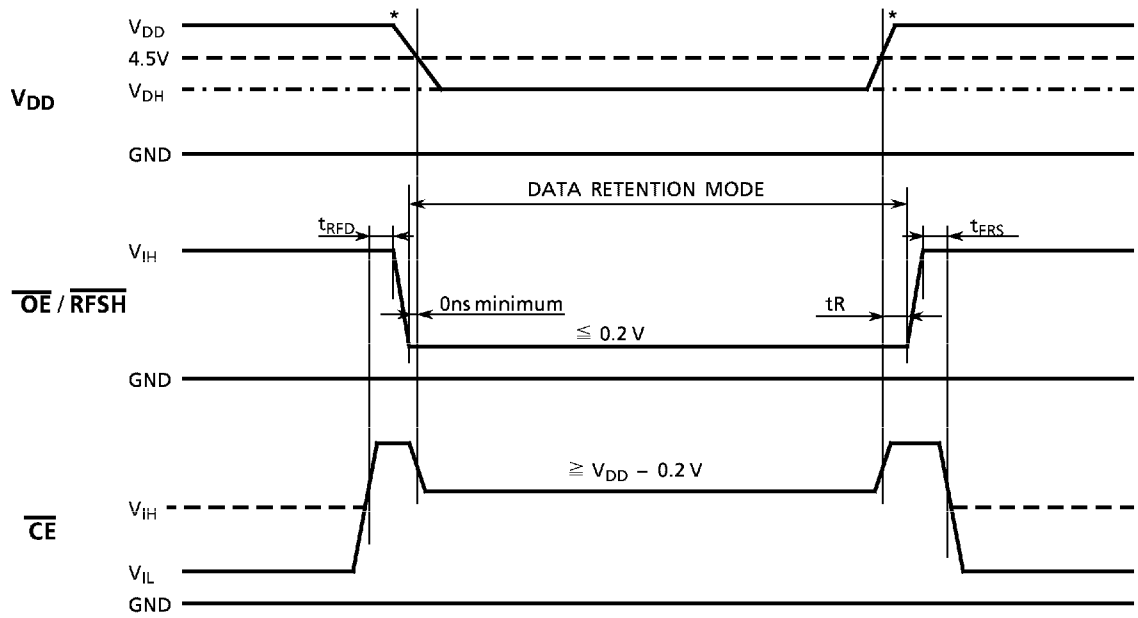
Input Level	:	V_{IH} = 2.6 V
		V_{IL} = 0.6 V
Input Reference Level	:	V_{IH} = 2.4 V
		V_{IL} = 0.8 V
Output Reference Level:		V_{OH} = 2.2 V
		V_{OL} = 0.8 V



8) Measured with a load equivalent to 1 TTL load and 100 pF.
9) Parameters t_{CHZ}, t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, input data is latched at the earlier of the R/W or $\overline{CE}$ rising edge. Therefore, input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched on the falling edge of $\overline{CE}$. Therefore, all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operations—auto refresh and self refresh—are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min)
    The timing parameter (t_{FRS}) must be observed for proper device operation in accordance with the following conditions.
    - After self refresh
    - When $\overline{OE}/\overline{RFSH}$ = " L " after power-up

DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage		2.7	–	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.3 V	–	–	40	μA
		V_{DH} = 3.6 V	–	–	50	μA
		V_{DH} = 5.5 V	–	–	100	μA
t_R	Recovery Time		5	–	–	mS



(Note)◦ R/W, A0 to A18 = Don't care.

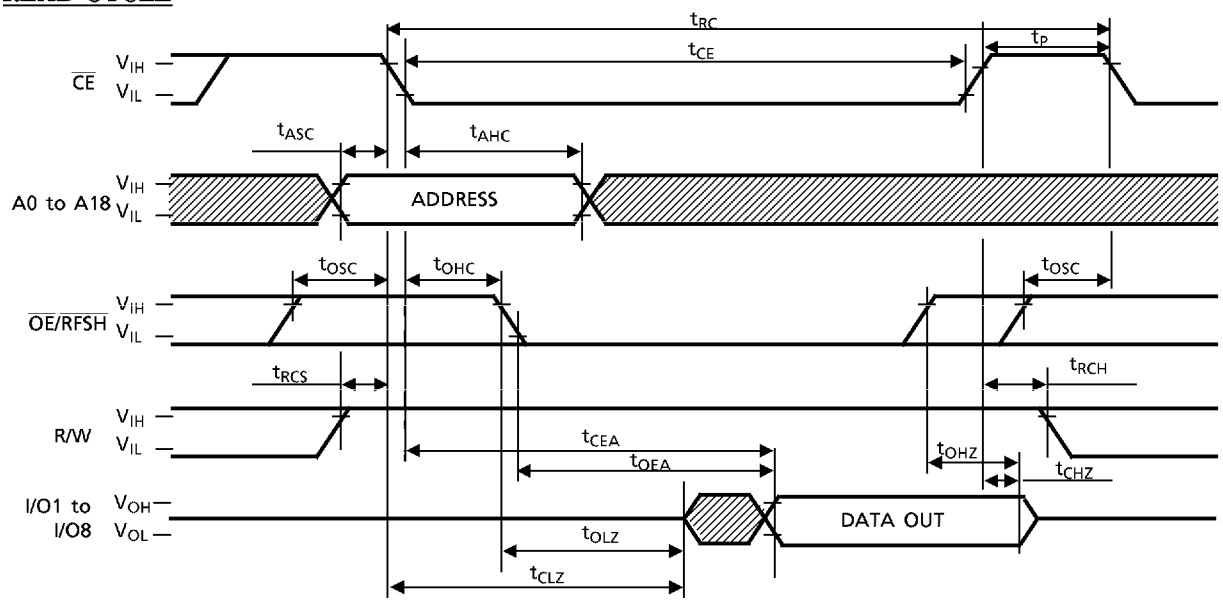
◦ I_{DDF1} is applied with $\overline{OE}/\overline{RFSH}$ = $V_{IL\ max}$, $\overline{CE}$ = $V_{IH\ min}$

◦ In all states except Data Retention Mode, Auto Refresh or CE-Only Refresh with 2048 cycles per 32 ms is required.

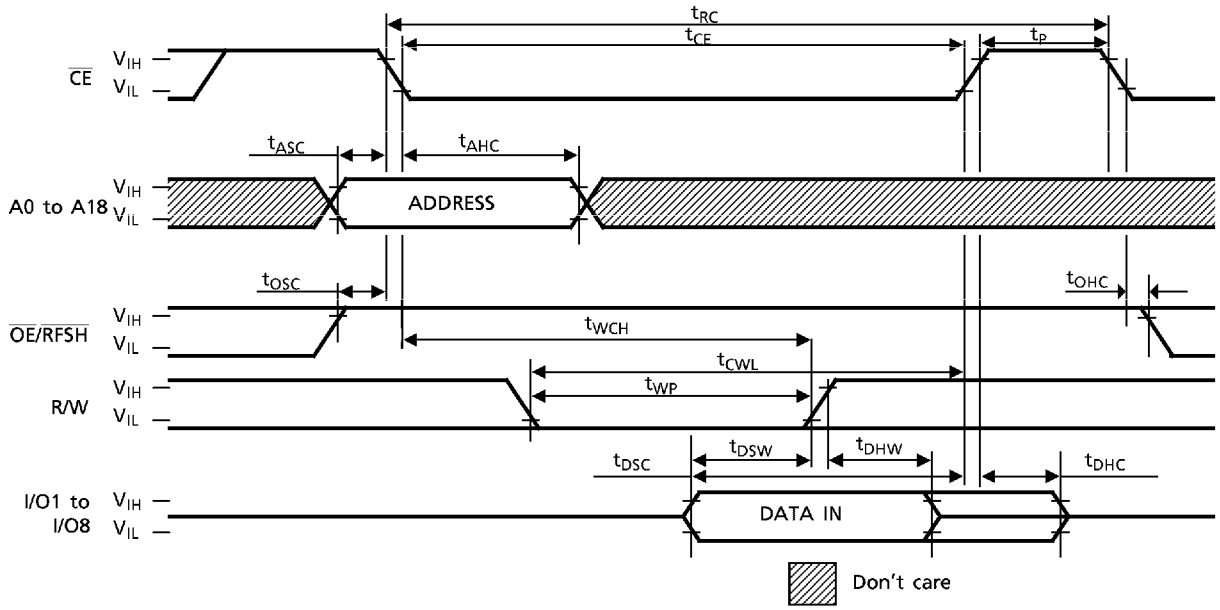
* The raising and falling slope of V_{DD} should be more than 50 ms in order to operate the device safely (20 ms/V).

TIMING DIAGRAMS

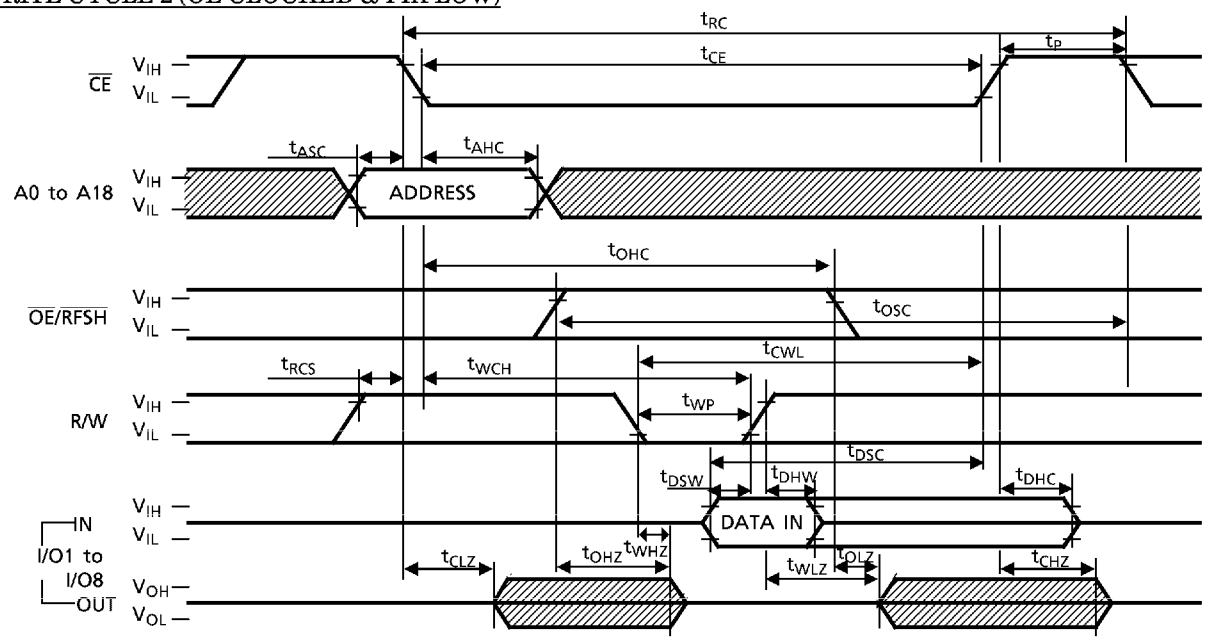
READ CYCLE



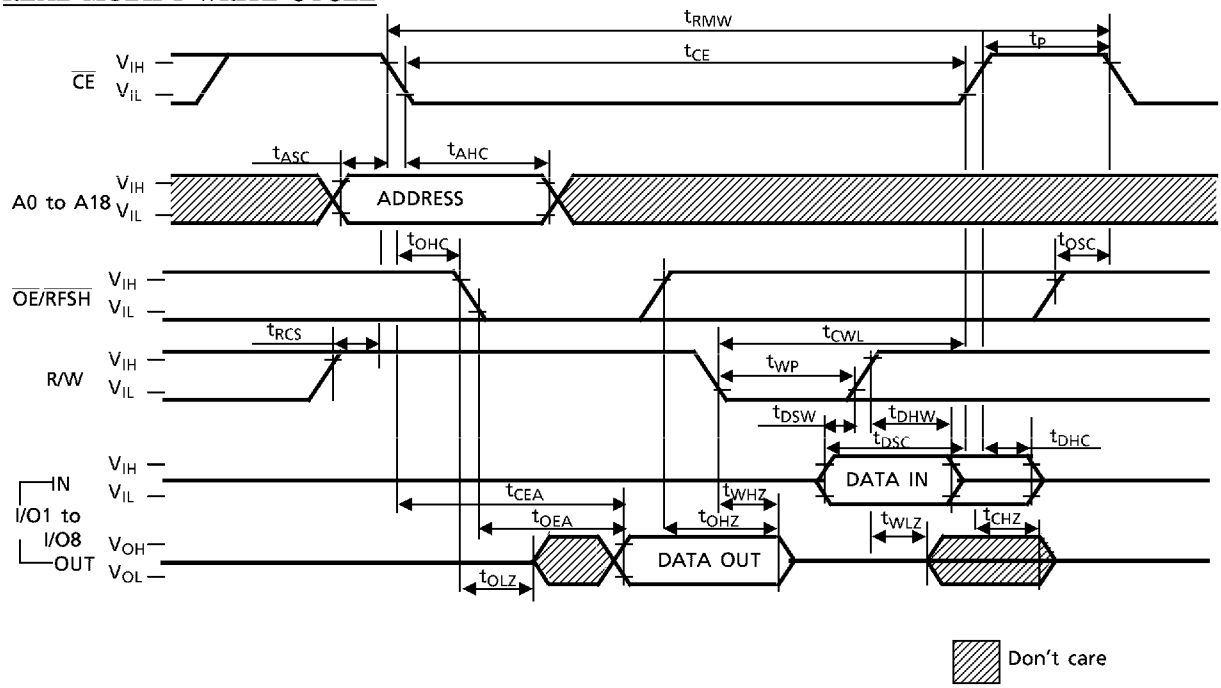
WRITE CYCLE 1 ($\overline{OE}$ High)



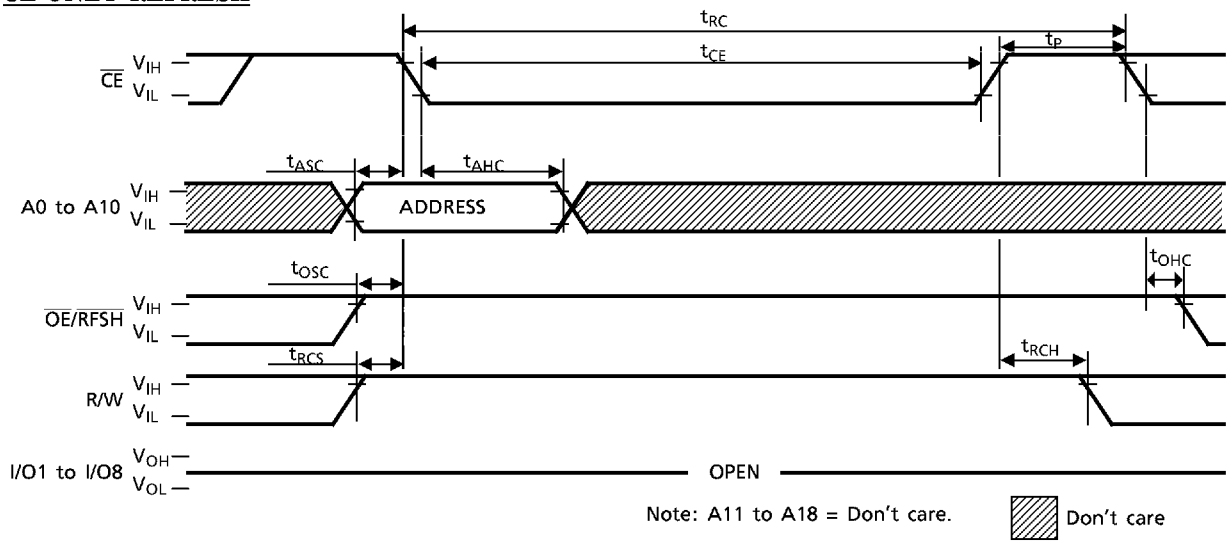
WRITE CYCLE 2 ($\overline{OE}$ CLOCKED & FIX LOW)



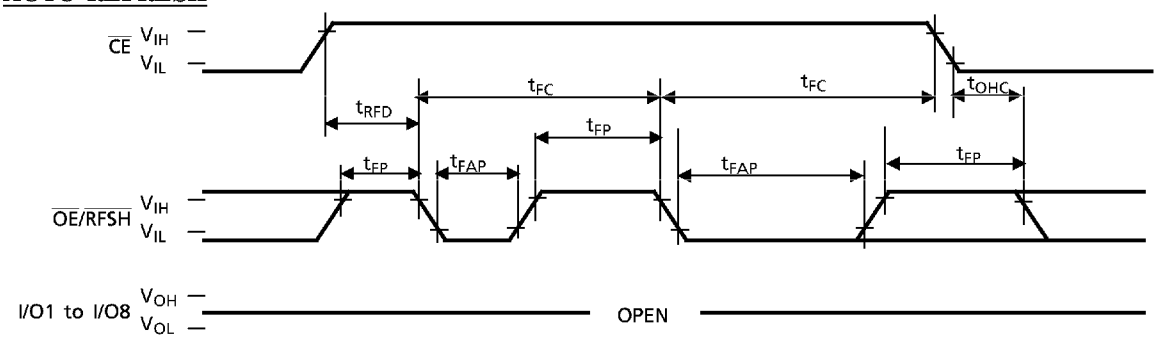
READ-MODIFY-WRITE CYCLE



$\overline{CE}$-ONLY REFRESH

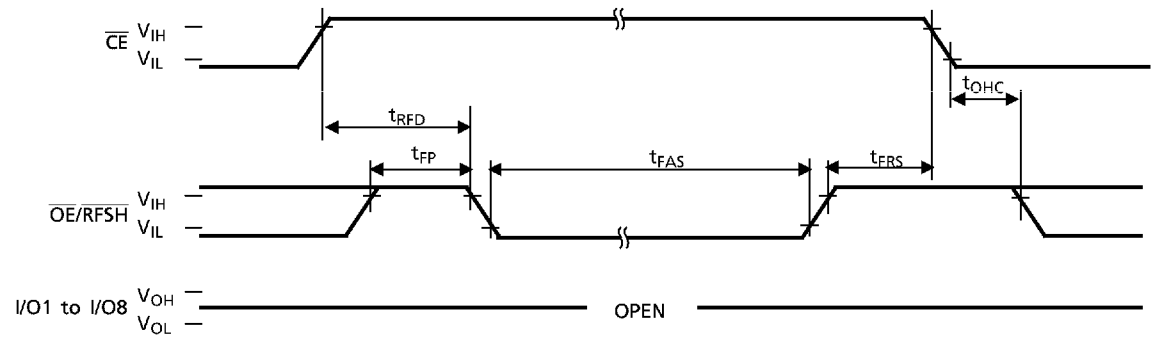


AUTO REFRESH



Note: R/W, A0 to A18 = Don't care.

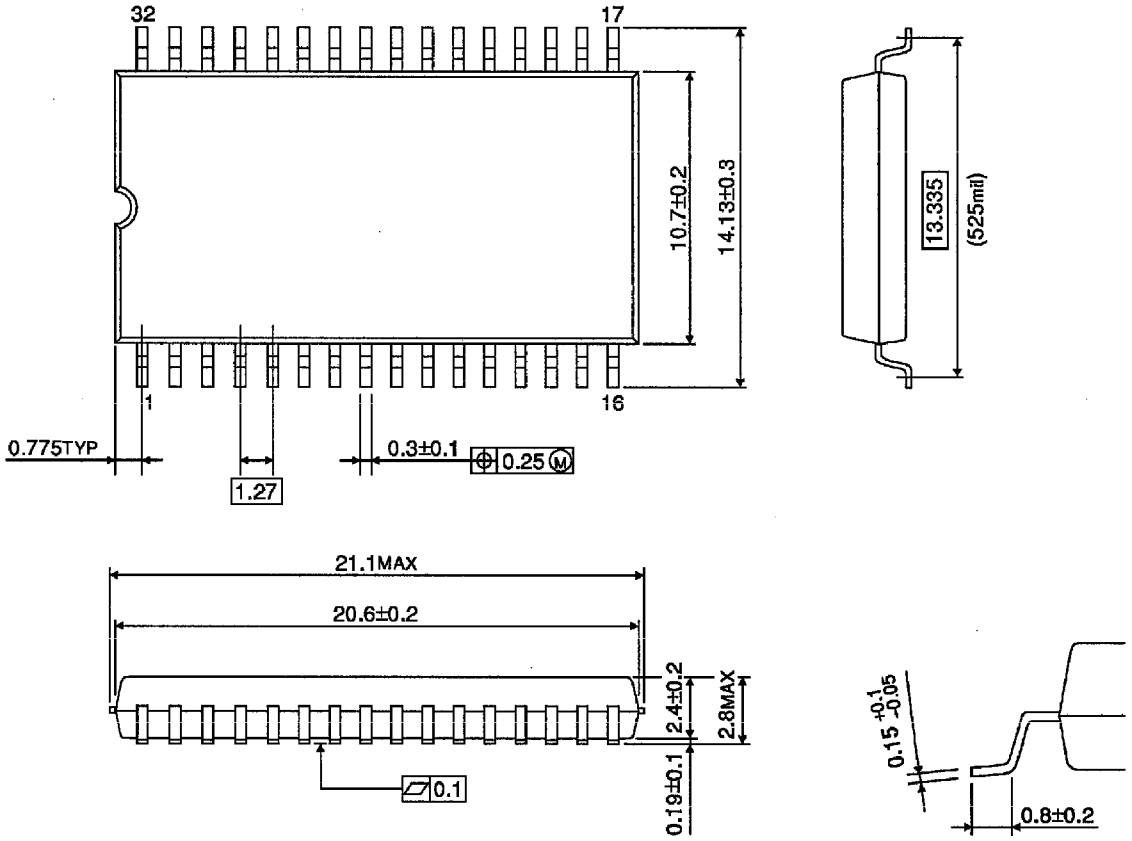
SELF REFRESH



Note: R/W, A0 to A18 = Don't care.

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

Units in mm

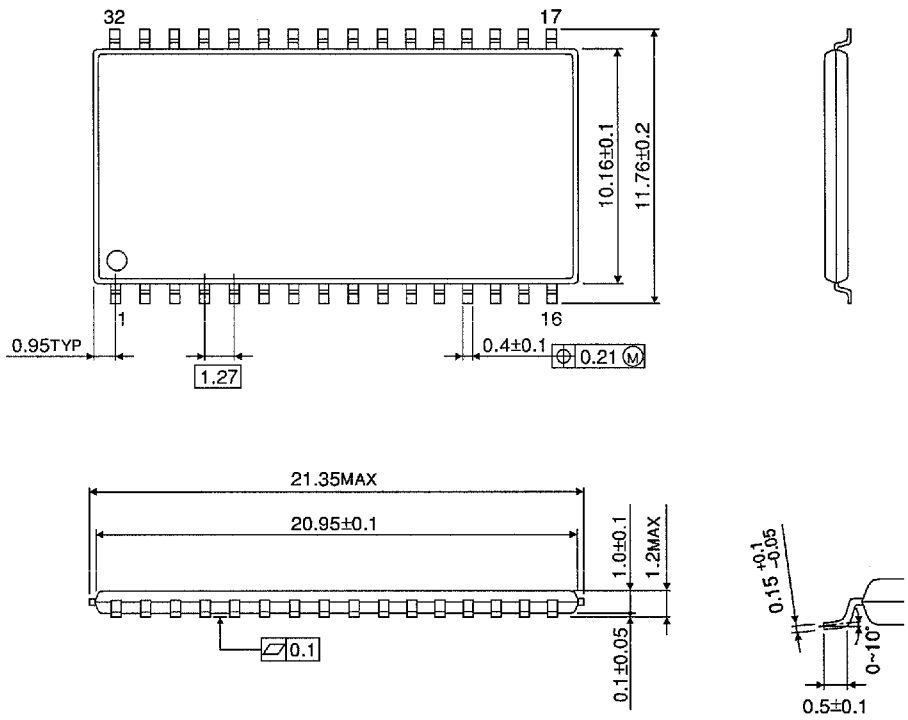


Weight: 1.10 g (typ)

TC518512AF - 70, - 80, - 10

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

Units in mm



Weight: 0.51 g (typ)

TC518512AFT - 70, - 80, - 10