

T-46-07-05

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

**Octal 3-State Noninverting
Transparent Latch with
LSTTL-Compatible Inputs
High-Performance Silicon-Gate CMOS**

The MC54/74HCT373 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT373 is identical in pinout to the LS373.

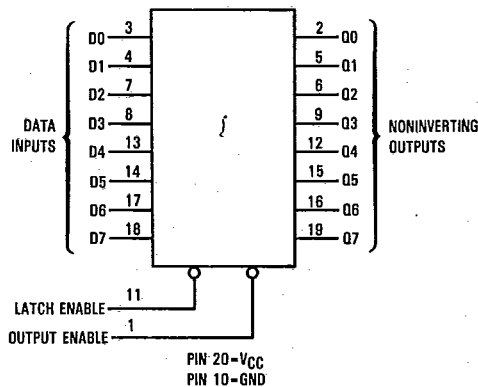
The eight latches of the HCT373 are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

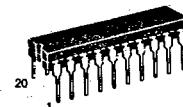
The HCT373 is identical in function to the HCT573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT533, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

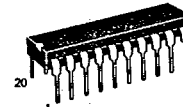
LOGIC DIAGRAM



MC54/74HCT373



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



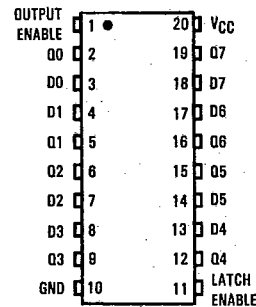
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74HCTXXXN Plastic
MC54HCTXXXJ Ceramic
MC74HCTXXXDW SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output	
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.70	μA
			5.5	0.1	0.1	0.1	
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} =V _{IL} or V _{IH} V _{out} =V _{CC} or GND	4.5	0.26	0.33	0.40	μA
			5.5	±0.1	±1.0	±1.0	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	4.5	±0.5	±5.0	±10.0	μA
			5.5	8	80	160	

ΔI _{CC}	Additional Quiescent Supply Current	V _{in} =2.4 V, Any One Input V _{in} =V _{CC} or GND, Other Inputs I _{out} =0 μA	≥ -55°C		25°C to 125°C	mA
			2.9	2.4		
5.5						

NOTES:

- Information on typical parametric values can be found in Chapter 4.
- Total Supply Current = I_{CC} + ΣΔI_{CC}.

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AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0 V ± 10%, C_L=50 pF, Input t_r=t_f=6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	35	44	53	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	35	44	53	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

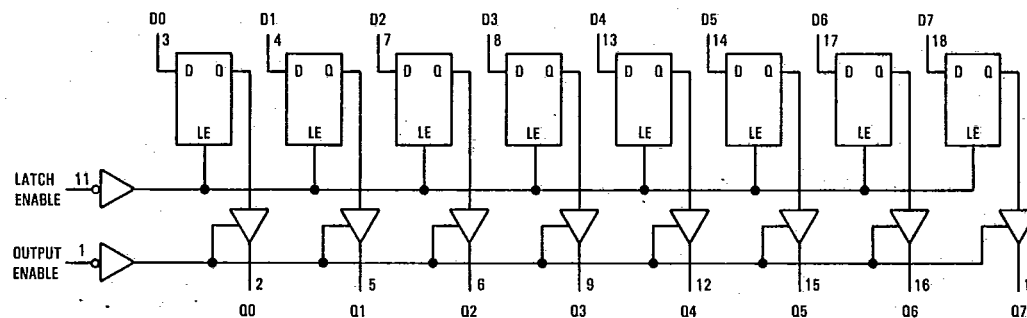
C _{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} =5.0 V	pF
		65	

TIMING REQUIREMENTS (V_{CC}=5.0 V ± 10%, Input t_r=t_f=6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, input D to Latch Enable (Figure 4)	10	13	15	ns
t _h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	10	13	15	ns
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	16	20	24	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

EXPANDED LOGIC DIAGRAM



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SWITCHING WAVEFORMS

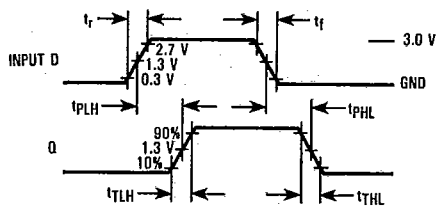


Figure 1

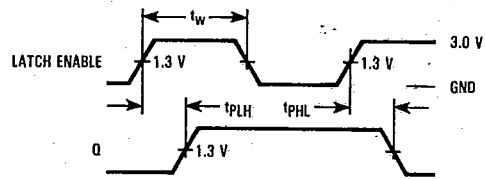


Figure 2

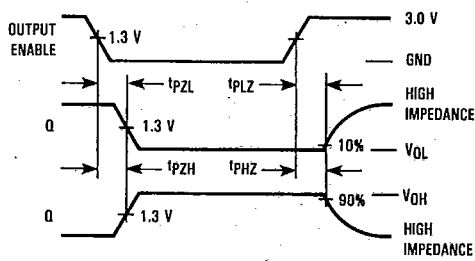


Figure 3

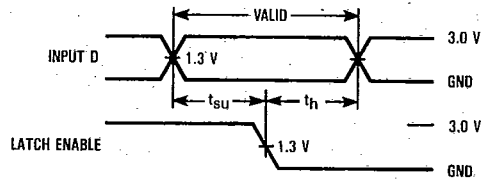
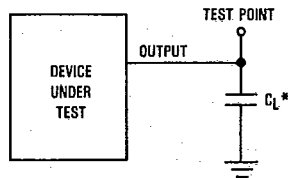
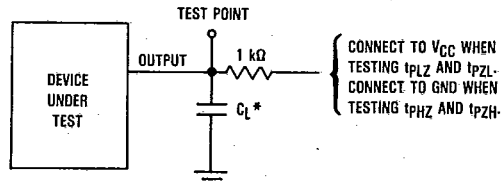


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

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