Signetics

54F657
Transceiver

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker (3-State Outputs)

Military Logic Products

Product Specification

FEATURES

- **High-impedance NPN base input for reduced loading (20 in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **24-pin slim dip (300-mil) package**
- **3-State outputs**
- **Outputs sink 48mA**
- **12mA source current**
- **Input diodes for termination effects**

DESCRIPTION

The 54F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 48mA at the B ports. The Transmit/Receive (T/R) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active High) enables data from A ports to B ports; Receive (active Low) enables data from B ports to A ports.

ORDERING INFORMATION

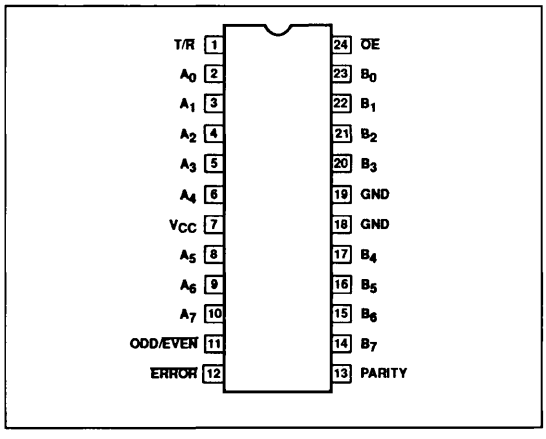
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F657/BLA
24-Pin Ceramic FlatPack	54F657/BKA
28-Pin Ceramic LLCC	54F657/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

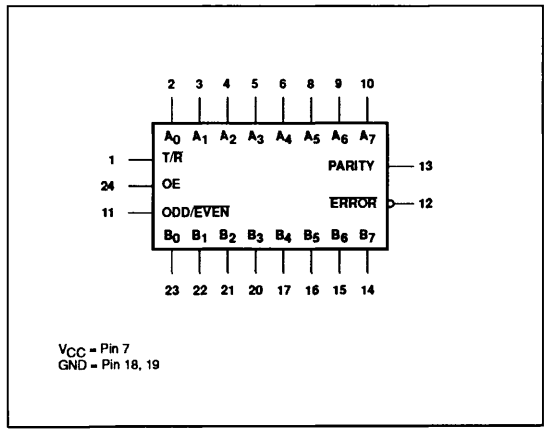
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A ports 3-State inputs	5.0/0.167	100μA/100μA
B_0 - B_7	B ports 3-State inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/R	Transmit/receive input	2.0/0.066	40μA/40μA
$\overline{ODD}$/EVEN	ODD/EVEN input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active Low)	2.0/0.066	40μA/40μA
A_0 - A_7	A ports 3-State outputs	150/33.3	3mA/20mA
B_0 - B_7	B ports 3-State outputs	600/80	12mA/48mA
PARITY	Parity output	150/33.3	3mA/20mA
$\overline{ERROR}$	Error output	150/33.3	3mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as 20μA in the High state and 0.6mA in the Low state.

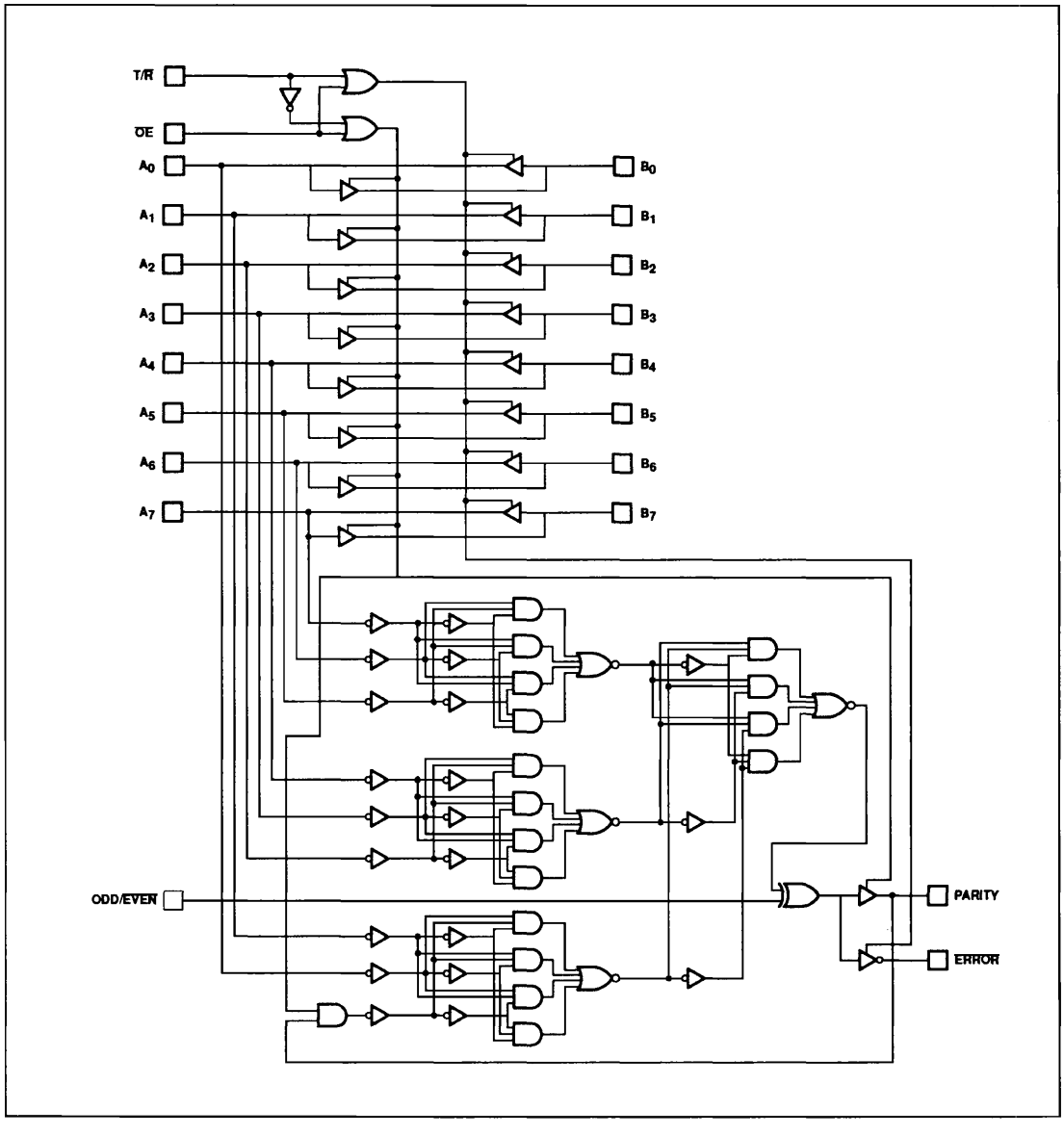
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM



The Output Enable inputs disable both the A and B ports by placing them in a High-Z condition when either the $\overline{OE}$ input is High or the $\overline{OE}$ input is Low.

The parity generator detects whether an even or odd number of bits on the A ports are High, depending on the condition of the Parity Select input. If the Even input is active High and an even number of A inputs are High, the Parity output is High. The parity of the data received on the B ports is compared with the Parity Select input and the Error output is Low if not equal.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	(Z)	Transmit
	L	H	L	L	(Z)	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	(Z)	Transmit
	L	H	L	H	(Z)	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	(Z)	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z)= High impedance state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in Huigh output state range		-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	A_0 - A_7	40	mA
		B_0 - B_7, PARITY, $\overline{ERROR}$	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage[4]		2.0			V
V_{IL}	Low-level input voltage[4]				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH2}	High-level output current	A_0 - A_7 & B_0 -B_7			-3	mA
		B_0 - B_7, PARITY, $\overline{ERROR}$			-12	mA
I_{OH1}	High-level output current	A_0 - A_7 & B_0 - B_7			-1	mA
I_{OL}	Low-level output current	A_0 - A_7			20	mA
		B_0 - B_7, PARITY, $\overline{ERROR}$			48	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All outputs	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH} = -3mA	2.4			V
				I_{OH} = -1mA	2.5	3.4		V
		B_0 - B_7, PARITY $\overline{ERROR}$		I_{OH} = -12mA	2.0			V
V_{OL}	Low-level output voltage	A_0 - A_7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 20mA		.35	.50	V
		B_0 - B_7, PARITY $\overline{ERROR}$		I_{OL} = 48mA		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	T/$\overline{R}$, $\overline{OE}$, ODD/$\overline{EVEN}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_7	V_{CC} = 5.5V, V_I = 5.5V				2	mA
		B_0 - B_7	V_{CC} = 5.5V, V_I = 5.5V				1	mA
I_{IH1}	High-level input current	ODD/$\overline{EVEN}$	V_{CC} = Max, V_I = 2.7V				20	µA
		T/$\overline{R}$, $\overline{OE}$					40	µA
I_{IL}	Low-level input current	ODD/$\overline{EVEN}$	V_{CC} = Max, V_I = 0.5V				-20	µA
		T/$\overline{R}$, $\overline{OE}$					-40	µA
I_{IH} + I_{OZH}	Off-state current High level voltage applied	A_0 - A_7	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				100	µA
I_{IH} + I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-100	µA
I_{IH} + I_{OZH}	Off-state current High level voltage applied	B_0 - B_7 PARITY	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				70	µA
I_{IH} + I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-70	µA
I_{OZH}	Off-state current High level voltage applied	$\overline{ERROR}$	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]	A_0 - A_7	V_{CC} = Max		-60		-150	mA
		B_0 - B_7			-100		-225	mA
I_{CC}	Supply current (total	I_{CCH}	V_{CC} = Max			90	125	mA
		I_{CCL}				106	150	mA
		I_{CCZ}				98	145	mA

AC ELECTRICAL CHARACTERISTICS

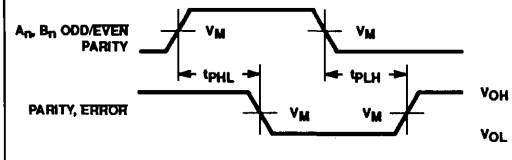
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ[2]	Max	Min	Max	
t_{PLH1} t_{PHL1}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.5 8.5	ns ns
t_{PLH2} t_{PHL2}	Propagation delay A_n to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 14.0	6.5 6.5	18.0 18.5	ns ns
t_{PLH3} t_{PHL3}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.0 4.0	13.0 14.5	ns ns
t_{PLH4} t_{PHL4}	Propagation delay B_n to $\overline{\text{ERROR}}$	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.0 7.0	24.0 25.5	ns ns
t_{PLH5} t_{PHL5}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.0 7.5	18.0 19.5	ns ns
t_{PZH} t_{PZL}	Output enable time[5] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.5 12.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.5 8.0	ns ns

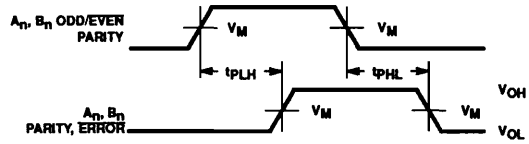
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. When testing devices to the functional table specified refer to the "Recommended Operating Conditions" section of the Applications Note 202, "Testing and Specifying FAST Logic".
5. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$. VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY).

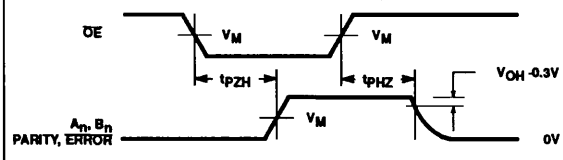
AC WAVEFORMS



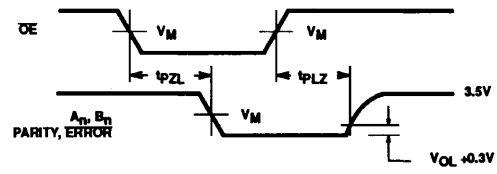
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



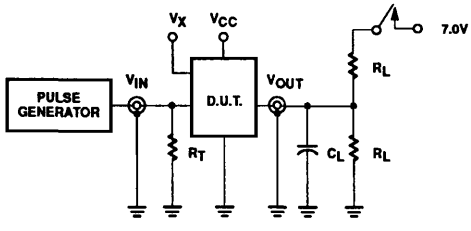
Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



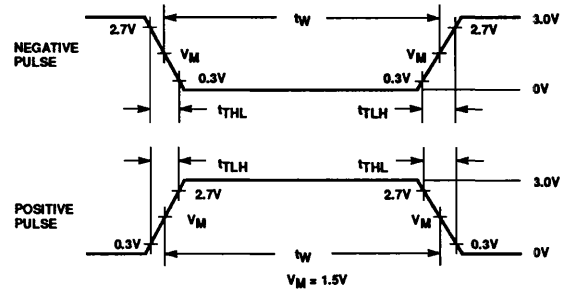
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at:: ≤0.8V, ≥2.7V or open per FunctionTable.