National Semiconductor

54AC/74AC646 • 54ACT/74ACT646
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

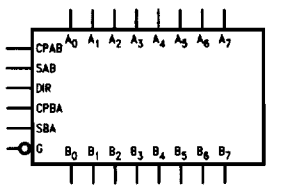
The 'AC/'ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1-4*.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACT646 has TTL compatible inputs
- Standard Military Drawing (SMD)
  — 'AC646: 5962-89682

Ordering Code: See Section 8

Logic Symbols



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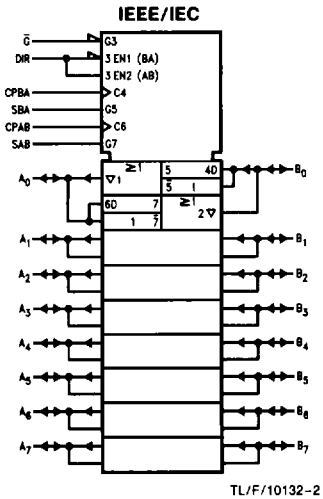

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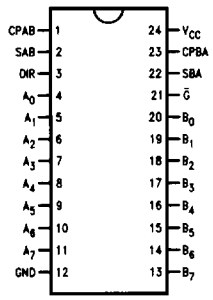
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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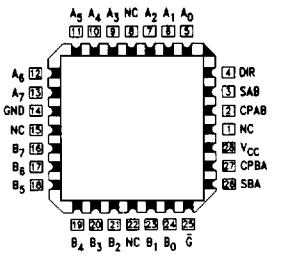
Pin Assignment for LCC and PCC



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Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Real Time Transfer A-Bus to B-Bus

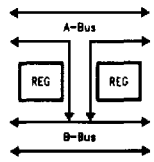

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

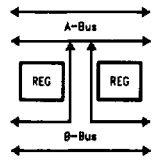

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FIGURE 2

Storage from Bus to Register

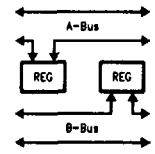

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FIGURE 3

Transfer from Register to Bus

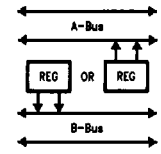

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FIGURE 4

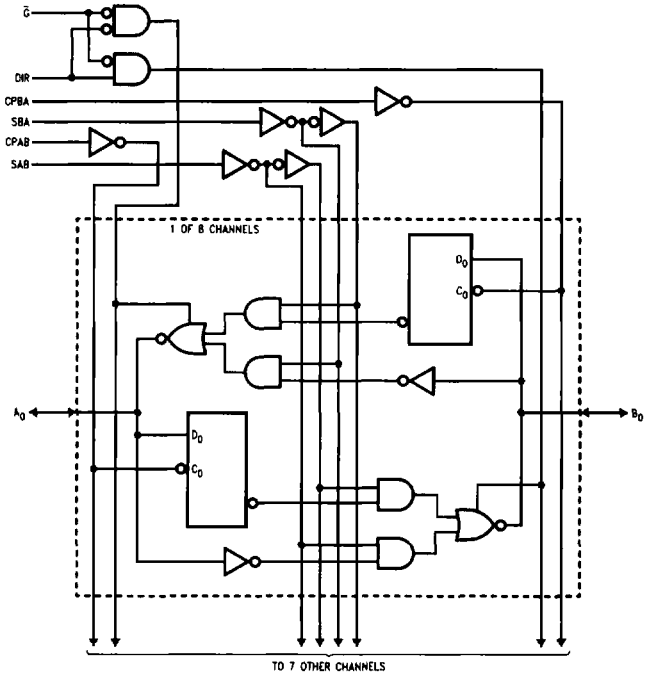
Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock A_n Data into A Register
H	X	X	↗	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↗	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↗	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		I_{OH} −24 mA
		5.5		4.86	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		I_{OL} 24 mA
		5.5		0.36	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	4.0 2.5	10.5 7.5	16.5 12.0	1.0 1.0	20.0 14.0	3.0 2.0	18.5 13.0	ns	2-3, 4
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	3.0 2.0	9.5 6.5	14.5 10.5	1.0 1.0	17.5 12.0	2.5 1.5	16.0 11.5	ns	2-3, 4
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	2.5 1.5	7.5 5.0	12.0 8.0	1.0 1.0	15.0 10.0	2.0 1.0	13.5 9.0	ns	2-3, 4
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	7.5 5.0	12.5 9.0	1.0 1.0	14.5 9.5	1.5 1.0	13.5 9.5	ns	2-3, 4
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	2.0 1.5	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.5 11.0	ns	2-3, 4
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.0 11.0	ns	2-3, 4
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	1.0 1.0	13.0 9.5	2.0 1.5	12.5 9.0	ns	2-5
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	1.0 1.0	15.5 11.0	2.0 1.5	14.0 10.0	ns	2-6
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	3.0 2.0	8.0 6.5	12.5 10.0	1.0 1.0	14.0 11.5	2.5 2.0	13.5 11.0	ns	2-5
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.0 1.5	7.5 6.0	12.0 9.5	1.0 1.0	13.5 11.0	2.0 1.5	13.5 10.5	ns	2-6
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	2.0 1.5	6.5 5.0	11.0 7.5	1.0 1.0	14.5 10.5	1.5 1.0	12.0 8.5	ns	2-5
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.0	1.0 1.0	16.0 12.5	2.0 1.0	13.0 9.0	ns	2-6
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.5	1.0 1.0	14.5 12.0	1.5 1.5	12.5 10.0	ns	2-5
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.5 1.5	7.5 5.5	12.0 9.5	1.0 1.0	16.5 12.0	1.5 1.5	13.5 10.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	5.0 4.0	6.0 4.5	5.5 4.5	ns	2-7
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 0.5	1.5 2.0	0 1.0	ns	2-7
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.5	5.0 5.0	4.5 3.5	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5			3.0	16.0	ns	2-3, 4
t_{PHL}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5			3.5	16.0	ns	2-3, 4
t_{PLH}	Propagation Delay Bus to Bus	5.0	4.5	8.5	10.5			2.5	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay Bus to Bus	5.0	5.0	8.5	10.5			2.0	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay SBA or SAB to A_n to B_n (w/A_n or B_n HIGH or LOW)	5.0	5.0	9.5	11.5			2.5	12.5	ns	2-3, 4
t_{PHL}	Propagation Delay SBA or SAB to A_n to B_n (w/A_n or B_n HIGH or LOW)	5.0	5.0	9.5	11.5			2.5	12.5	ns	2-3, 4
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	5.0	6.0	9.0	11.0			1.5	12.0	ns	2-5
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	5.0	5.0	9.0	11.0			3.0	12.0	ns	2-6
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	7.5	10.5	13.0			4.5	14.5	ns	2-5
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	5.5	10.0	12.5			3.0	14.0	ns	2-6
t_{PZH}	Enable Time DIR to A_n or B_n	5.0	5.5	6.5	10.5			1.5	11.5	ns	2-5
t_{PZL}	Enable Time DIR to A_n or B_n	5.0	4.0	6.5	10.5			3.0	11.5	ns	2-6
t_{PHZ}	Disable Time DIR to A_n or B_n	5.0	5.5	8.5	12.5			4.5	13.5	ns	2-5
t_{PLZ}	Disable Time DIR to A_n or B_n	5.0	4.0	8.5	12.5			3.0	13.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW BUS to Clock	5.0	2.5	7.0		8.0	ns	2-7
t_h	Hold Time, HIGH or LOW Bus to Clock	5.0	0	2.5		2.5	ns	2-7
t_w	Clock Pulse Width HIGH or LOW	5.0	4.5	7.0		8.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V