

## 8M-Bit (1M X8) CMOS MASK ROM

### FEATURES

- 1,048,576x 8 bit organization
- Fast access time :120ns(max.)
- Supply voltage : single +5V
- Current consumption  
Operating :60 mA(max.)  
Standby : 50  $\mu$ A (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package  
- KM23C8000C : 32-DIP-600  
- KM23C8000CG : 32-SOP-525

### GENERAL DESCRIPTION

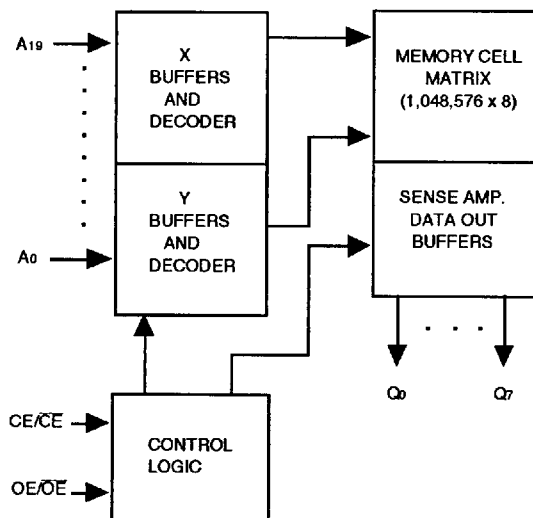
The KM23C8000C is a fully static mask programmable ROM organized 1,048,576x8bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

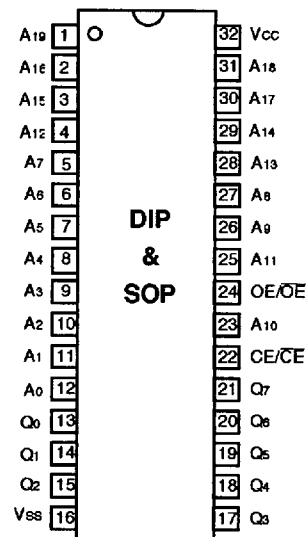
It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C8000C is packaged in a 32-DIP, and the KM23C8000CG in a 32-SOP, provide polarity programmable CE and OE buffer as user option mode.

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION



**KM23C8000C**  
**(KM23C8000CG)**

| Pin Name | Pin Function   |
|----------|----------------|
| A0-A19   | Address Inputs |
| Q0-Q7    | Data Outputs   |
| CE/CE*   | Chip Enable    |
| OE/OE*   | Output Enable  |
| Vcc      | Power (+5V)    |
| Vss      | Ground         |

\* User Selectable Polarity

### ABSOLUTE MAXIMUM RATINGS

| Item                               | Symbol            | Rating       | Unit |
|------------------------------------|-------------------|--------------|------|
| Voltage on Any Pin Relative to Vss | V <sub>IN</sub>   | -0.3 to +7.0 | V    |
| Temperature Under Bias             | T <sub>bias</sub> | -10 to +85   | °C   |
| Storage Temperature                | T <sub>stg</sub>  | -55 to +150  | °C   |

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T<sub>A</sub>= 0 to 70°C)

| Item           | Symbol          | Min | Typ | Max | Unit |
|----------------|-----------------|-----|-----|-----|------|
| Supply Voltage | V <sub>CC</sub> | 4.5 | 5.0 | 5.5 | V    |
| Supply Voltage | V <sub>SS</sub> | 0   | 0   | 0   | V    |

### DC CHARACTERISTICS

| Parameter                      | Symbol           | Test Conditions                                      | Min  | Max                   | Unit |
|--------------------------------|------------------|--|------|-----------------------|------|
| Operating Current              | I <sub>CC</sub>  | CE=OE=V <sub>IL</sub> , f=6.7MHz<br>all outputs open | -    | 60                    | mA   |
| Standby Current (TTL)          | I <sub>SB1</sub> | CE=V <sub>IH</sub> , all outputs open                | -    | 1                     | mA   |
| Standby Current (CMOS)         | I <sub>SB2</sub> | CE=V <sub>CC</sub> , all outputs open                | -    | 50                    | μA   |
| Input Leakage Current          | I <sub>I</sub>   | V <sub>IN</sub> =0 to V <sub>CC</sub>                | -    | 10                    | μA   |
| Output Leakage Current         | I <sub>O</sub>   | V <sub>OUT</sub> =0 to V <sub>CC</sub>               | -    | 10                    | μA   |
| Input High Voltage, All Inputs | V <sub>IH</sub>  |  | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage, All Inputs  | V <sub>IL</sub>  |  | -0.3 | 0.8                   | V    |
| Output High Voltage Level      | V <sub>OH</sub>  | I <sub>OH</sub> = - 400 μA                           | 2.4  | -                     | V    |
| Output Low Voltage Level       | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1 mA                             | -    | 0.4                   | V    |

### CAPACITANCE (T<sub>A</sub>=25°C, f=1.0MHz)

| Item               | Symbol           | Test Conditions       | Min | Max | Unit |
|--------------------|------------------|-----------------------|-----|-----|------|
| Output Capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> = 0V | -   | 12  | pF   |
| Input Capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> = 0V  | -   | 12  | pF   |

Note : Capacitance is periodically sampled and not 100% tested.

### MODE SELECTION

| CE/CE | OE/OE | Mode      | Data   | Power   |
|-------|-------|-----------|--------|---------|
| L/H   | X     | Standby   | High-Z | Standby |
| H/L   | L/H   | Operating | High-Z | Active  |
|       | H/L   | Operating | Dout   | Active  |

**AC CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ , unless otherwise noted.)

**TEST CONDITIONS**

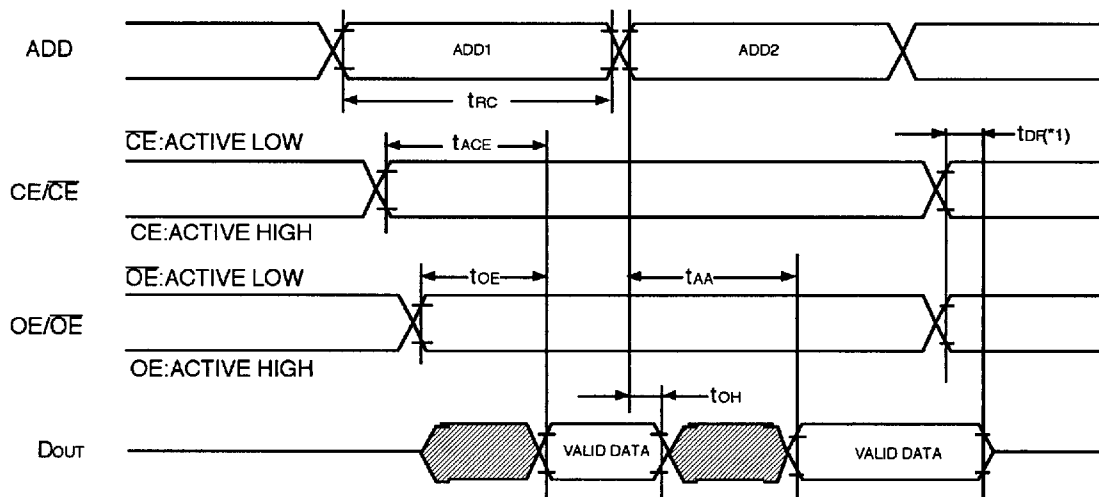
| Item                           | Value                               |
|--------------------------------|-------------------------------------|
| Input Pulse Levels             | 0.6V to 2.4V                        |
| Input Rise and Fall Times      | 10ns                                |
| Input and Output timing Levels | 0.8V and 2.0V                       |
| Output Loads                   | 1 TTL Gate and $C_L = 100\text{pF}$ |

**READ CYCLE**

| Parameter                               | Symbol           | KM23C8000C-12 |     | KM23C8000C-15 |     | KM23C8000C-20 |     | Unit |
|---|------------------|---------------|-----|---------------|-----|---------------|-----|------|
|   |                  | Min           | Max | Min           | Max | Min           | Max |      |
| Read Cycle Time                         | t <sub>RC</sub>  | 120           |     | 150           |     | 200           |     | ns   |
| Chip Enable Access Time                 | t <sub>ACE</sub> |               | 120 |               | 150 |               | 200 | ns   |
| Address Access Time                     | t <sub>AA</sub>  |               | 120 |               | 150 |               | 200 | ns   |
| Output Enable Access Time               | t <sub>OE</sub>  |               | 60  |               | 70  |               | 90  | ns   |
| Output or Chip Disable to Output High-Z | t <sub>DF</sub>  |               | 20  |               | 30  |               | 40  | ns   |
| Output Hold from Address Change         | t <sub>OH</sub>  | 0             |     | 0             |     | 0             |     | ns   |

**TIMING DIAGRAM**

**READ**

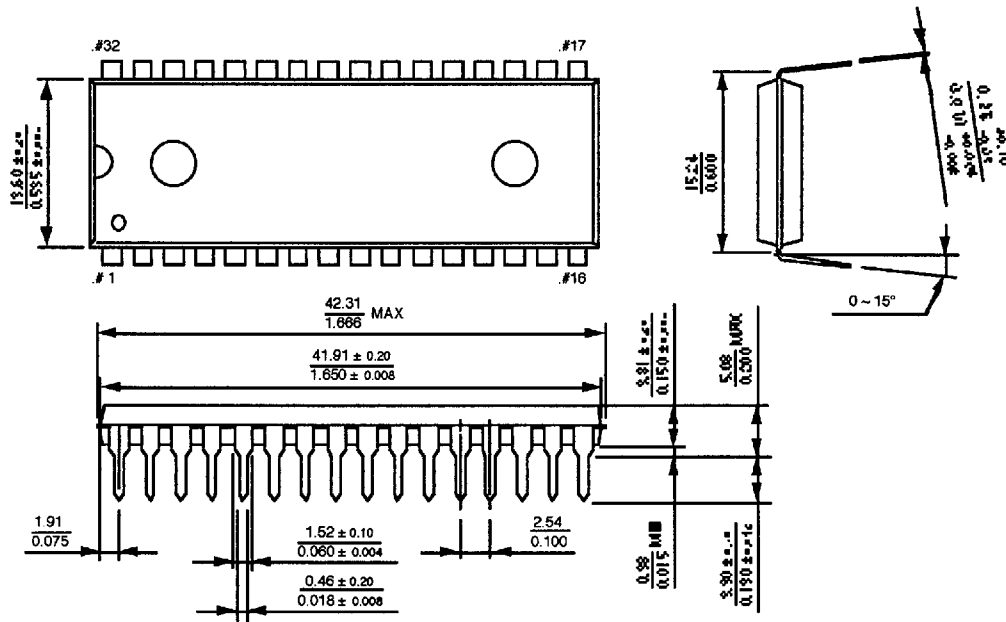


(\*1) t<sub>DF</sub> is defined as the time which the outputs achieve the open circuit condition and is not referenced to V<sub>OH</sub> or V<sub>OL</sub> level.

**PACKAGE DIMENSIONS**

**32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8000C)**

Unit : mm/Inch



**32 LEAD SMALL OUTLINE PACKAGE (KM23C8000CG)**

