250-mA Ultra Low-Noise LDO Regulator with Discharge Option

DESCRIPTION

The SiP21103 is a 250 mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current makes this part attractive for battery operated power systems. The SiP21103 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source, such as RF applications, will benefit from the SiP21103's ultra low output noise. An external noise bypass capacitor connected to the device's BP pin can further reduce the noise level. The SiP21103 is designed to maintain regulation while delivering 400 mA peak current, making it ideal for systems that have a high surge current upon turn-on.

For better transient response and regulation, an active pull-down circuit is built into the SiP21103 to clamp the output voltage when it rises beyond normal regulation. The SiP21103 automatically discharges the output voltage by connecting the output to ground through a 100 Ω N-channel MOSFET when the device is put in shutdown mode.

The SiP21103 features reverse battery protection to limit reverse current flow to approximately 1 µA in the event reversed battery is applied at the input, thus preventing damage to the IC.

The SiP21103 is available in a lead (Pb)-free 5-pin MLP22 PowerPAK package and is specified to operate over the industrial temperature range of - 40 °C to 85 °C.

FEATURES

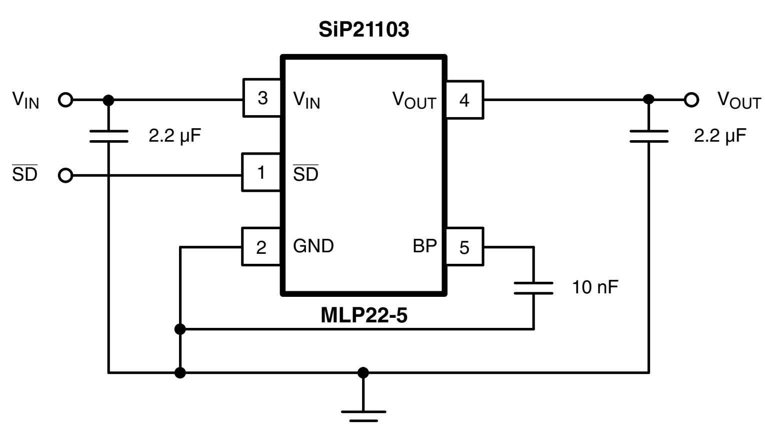
- Ultra low dropout - 250 mV at 250 mA load
- Ultra low noise - 30 μV_{RMS} (10 Hz to 100 kHz)
- Shutdown control
- 130 µA ground current at 250 mA load
- 2 % guaranteed output voltage accuracy
- 400 mA peak output current capability
- Uses low ESR ceramic capacitors
- Fast start-up (50 µs)
- Fast line and load transient response (≤ 30 µs)
- 1 µA maximum shutdown current
- Output current limit
- Reverse battery protection
- Built-in short circuit and thermal protection
- Output, auto-discharge in shutdown mode
- Fixed 1.2 V, 1.8 V, 2.5 V, 2.6 V, 2.8 V, 2.85 V, 3.0 V, 3.3 V, 5.0 V output voltage options
- MLP22-5 PowerPAK® package
- Compliant to RoHS directive 2002/95/EC

Pb-free Available
RoHS*
COMPLIANT

APPLICATIONS

- Cellular phones, wireless handsets
- Noise-sensitive electronic systems, laptop and palmtop computers
- PDAs
- Pagers
- Digital cameras
- MP3 player
- Wireless modem

TYPICAL APPLICATION CIRCUIT



* Pb containing terminations are not RoHS compliant, exemptions may apply .

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Input Voltage, V_{IN} to GND		- 6.0 to 6.5	V
$V_{\overline{SD}}$ (See Detailed Description)		- 0.3 to V_{IN}	
Output Current, I_{OUT}		Short Circuit Protected	
Output Voltage, V_{OUT}		- 0.3 to V_{IN} + 0.3	V
Package Power Dissipation, (P_d)[b]		1.23	W
Thermal Resistance	(Θ_{JA})[a]	65	°C/W
	$R_{(\Theta JC)}$[a]	8	
Maximum Junction Temperature, $T_{J(max)}$		150	°C
Storage Temperature, T_{STG}		- 65 to 150	

Notes:
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 15.4 mW/°C above T_A = 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage, V_{IN}	2 to 6	V
Input Voltage, $V_{\overline{SD}}$	0 to V_{IN}	
Output Current	0 to 250	mA
C_{IN}, C_{OUT}[a] (Ceramic)	2.2	µF
C_{IN}, (Ceramic)	0.01	
Operating Ambient Temperature, T_A	- 40 to 85	°C
Operating Junction Temperature, T_J	- 40 to 125	

Notes:
a. Maximum ESR of C_{OUT}: 0.2 Ω.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified T_A = 25 °C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $V_{\overline{SD}}$ = 1.5 V		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Start-Up BP Current	I_{OUT}	ON/$\overline{OFF}$ = High		Room		1		mA
Input Voltage Range	V_{IN}			Full	2		6	V
Output Voltage Accuracy		1 mA ≤ I_{OUT} ≤ 250 mA	V_{OUT} ≥ 1 8 V	Room	- 2.0	1	2.0	%
				Full	- 3.0	1	3.0	
			V_{OUT} = 1 2 V, 1.5 V	Room	- 2.5	1	2.5	
				Full	- 3.5	1	3.5	
Line Regulation (V_{OUT} ≤ 3 V)	$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$	From V_{IN} = $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V		Full	- 0.06		0.18	%/V
Line Regulation (3.0 V < V_{OUT} ≤ 3.6 V)				Full	0		0.3	
Line Regulation (5 V Version)		From V_{IN} = 5.5 V to 6 V		Full	0		0.4	
Dropout Voltage[d, g] ($V_{OUT(nom)}$ ≥ 2.6 V)	V_{IN} - V_{OUT}	I_{OUT} = 1 mA		Room		1		mV
		I_{OUT} = 50 mA		Room		45	80	
				Full		50	90	
		I_{OUT} = 250 mA		Room		250	350	
				Full			415	
Dropout Voltage[d, g] ($V_{OUT(nom)}$ < 2.6 V, V_{IN} ≥ 2 V)		I_{OUT} = 50 mA		Room		65	100	
				Full			120	
		I_{OUT} = 250 mA		Room		350	520	
				Full			570	

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified T_A = 25 °C, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{IN} = 2 µF, C_{OUT} = 2.0 µF, $V_{\overline{SD}}$ = 1.5 V		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Ground Pin Current[e, g] ($V_{OUT(nom)} \le$ 3 V)	I_{GND}	I_{OUT} = 0 mA		Room		100	150	µA
				Full			180	
		I_{OUT} = 250 mA		Room		120	200	
				Full			330	
Ground Pin Current[e] ($V_{OUT(nom)}$ > 3 V)		I_{OUT} = 0 mA		Room		110	170	
				Full			200	
		I_{OUT} = 250 mA		Room		140	225	
				Full			275	
Peak Output current	$I_{O(peak)}$	$V_{OUT} \ge 0.95 \times V_{OUT(nom)}$, t_{PW} = 2 ms		Full	400			mA
Output Noise Voltage	e_N	V_{NOM} = 2.6 V, BW = 10 Hz to 100 kHz, 0 mA < I_{OUT} < 250 mA, C_{NOISE} = 0.01 µF		Room		30		µV(rms)
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 250 mA	f = 1 kHz	Room		60		dB
			f = 10 kHz	Room		40		
			f = 100 kHz	Room		30		
Dynamic Line Regulation	$\Delta V_{O(line)}$	V_{IN} : $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V t_r/t_f = 2 µs, I_{OUT} = 250 mA		Room		20		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	I_{OUT} : 1 mA to 250 mA, t_r/t_f = 2 µs		Room		20		
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$			Room		150		°C
Thermal Hysteresis	T_{HYST}			Room		20		
Reverse Current	I_R	V_{IN} = - 6.0 V		Room		1		µA
Short Circuit Current	I_{SC}	V_{OUT} = 0 V		Room		700		mA
Shutdown								
Shutdown Supply Current	$I_{CC(off)}$	$V_{\overline{SD}}$ = 0 V		Room		0.1	1	µA
$\overline{SD}$ Pin Input Voltage	$V_{\overline{SD}}$	High = Regulator ON (Rising)		Full	1.5		V_{IN}	V
		Low = Regulator OFF (Falling)		Full			0.4	
Auto Discharge Resistance	R_DIS			Room		100		Ω
$\overline{SD}$ Pin Input Current[f]	$I_{IN(\overline{SD})}$	$V_{\overline{SD}}$ = 1.5 V, V_{IN} = 6 V		Room		0.7		µA
$\overline{SD}$ Hysteresis	$V_{HYST(\overline{SD})}$			Full		150		mV
V_{OUT} Turn-On Time	t_{ON}	$V_{\overline{SD}}$ (See Figure 1), I_{LOAD} = 100 nA				50		µS

Notes:
a. Room = 25 °C, Full = - 40 °C to 85 °C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at $V_{OUT} \ge$ 2 V are measured at VOUT = 3.3 V, while typical values for dropout voltage at V_{OUT} < 2 V are measured at V_{OUT} = 1.8 V.
d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2 % below the output voltage measured with a 1 V differential, provided that V_{IN} does not drop below 2.0 V.
e. Ground current is specified for normal operation as well as "drop-out" operation.
f. The device's shutdown pin includes a typical 2 MΩ internal pull-down resistor connected to ground.
g. $V_{OUT(nom)}$ is V_{OUT} when measured with a 1 V differential to V_{IN}.

TIMING WAVEFORMS

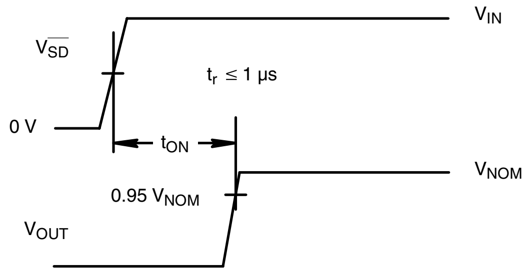
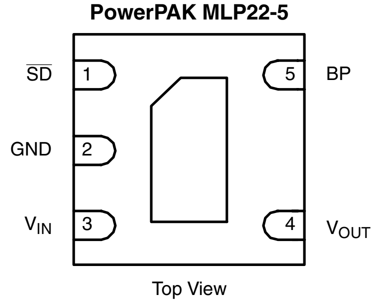


Figure 1. Timing Diagram for Power-Up

PIN CONFIGURATION



PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	$\overline{SD}$	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused
2	GND	Ground pin. For better thermal capability, directly connected to large ground plane
3	V_{IN}	Input supply pin. Bypass this pin with a 1 µF ceramic or tantalum capacitor to ground
4	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.
5	BP	Noise bypass pin. For low noise applications, a 0.01 µF ceramic capacitor should be connected from this pin to ground.

ORDERING INFORMATION				
Lead (Pb)-free Part Number	**Marking**	**Voltage**	**Temperature Range**	**Package**
SiP21103DLP-12-E3	X0LL	1.2	- 40 °C to 85 °C	MLP22-5
SiP21103DLP-18-E3	A0LL	1.8		
SiP21103DLP-25-E3	A3LL	2.5		
SiP21103DLP-26-E3	A4LL	2.6		
SiP21103DLP-28-E3	A6LL	2.8		
SiP21103DLP-285-E3	A7LL	2.85		
SiP21103DLP-30-E3	B0LL	3.0		
SiP21103DLP-33-E3	B1LL	3.3		
SiP21103DLP-50-E3	B4LL	5.0		

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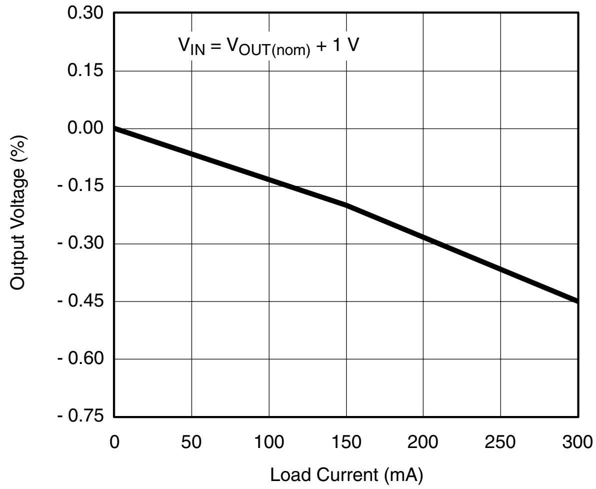
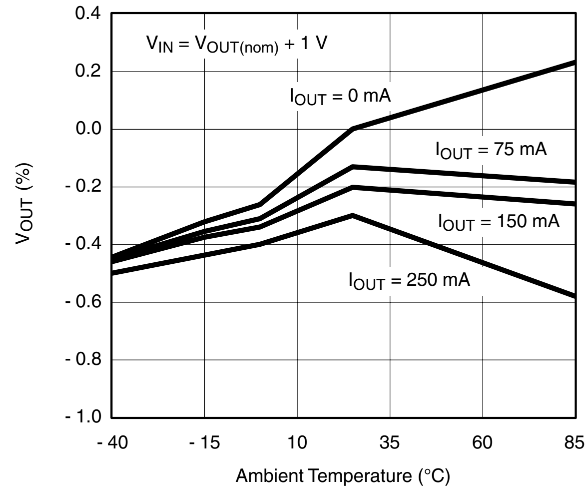
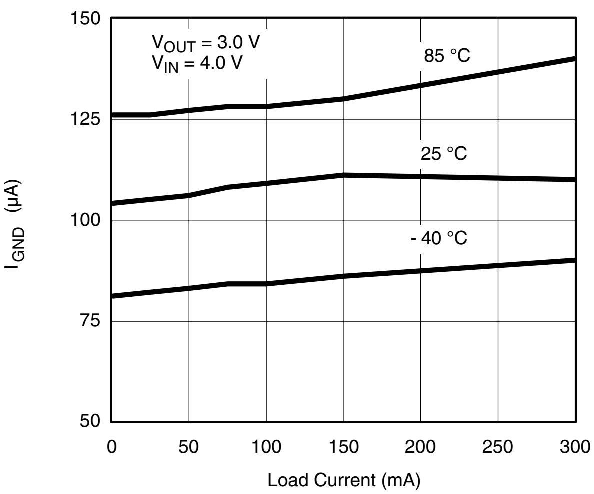
TYPICAL CHARACTERISTICS Internally Regulated, 25 °C, unless otherwise noted



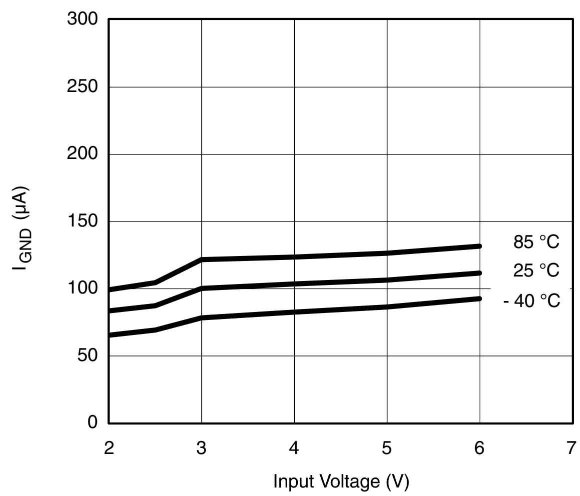
Normalized Output Voltage vs. Load Current



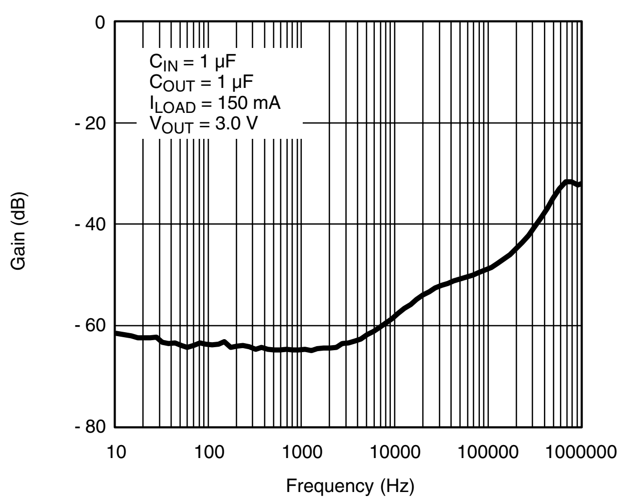
Normalized V_{OUT} vs. Temperature



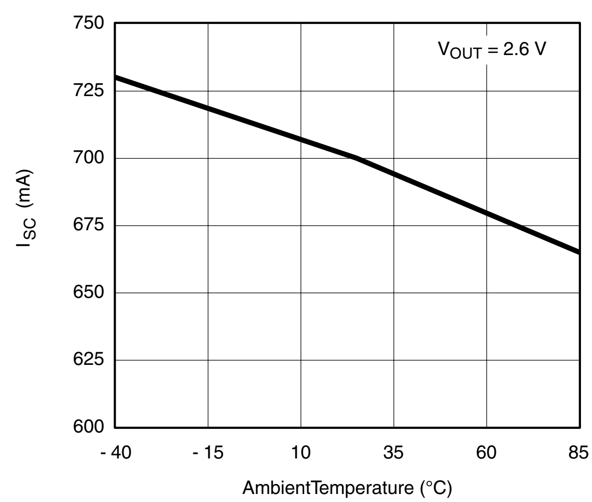
GND Current vs. Load Current



No Load GND Pin Current vs. Input Voltage

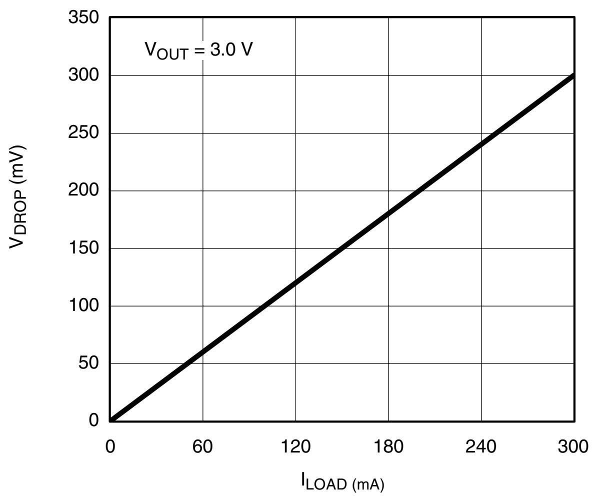


Power Supply Rejection

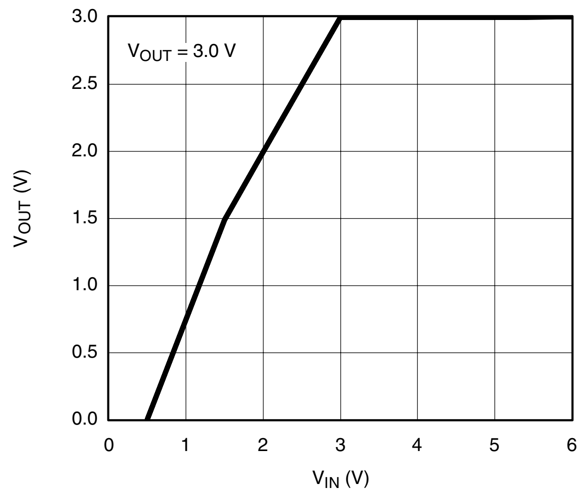


Output Short Circuit Current vs. Temperature

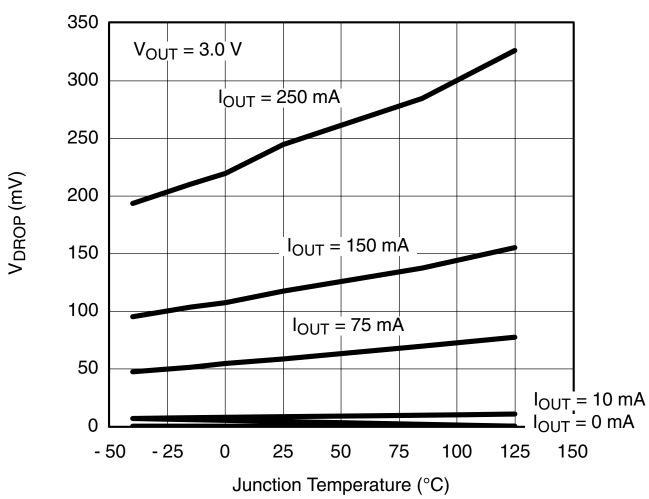
TYPICAL CHARACTERISTICS Internally Regulated, 25 °C, unless otherwise noted



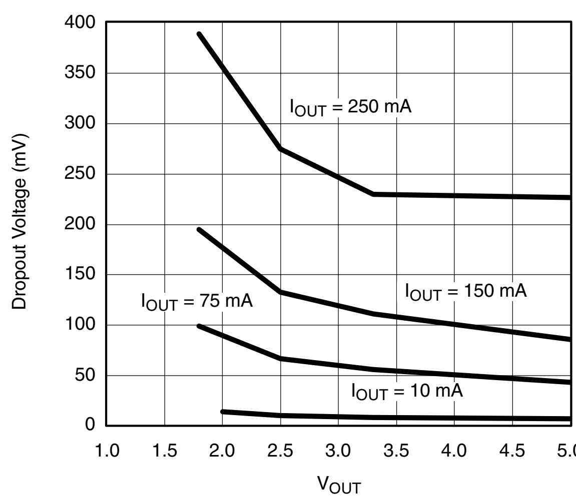
Dropout Voltage vs. Load Current



V_{IN} - V_{OUT} Transfer Characteristic

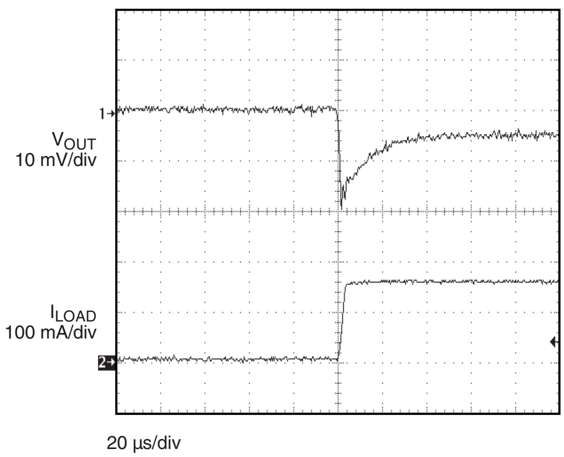


Dropout Voltage vs. Temperature



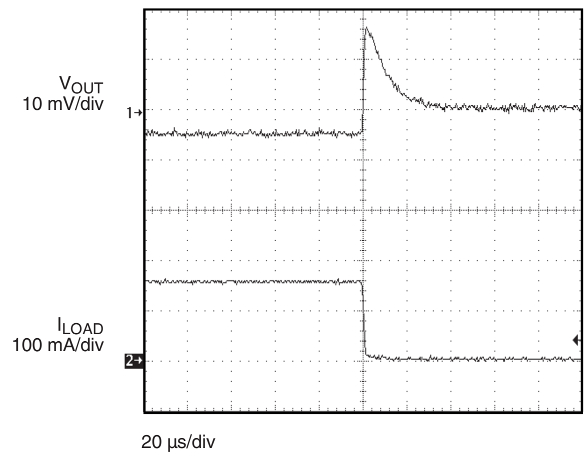
Dropout Voltage vs. V_{OUT}

TYPICAL WAVEFORMS



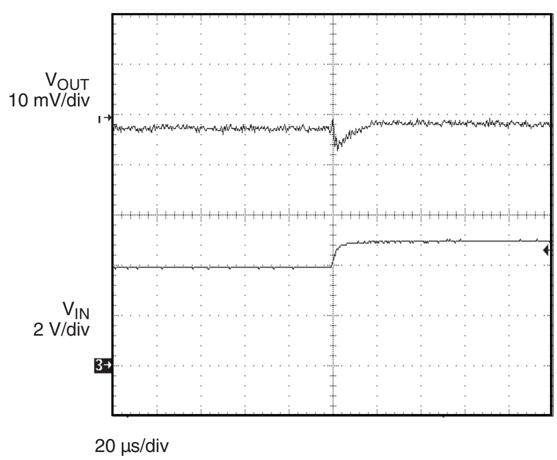
V_{OUT} = 3.0 V
C_{OUT} = 1 µF
I_{LOAD} = 1 to 150 mA
t_{rise} = 2 µs

Load Transient Response-1



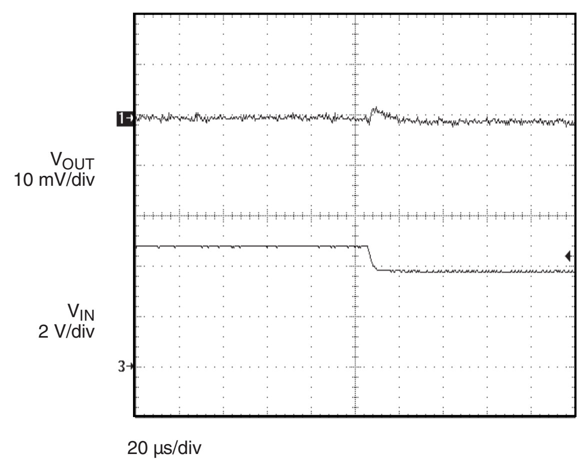
V_{OUT} = 3.0 V
C_{OUT} = 1 µF
I_{LOAD} = 150 to 1 mA
t_{fall} = 2 µs

Load Transient Response-2



V_{INSTEP} = 4 to 5 V
V_{OUT} = 3 V
C_{OUT} = 1 µF
C_{IN} = 1 µF
I_{LOAD} = 150 mA
t_{rise} = 5 µs

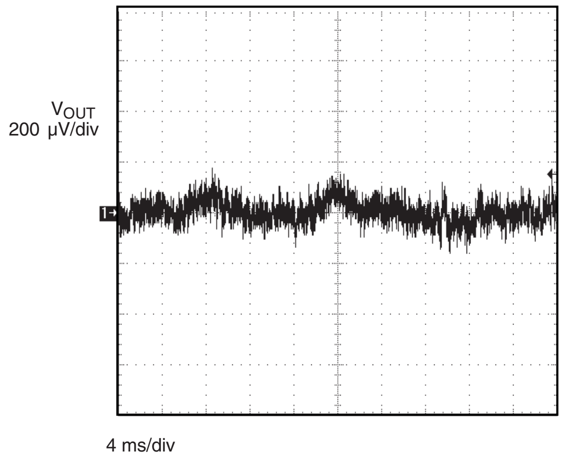
Line Transient Response-1



V_{INSTEP} = 5 to 4 V
V_{OUT} = 3 V
C_{OUT} = 1 µF
C_{IN} = 1 µF
I_{LOAD} = 150 mA
t_{fall} = 5 µs

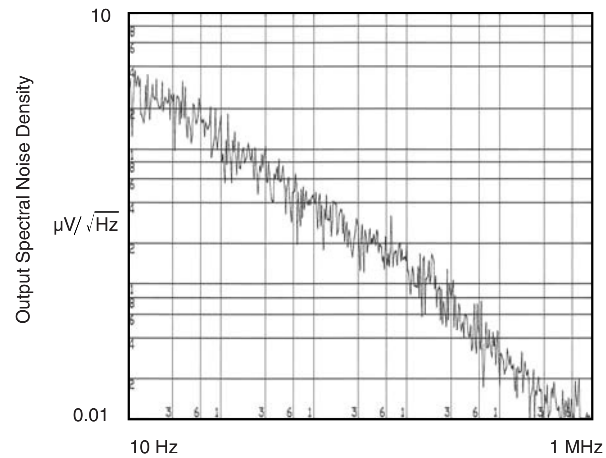
Line Transient Response-2

TYPICAL WAVEFORMS



V_{IN} = 4 V
V_{OUT} = 3 V
I_{OUT} = 150 mA
C_{NOISE} = 0.01 μF
BW = 10 Hz to 100 kHz

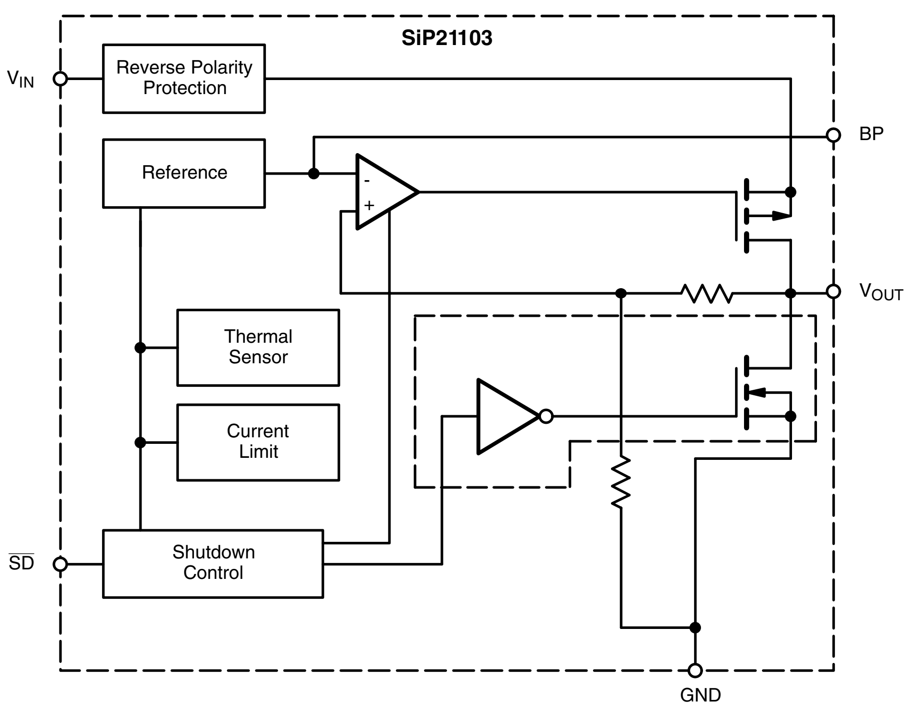
Output Noise



V_{IN} = 4 V
V_{OUT} = 3 V
I_{LOAD} = 150 mA
C_{NOISE} = 0.01 μF

Noise Spectrum

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

The SiP21103 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint MLP22-5 package. The SiP21103 can supply loads up to 250 mA. As shown in the block diagram, the circuit consists of a bandgap reference error, amplifier, P-Channel pass transistor and feedback resistor string. An external bypass capacitor connected to the BP pin reduces noise at the output. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection and thermal sensor.

Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150 °C, the device turns the P-Channel pass transistor off.

Reverse Battery Protection

The SiP21103 has a battery reverse protection circuitry that disconnects the internal circuitry when V_{IN} drops below the GND voltage. There is no current drawn in such an event. When the $\overline{SD}$ pin is hardwired to V_{IN}, the user must connect the $\overline{SD}$ pin to V_{IN} via a 100 kΩ resistor if reverse battery protection is desired. Hardwiring the $\overline{SD}$ pin directly to the V_{IN} pin is allowed when reverse battery protection is not desired.

Noise Reduction

An external 10 nF bypass capacitor at BP is used to create a low pass filter for noise reduction. The start-up time is fast, since a power-on circuit pre-charges the bypass capacitor. After the power-up sequence the pre-charge circuit is switched to standby mode in order to save current. It is therefore not recommended to use larger bypass capacitor values than 50 nF. When the circuit is used without a capacitor, stable operation is guaranteed.

Auto-Discharge

The SiP21103 V_{OUT} has an internal 100 Ω (typ.) discharge path to ground when the $\overline{SD}$ pin is low.

Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 1.5 µF at 250 mA). Since the bandwidth of the error amplifier is around 1-3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 250 mA load current, an ESR < 0.2 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.

Safe Operating Area

The ability of the SiP21103 to supply current is ultimately dependent on the junction temperature of the pass device. Junction temperature is in turn dependent on power dissipation in the pass device, the thermal resistance of the package and the circuit board, and the ambient temperature.

The power dissipation is defined as

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT}.$$

Junction temperature is defined as

$$T_J = T_A + ((P_D * (R\theta_{JC} + R\theta_{CA})).$$

To calculate the limits of performance, these equations must be rewritten.

Allowable power dissipation is calculated using the equation

$$P_D = (T_J - T_A) / (R\theta_{JC} + R\theta_{CA})$$

While allowable output current is calculated using the equation

$$I_{OUT} = (T_J - T_A) / (R\theta_{JC} + R\theta_{CA}) * (V_{IN} - V_{OUT}).$$

Ratings of the SiP21103 that must be observed are

T_{Jmax} = 125 °C, T_{Amax} = 85 °C, $(V_{IN} - V_{OUT})_{max}$ = 5.3 V, $R\theta_{JC}$ = 8 °C/W.

The value of $R\theta_{CA}$ is dependent on the PC board used. The value of $R\theta_{CA}$ for the board used in device characterization is approximately 57 °C/W.

Figure 1 shows the performance limits graphically for the SiP21103 mounted on the circuit board used for thermal characterization.

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