

SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

description

These octal bus transceivers provide for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing. The 'ABT620 devices provide inverted data at the outputs.

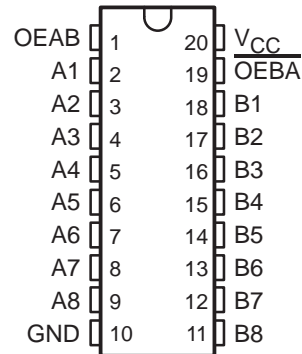
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 total) remain at their last states. In this way, each output reinforces its input in this configuration.

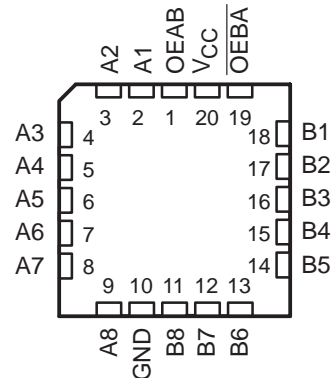
To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT620 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT620 is characterized for operation from -40°C to 85°C .

SN54ABT620 . . . J PACKAGE
SN74ABT620 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT620 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II^B is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

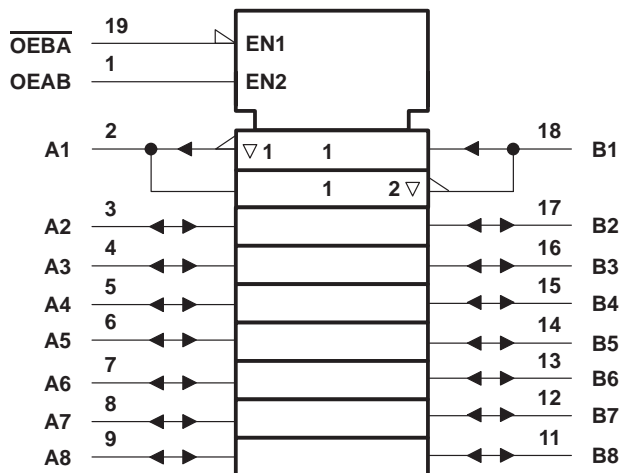
SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

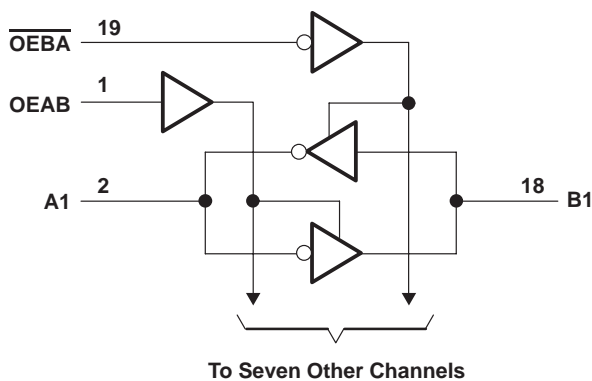
FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	\bar{B} data to A bus
L	H	\bar{B} data to A bus, A data to B bus
H	L	Isolation
H	H	\bar{A} data to B bus

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT620	96 mA
SN74ABT620	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

recommended operating conditions (see Note 3)

		SN54ABT620		SN74ABT620		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused pins (control or I/O) of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT620		SN74ABT620		UNIT			
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX				
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V			
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V			
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3					
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2							
I _{OH} = -32 mA		2*					2						
V _{OL}	V _{CC} = 4.5 V		I _{OL} = 48 mA			0.55		0.55		V			
			I _{OL} = 64 mA			0.55*			0.55				
V _{hys}			100							mV			
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND	±1			±1		±1		μA			
	A or B ports		±100			±100		±100					
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V		50			50		50		μA			
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V		-50			-50		-50		μA			
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA			
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high			50		50		μA			
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA			
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			5 250		250		250		μA	
			Outputs low			24 30			30		30		mA
			Outputs disabled			0.5 250			250		250		μA
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled			1.5		1.5		1.5		mA	
			Outputs disabled			0.05			0.05		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5				
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4							pF		
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		7							pF		

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT620, SN74ABT620
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C		SN54ABT620		SN74ABT620		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4.1	1		1	4.8	ns
t_{PHL}			1	4.3	1		1	4.8	
t_{PZH}	\overline{OEBA}	A	1.3	4.6	1.3		1.3	5.5	ns
t_{PZL}			1	6.1	1		1	7.1	
t_{PHZ}	\overline{OEBA}	A	2	6.3	2		2	7	ns
t_{PLZ}			1.4	5.4	1.4		1.4	5.8	
t_{PZH}	OEAB	B	1.6	6.2	1.6		1.6	6.8	ns
t_{PZL}			2	5.9	2		2	6.4	
t_{PHZ}	OEAB	B	1.2	5.6	1.2		1.2	6.5	ns
t_{PLZ}			1.1	4.7	1.1		1.1	5.6	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

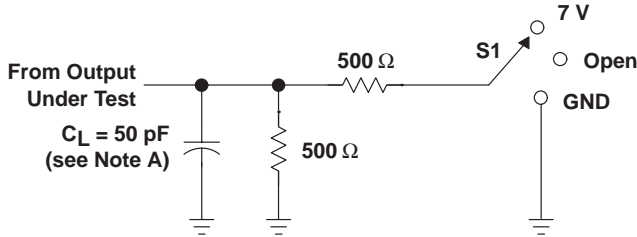


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

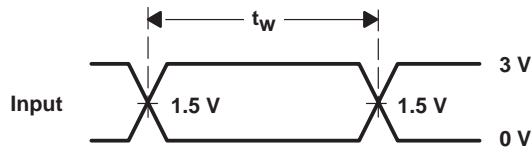
SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

PARAMETER MEASUREMENT INFORMATION

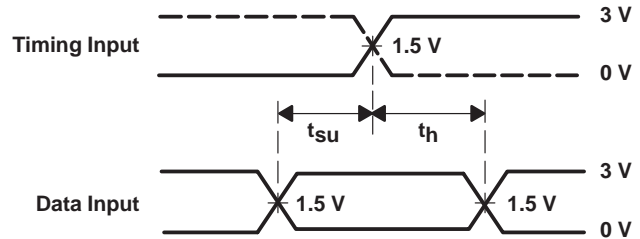


LOAD CIRCUIT

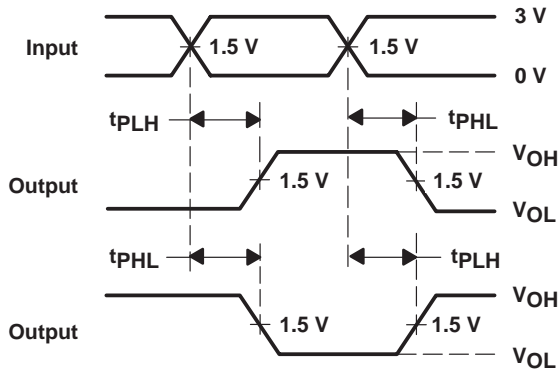
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



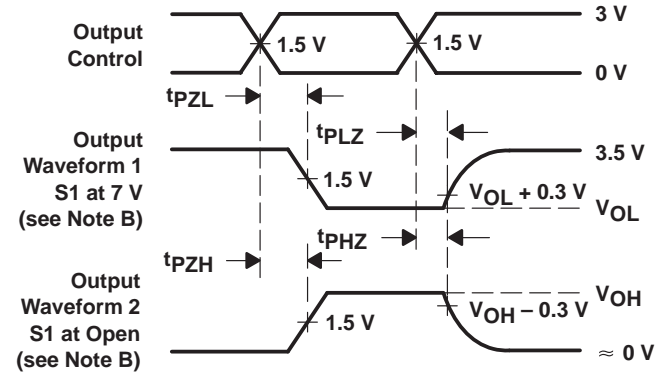
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [SAMPLES](#)
| [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74ABT620, Octal Bus Transceivers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ABT620
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-32/64
No. of Outputs	8
Logic	Inv
Static Current	15.12
tpd max (ns)	4.8

FEATURES

[▲ Back to Top](#)

- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (-32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

EPIC-IIB is a trademark of Texas Instruments Incorporated.

DESCRIPTION

[▲ Back to Top](#)

These octal bus transceivers provide for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing. The 'ABT620 devices provide inverted data at the outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (OEAB and OEBA\) inputs.

The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and OEBA\ . When both OEAB and OEBA\ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 total) remain at their last states. In this way, each output reinforces its input in this configuration.

To ensure the high-impedance state during power up or power down, OEBA\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT620 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT620 is characterized for operation from -40°C to 85°C .

TECHNICAL DOCUMENTS[▲Back to Top](#)

To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET[▲Back to Top](#)

Full datasheet in Acrobat PDF: [sn74abt620.pdf](#) (117 KB,Rev.D) (Updated: 04/08/1998)

APPLICATION NOTES[▲Back to Top](#)

View Application Notes for [Digital Logic](#)

- [Advanced BiCMOS Technology \(ABT\) Logic Characterization Information \(Rev. B\)](#) (SCBA008B - Updated: 06/01/1997)
- [Advanced BiCMOS Technology \(ABT\) Logic Enables Optimal System Design \(Rev. A\)](#) (SCBA001A - Updated: 03/01/1997)
- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices \(Rev. A\)](#) (SCBA006A - Updated: 12/01/1996)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)
- [Power-Up 3-State \(PU3S\) Circuits in TI Standard Logic Devices](#) (SZZA033 - Updated: 05/10/2002)
- [Quad Flatpack No-Lead Logic Packages \(Rev. A\)](#) (SCBA017A - Updated: 09/10/2002)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

RELATED DOCUMENTS[▲Back to Top](#)

View Related Documentation for [Digital Logic](#)

- [Advanced Bus Interface Logic Selection Guide](#) (SCYT126, 453 KB - Updated: 01/09/2001)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES[▲Back to Top](#)

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ABT620DBR	SSOP (DB)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT620DW	SOP (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT620N	PDIP (N)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG[▲Back to Top](#)

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74ABT620DBLE	OBSOLETE	SSOP (DB) 20	-40 TO 85	View Contents	1KU		N/A*		Not Available			
SN74ABT620DBR	ACTIVE	SSOP (DB) 20	-40 TO 85	View Contents	1KU 1.47	2000	N/A*	5568 07 Oct	4 WKS			
								>10k 21 Oct				
SN74ABT620DW	ACTIVE	SOP (DW) 20	-40 TO 85	View Contents	1KU 1.47	25	2100	5568 04 Oct	4 WKS			
								>10k 18 Oct				
SN74ABT620DWR	ACTIVE	SOP (DW) 20	-40 TO 85	View Contents	1KU 1.50	2000	N/A*	497 25 Sep	4 WKS			
								5568 04 Oct				
								>10k 18 Oct				
SN74ABT620N	ACTIVE	PDIP (N) 20	-40 TO 85	View Contents	1KU 1.47	20	N/A*	1240 03 Oct	4 WKS			
								5564 07 Oct				
								>10k 21 Oct				
SN74ABT620NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 1.47	2000	N/A*	310 23 Sep	4 WKS			
								5575 14 Oct				
								>10k 21 Oct				

Table Data Updated on: 9/26/2002