Comlinear
A National Semiconductor Company

Low-Cost, Low-Power, 110MHz Op Amp with Disable

CLC405

APPLICATIONS:
- Desktop Video Systems
- Multiplexers
- Video Distribution
- Flash A/D Driver
- High-Speed Switch/Driver
- High-Source Impedance Applications
- Peak Detector Circuits
- Professional Video Processing
- High Resolution Monitors

FEATURES:
- Low-cost
- Very low input bias current: 100nA
- High input impedance: 6MΩ
- 110MHz -3dB bandwidth (A_V = +2)
- Low power: I_{CC} = 3.5mA
- Ultra-fast enable/disable times
- High output current: 60mA

3

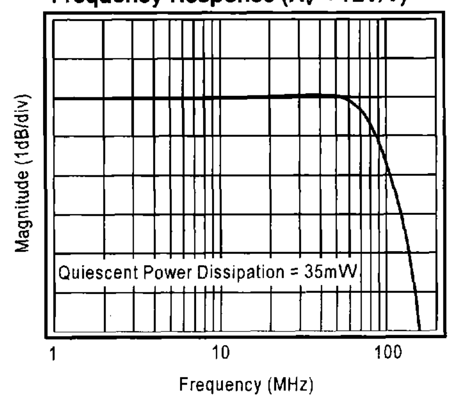
DESCRIPTION

The CLC405 is a low-cost, wideband (110MHz) op amp featuring a TTL-compatible disable which quickly switches off in 18ns and back on in 40ns. While disabled, the CLC405 has a very high input/output impedance and its total power consumption drops to a mere 8mW. When enabled, the CLC405 consumes only 35mW and can source or sink an output current of 60mA. These features make the CLC405 a versatile, high-speed solution for demanding applications that are sensitive to both power and cost.

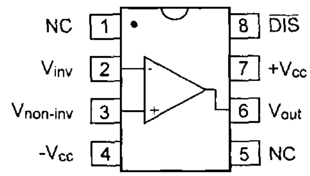
Utilizing Comlinear's proven architectures, this current feedback amplifier surpasses the performance of alternative solutions and sets new standards for low power at a low price. This power-conserving op amp achieves low distortion with -72dBc and -70dBc for second and third harmonics respectively. Many high source impedance applications will benefit from the CLC405's 6MΩ input impedance. And finally, designers will have a bipolar part with an exceptionally low 100nA non-inverting bias current.

With 0.1dB flatness to 50MHz and low differential gain and phase errors, the CLC405 is an ideal part for professional video processing and distribution. However, the 110MHz -3dB bandwidth (Av = +2) coupled with a 350V/μs slew rate also make the CLC405 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems.

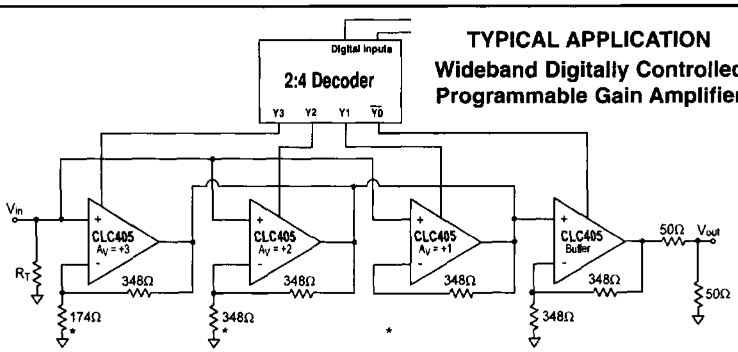
Frequency Response (A_V = +2V/V)



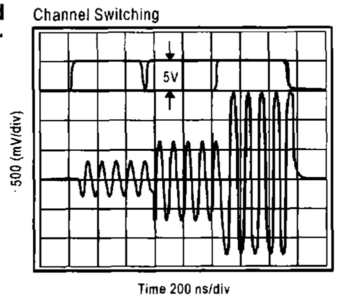
PINOUT
DIP & SOIC



TYPICAL APPLICATION
Wideband Digitally Controlled Programmable Gain Amplifier



Channel Switching



*NOTE: Selectable gains can be changed by using different R_g resistors

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CLC405 Electrical Characteristics (A_V = +2, R_f = 348Ω; V_{cc} = ±5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC405AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	110	75	50	45	MHz	B
	V_{out} < 5.0V_{pp}	42	31	27	26	MHz	1
-3dB bandwidth A_V = +1	V_{out} < 0.5V_{pp} (R_f = 2K)	135				MHz	
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	50	15			MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0	0.6	0.8	1.0	dB	B
rolloff	<30MHz	0.05	0.3	0.4	0.5	dB	B
linear phase deviation	<20MHz	0.3	0.6	0.7	0.7	deg	
differential gain	NTSC, R_L=150Ω	0.01	0.03	0.04	0.05	%	
	NTSC, R_L=150Ω (Note 2)	0.01				%	2
differential phase	NTSC, R_L=150Ω	0.25	0.4	0.5	0.55	deg	
	NTSC, R_L=150Ω (Note 2)	0.08				deg	2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	5	7.5	8.2	8.4	ns	
settling time to 0.05%	2V step	18	27	36	39	ns	
overshoot	2V step	3	12	12	12	%	
slew rate A_V = +2	2V step	350	260	225	215	V/µs	
A_V = -1	1V step	650				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz/10MHz	-72/-52	-46	-45	-44	dBc	B, C
3rd harmonic distortion	2V_{pp}, 1MHz/10MHz	-70/-57	-50	-47	-46	dBc	B, C
equivalent input noise							
non-inverting voltage	>1MHz	5	6.3	6.6	6.7	nV/√Hz	
inverting current	>1MHz	12	15	16	17	pA/√Hz	
non-inverting current	>1MHz	3	3.8	4	4.2	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1	5	7	8	mV	A
average drift		30	50		50	µV/°C	
input bias current	non-inverting	100	500	700	1100	nA	A
average drift		3		8	11	nA/°C	
input bias current	inverting	1	5	6	8	µA	A
average drift		17		40	45	nA/°C	
power supply rejection ratio	DC	52	47	46	45	dB	B
common-mode rejection ratio	DC	50	45	44	43	dB	
supply current	R_L= ∞	3.5	4.0	4.1	4.4	mA	A
disabled	R_L= ∞	0.8	0.9	0.95	1	mA	A
SWITCHING PERFORMANCE							
turn on time		40	55	58	58	ns	
turn off time	to >50dB attn. @ 10MHz	18	26	30	32	ns	
off isolation	10MHz	59	55	55	55	dB	
high input voltage	V_{IH}		2	2	2	V	
low input voltage	V_{IL}		0.8	0.8	0.8	V	
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6	3	2.4	1	MΩ	
input resistance	inverting	182				Ω	
input capacitance	non-inverting	1	2	2	2	pF	
common mode input range		±2.2	1.8	1.7	1.5	V	
output voltage range	R_L = 100Ω	+ 3.5,-2.8	+3.1,-2.7	+2.9,-2.6	+2.4,-1.6	V	
output voltage range	R_L = ∞	+4.0,-3.3	+3.9,-3.2	+3.8,-3.1	+3.7,-2.8	V	
output current		60	44	38	20	mA	
output resistance, closed loop		0.06	0.2	0.25	0.4	Ω	

Recommended gain range ±1 to ±40 V/V

Absolute Maximum Ratings

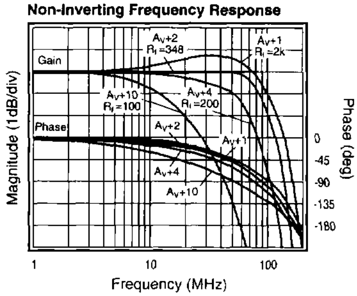
supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

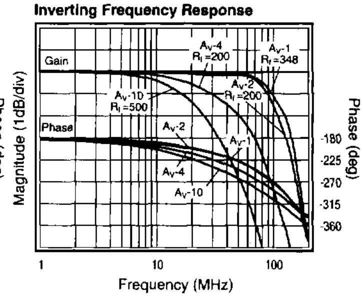
1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
2) An 825Ω pull-down resistor is connected between V_o and $-V_{cc}$.
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C. LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.
C) Guaranteed at 10MHz.

CLC405 Typical Performance Characteristics (A_V = +2, R_f = 348Ω: V_{cc} = + 5V, R_L = 100Ω unless specified)

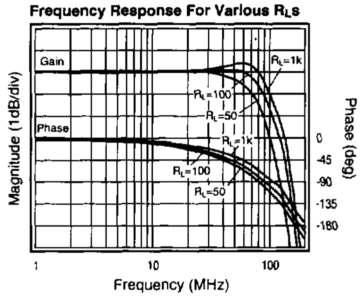
Non-Inverting Frequency Response



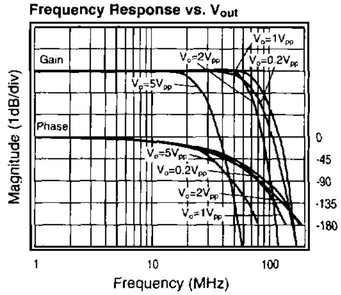
Inverting Frequency Response



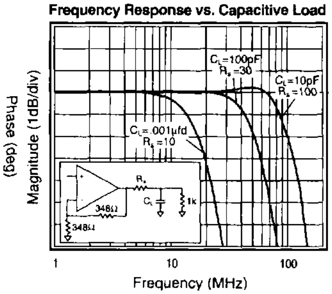
Frequency Response For Various R_Ls



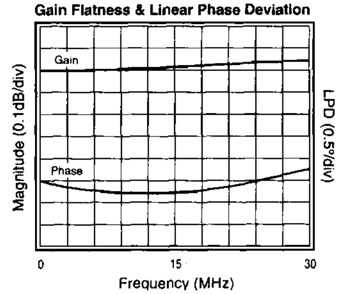
Frequency Response vs. V_{out}



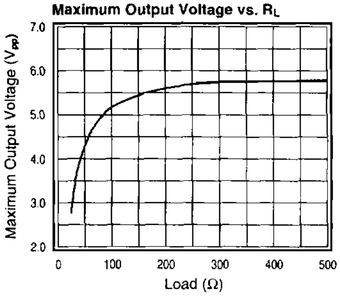
Frequency Response vs. Capacitive Load



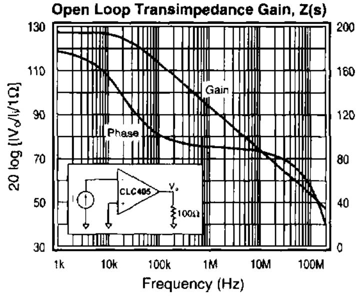
Gain Flatness & Linear Phase Deviation



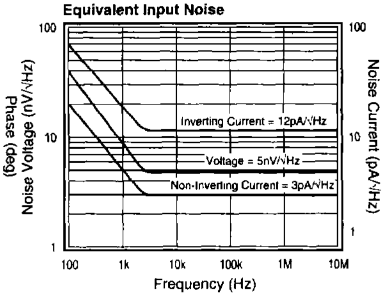
Maximum Output Voltage vs. R_L



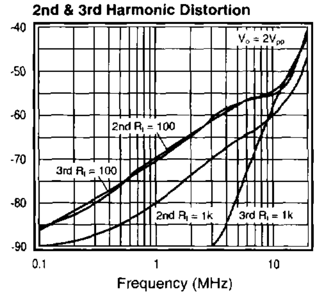
Open Loop Transimpedance Gain, Z(s)



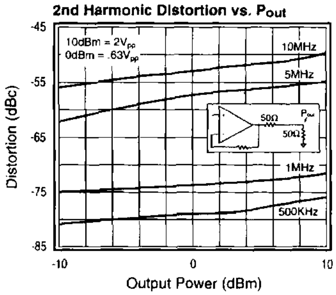
Equivalent Input Noise



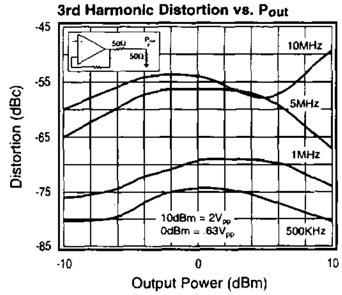
2nd & 3rd Harmonic Distortion



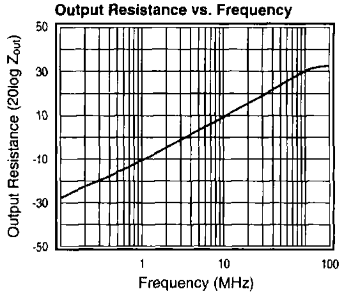
2nd Harmonic Distortion vs. P_{out}



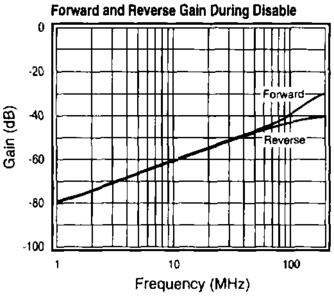
3rd Harmonic Distortion vs. P_{out}



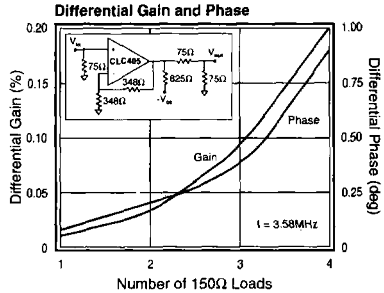
Output Resistance vs. Frequency



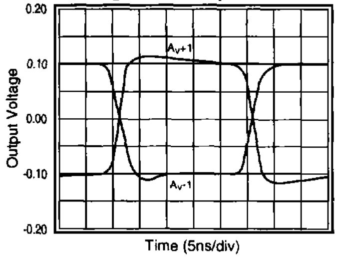
Forward and Reverse Gain During Disable



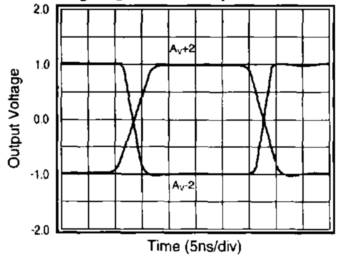
Differential Gain and Phase



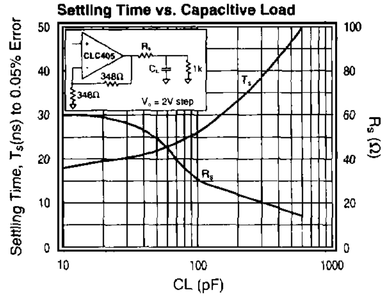
Small Signal Pulse Response



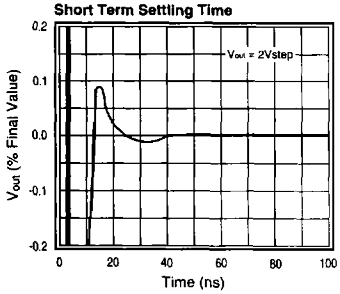
Large Signal Pulse Response



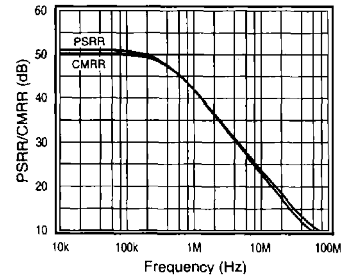
Settling Time vs. Capacitive Load



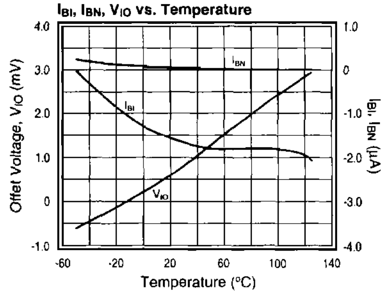
Short Term Settling Time



PSRR and CMRR



I_{BI}, I_{BN}, V_{IO} vs. Temperature



CLC405 OPERATION

Feedback Resistor

The feedback resistor, R_f, determines the loop gain and frequency response for a current feedback amplifier. Unless otherwise stated, the performance plots and data sheet specify CLC405 operation with R_f of 348Ω at a gain of +2V/V. Optimize frequency response for different gains by changing R_f. Decrease R_f to peak frequency response and extend bandwidth. Increase R_f to roll off of the frequency response and decrease bandwidth. Use a 2kΩ R_f for unity gain, voltage follower circuits.

Use application note OA-13 to optimize your R_f selection. The equations in this note are a good starting point for selecting R_f. The value for the inverting input impedance for OA-13 is approximately 182Ω.

Enable/Disable Operation Using ±5V Supplies

The CLC405 has a TTL & CMOS logic compatible disable function. Apply a logic low (i.e. < 0.8V) to pin 8, and the CLC405 is guaranteed disabled across its temperature range. Apply a logic high to pin 8, (i.e. > 2.0V) and the CLC405 is guaranteed enabled. Voltage, not current, at pin 8 determines the enable/disable state of the CLC405.

Disable the CLC405 and its inputs and output become high impedances. While disabled, the CLC405's quiescent power drops to 8mW.

Use the CLC405's disable to create analog switches or multiplexers. Implement a single analog switch with one CLC405 positioned between an input and output. Create an analog multiplexer with several CLC405s. Tie the outputs together and put a different signal on each CLC405 input.

Operate the CLC405 without connecting pin 8. An internal 20kΩ pull-up resistor guarantees the CLC405 is enabled when pin 8 is floating.

Enable/Disable Operation for Single or Unbalanced Supply Operation

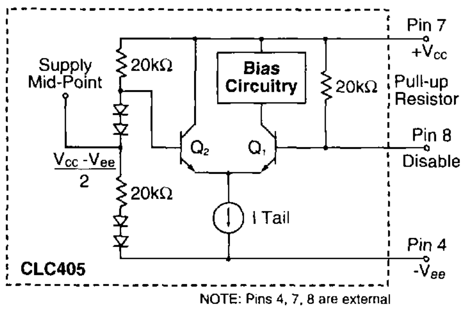


Figure 1

Figure 1 illustrates the internal enable/disable operation of the CLC405. When pin 8 is left floating or is tied to $+V_{cc}$, Q1 is on and pulls tail current through the CLC405 bias circuitry. When pin 8 is less than 0.8V above the supply midpoint, Q1 stops tail current from flowing in the CLC405 circuitry. The CLC405 is now disabled.

Disable Limitations

The feedback resistor, R_f, limits off isolation in inverting gain configurations. Do not apply voltages greater than $+V_{cc}$ or less than $-V_{ee}$ to pin 8 or any other pin.

Input - Bias Current, Impedances, and Source Termination Considerations

The CLC405 has:

- a 6MΩ non-inverting input impedance.
- a 100nA non-inverting input bias current.

If a large source impedance application is considered, remove all parasitic capacitance around the non-inverting input and source traces. Parasitic capacitances near the input and source act as a low-pass filter and reduce bandwidth.

Current feedback op amps have uncorrelated input bias currents. These uncorrelated bias currents prevent source impedance matching on each input from canceling offsets. Refer to application note OA-07 of the data book to find specific circuits to correct DC offsets.

Layout Considerations

Whenever questions about layout arise, USE THE EVALUATION BOARD AS A TEMPLATE.

Use the 730013 and 730027 evaluation boards for the DIP and SOIC respectively. These board layouts were optimized to produce the typical performance of the CLC405 shown in the data sheet. To reduce parasitic capacitances, the ground plane was removed near pins 2, 3, and 6. To reduce series inductance, trace lengths of components and nodes were minimized.

Parasitics on traces degrade performance. Minimize coupling from traces to both power and ground planes. Use low inductive resistors for leaded components.

Do not use dip sockets for the CLC405 DIP amplifiers. These sockets can peak the frequency domain response or create overshoot in the time domain response. Use flush-mount socket pins when socketing is necessary. The 730013 circuit board device holes are sized for Cambion P/N 450-2598 socket pins or their functional equivalent.

Insert the back matching resistor (R_{out}) shown in Figure 2 when driving coaxial cable or a capacitive load. Use the plot in the typical performance section labeled "Settling Time vs. Capacitive Load" to determine the optimum resistor value for $\mathbf{R_{out}}$ for different capacitive loads. This optimal resistance improves settling time for pulse-type applications and increases stability.

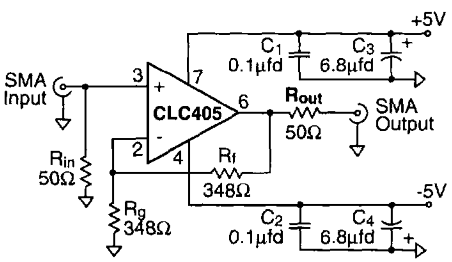
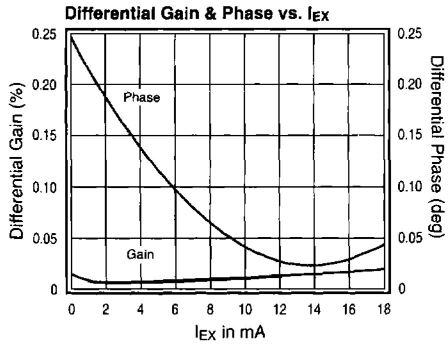


Figure 2

Use power-supply bypassing capacitors when operating this amplifier. Choose quality 0.1μF ceramics for C_1 and C_2. Choose quality 6.8μF tantalum capacitors for C_3 and C_4. Place the 0.1μF capacitors within 0.1 inches from the power pins. Place the 6.8μF capacitors within 3/4 inches from the power pins.

Video Performance vs. I_{EX}

Improve the video performance of the CLC405 by drawing extra current from the amplifier output stage. Using a single external resistor as shown in Figure 3, you can adjust the differential phase. Video performance vs. I_{EX} is illustrated below in Graph 1. This graph represents positive video performance with negative synchronization pulses.



Graph1

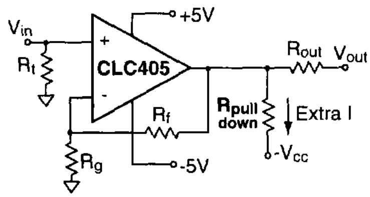


Figure 3

The value for R_{pd} in Figure 3 is determined by :

$$R_{pd} = \frac{5}{I_{EX}}$$

at ±5V supplies.

Wideband Digital PGA

As shown on the front page, the CLC405 is easily configured as a digitally controlled programmable gain amplifier. Make a PGA by configuring several amplifiers at required gains. Keep R_f near 348Ω and change R_g for each different gain. Use a TTL decoder that has enough outputs to control the selection of different gains and the buffer stage. Connect the buffer stage like the buffer of the front page. The buffer isolates each gain stage from the load and can produce a gain of zero for a gain selection of zero. Use of an inverter (7404) on the buffer disable pin to keep the buffer operational at all gains except zero. Or float the buffer disable pin for a continuous enable state.

Amplitude Equalization

Sending signals over coaxial cable greater than 50 meters in length will attenuate high frequency signal components. Equalizers restore the attenuated components of this signal. The circuit in Figure 4, is an op amp equalizer. The RC networks peak the response of the CLC405 at higher frequencies. This peaking restores cable-attenuated frequencies. Graph 2 shows how the equalizer actually restored a digital word through 150 meters of coaxial cable.

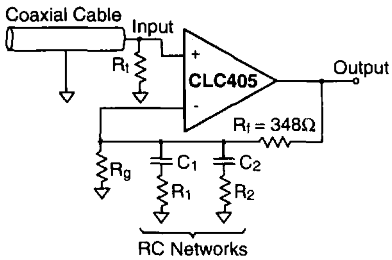
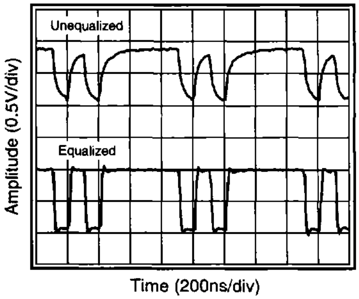


Figure 4

Digital Word Amplitude Equalization



Graph 2

The values used to produce Graph 2 are:

$R_g = 348\Omega$ $C_1 = 470pF$ $C_2 = 70pF$

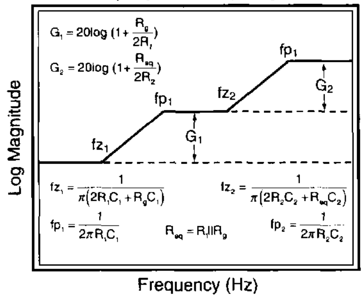
$R_1 = 450\Omega$ $R_2 = 90\Omega$

Amplitude Equalizer

Place the first zero (fz_1) at some low frequency (540 khz for Graph 2). R_1 & C_1 produce a pole (fp_1 @ 750khz) that cancels fz_1. Place a second zero at a higher frequency (fz_2 @ 12Mhz). R_2 & C_2 provide a canceling pole (of fp_2 = 25Mhz).

Graph 3 shows the closed loop response of the op amp equalizer with equations for the poles, zeros, and gains.

Closed Loop Equalizer Frequency Response



Graph 3

Note: For very-high frequency equalization, use a higher bandwidth part (i.e. CLC44X)

Package Thermal Resistance

Package	θjc	θjA
Plastic (AJP)	75°/W	125°/W
Surface Mount (AJE)	130°/W	150°/W
CerDip	65°/W	155°/W

Ordering Information

Model	Temperature Range	Description
CLC405AJP	-40°C to +85°C	8-pin PDIP
CLC405AJE	-40°C to +85°C	8-pin SOIC
CLC405AIB*	-40°C to +85°C	8-pin CerDIP
CLC405ALC	-55°C to +125°C	dice
CLC405SMD*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC405AMC	-55°C to +125°C	dice, MIL-STD-883

*See CLC405 MIL-883 Data Sheet for Specifications

