HARRIS SEMICONDUCTOR

CD74LPT646, CD74LPT652

December 1996

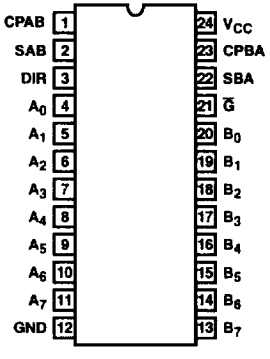
Fast CMOS 3.3V 8-Bit Registered Transceivers

Features

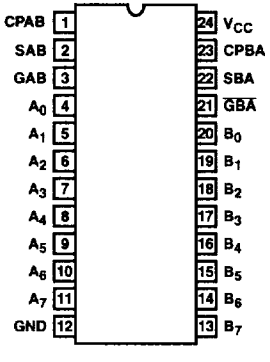
- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Pinout

CD74FCT646
(QSOP, SOIC)
TOP VIEW



CD74LPT652
(QSOP, SOIC)
TOP VIEW



Description

The CD74LPT646 and CD74LPT652 are designed with a bus transceiver with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The CD74LPT652 utilizes GAB and $\overline{GBA}$ signals to control the transceiver functions. The CD74LPT646 utilizes the enable control ($\overline{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74LPT646 and CD74LPT652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

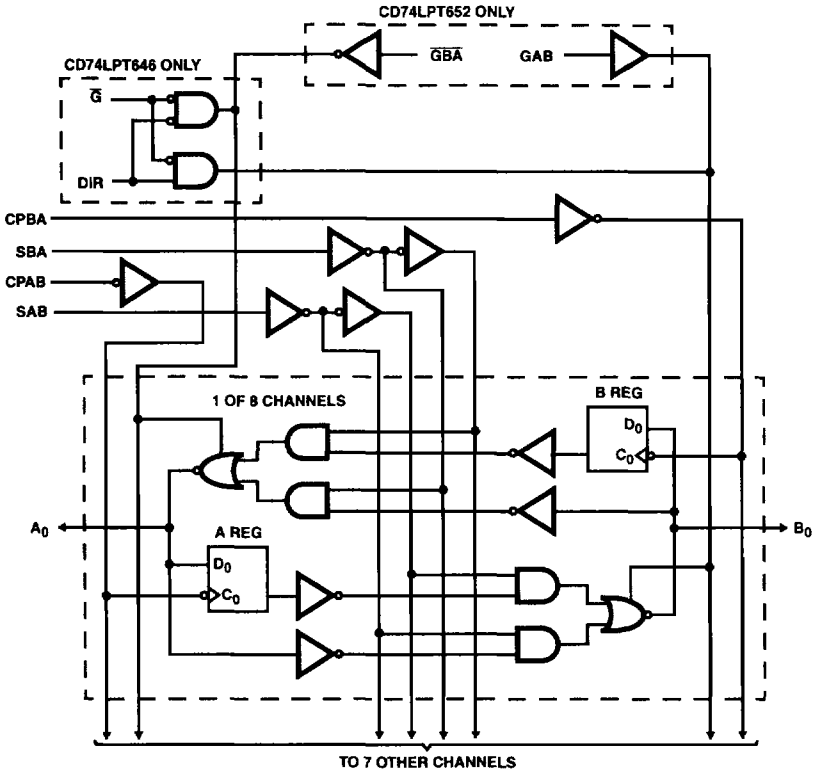
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74LPT646QM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT646AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT646CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT646M	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT646AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT646CM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT652QM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT652AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT652CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT652M	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT652AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT652CM	-40 to 85	24 Ld SOIC	M24.3-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

File Number 4257

Functional Block Diagram



TRUTH TABLE (CD74LPT646)

FUNCTION/OPERATION	INPUTS						DATA I/O (NOTE 1)	
	$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0 - A_7	B_0 - B_7
Isolation Store A and B Data	H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input
Real Time B Data to A Bus Stored B Data to A Bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real Time A Data to B Bus Stored A Data to B Bus	L L	H H	X H or L	X X	L H	X X	Input	Output

TRUTH TABLE (CD74LPT652)

FUNCTION/OPERATION	INPUTS						(NOTES 1, 2) DATA I/O	
	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_0 - A_7	B_0 - B_7
Isolation Store A and B Data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B Store A in Both Registers	X H	H H	↑ ↑	H or L ↑	X X (Note 2)	X X	Input Input	Unspecified Output (Note 1)

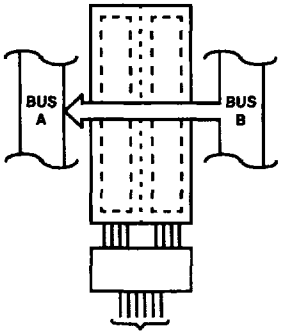
TRUTH TABLE (CD74LPT652) **(Continued)**

FUNCTION/OPERATION	INPUTS						(NOTES 1, 2) DATA I/O	
	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_0 - A_7	B_0 - B_7
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified	Input
Store B in Both Registers	L	L	↑	↑	X	X (Note 2)	Output (Note 1)	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

NOTES:

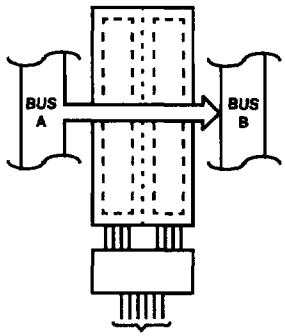
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR for the CD74LPT646 type and GAB or $\overline{GBA}$ for CD74LPT652 type inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select Control = L: clocks can occur simultaneously.
   Select Control = H: clocks must be staggered in order to load both registers.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
↑= LOW-to-HIGH transition



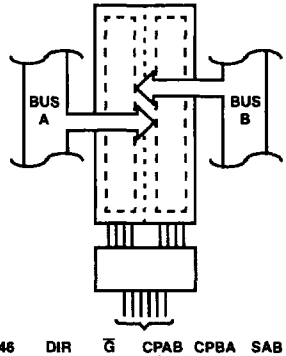
CD74LPT646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



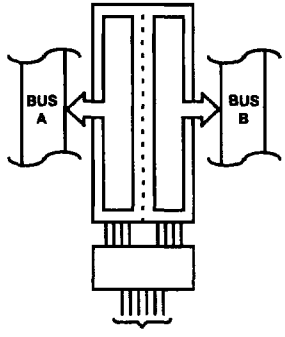
CD74LPT646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



CD74LPT646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

FIGURE 3. STORAGE FROM A AND/OR B



CD74LPT646 (NOTE 3)	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

3. Cannot transfer data to A bus and B bus simultaneously.

Pin Descriptions

PIN NAME	DESCRIPTION
A_0 - A_7	Data Register A Inputs, Data Register B Outputs
B_0 - B_7	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (CD74LPT646)
GAB, $\overline{GBA}$	Output Enable Inputs (CD74LPT652)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = V_{CC} - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{G}$ = DIR = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply *Current (Note 14)*	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND 8 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

Switching Specifications Over Operating Range (NOTE 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPTxxx (NOTE 17) MIN	CD74LPTxxx MAX	CD74LPTxxxA (NOTE 17) MIN	CD74LPTxxxA MAX	CD74LPTxxxC (NOTE 17) MIN	CD74LPTxxxC MAX	UNITS
CD74LPT646									
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	ns
Output Enable Time $\overline{G}$, DIR to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	ns
Output Disable Time $\overline{G}$, DIR to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}		2.0	9.5	2.0	7.7	1.5	6.2	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW	t_W		6.0	-	5.0	-	5.0	-	ns

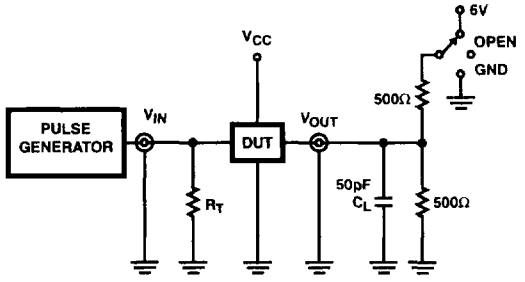
Switching Specifications Over Operating Range (NOTE 15) **(Continued)**

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPTxxx (NOTE 17) MIN	CD74LPTxxx MAX	CD74LPTxxxA (NOTE 17) MIN	CD74LPTxxxA MAX	CD74LPTxxxC (NOTE 17) MIN	CD74LPTxxxC MAX	UNITS
CD74LPT652									
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	ns
Output Enable Time $\overline{GBA}$, GAB to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	ns
Output Disable Time $\overline{GBA}$, GAB to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}		2.0	9.5	2.0	7.7	1.5	6.2	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW	t_W		6.0	-	5.0	-	5.0	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (N_{CP} f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

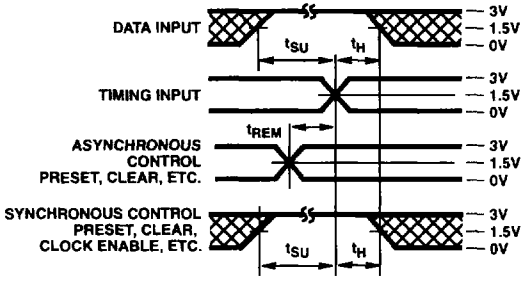


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

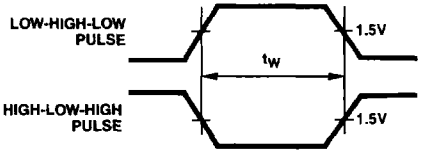


FIGURE 7. PULSE WIDTH

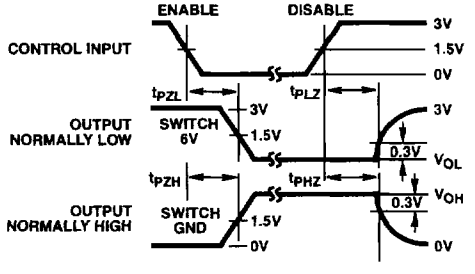


FIGURE 8. ENABLE AND DISABLE TIMING

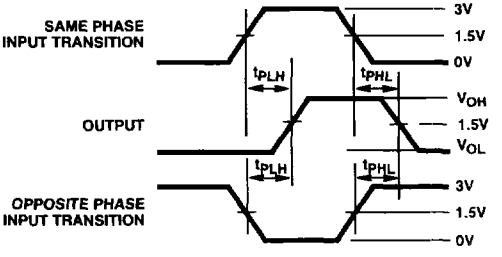


FIGURE 9. PROPAGATION DELAY