Integrated Circuit Systems, Inc.

ICS87604I

LOW VOLTAGE/LOW SKEW, 1:4 PCI/PCI-X ZERO DELAY CLOCK GENERATOR

GENERAL DESCRIPTION

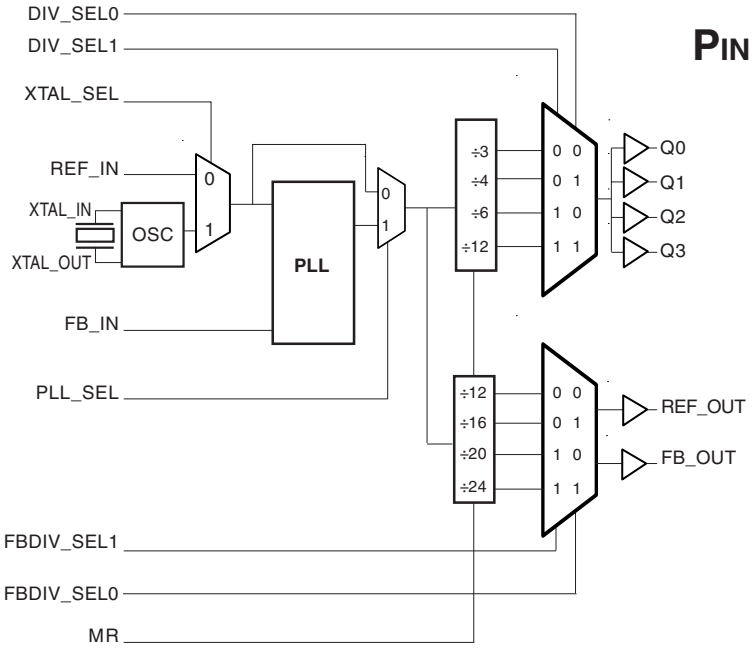
The ICS87604I is a 1:4 PCI/PCI-X Clock Generator and a member of the HiPerClockS™ family of high performance clock solutions from ICS. The ICS87604I has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels. The ICS87604I has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with "zero delay". The PLL's VCO has an operating range of 250MHz-500MHz, allowing this device to be used in a variety of general purpose clocking applications. For PCI/PCI-X applications in particular, the VCO frequency should be set to 400MHz. This can be accomplished by supplying 33.33MHz, 25MHz, 20MHz, or 16.66MHz on the reference clock or crystal input and by selecting ÷12, ÷16, ÷20, or ÷24, respectively as the feedback divide value. The divider on the output bank can then be configured to generate 33.33MHz (÷12), 66.66MHz (÷6), 100MHz (÷4), or 133.33MHz (÷3).

The ICS87604I is characterized to operate with its core supply at 3.3V and the bank supply at 3.3V or 2.5V. The ICS87604I is packaged in a small 6.1mm x 9.7mm TSSOP body, making it ideal for use in space-constrained applications.

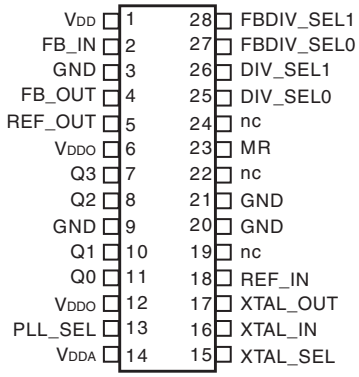
FEATURES

- Fully integrated PLL
- 4 LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_IN clock input
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 38MHz
- Maximum REF_IN input frequency: 41.67MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz
- Separate feedback control for generating PCI / PCI-X frequencies from a 16.66MHz or 20MHz crystal, or 25MHz or 33.33MHz reference frequency
- VCO range: 250MHz to 500MHz
- Cycle-to-cycle jitter: 120ps (maximum)
- Period jitter, RMS: 20ps (maximum)
- Output skew: 65ps (maximum)
- Static phase offset: 160ps ± 160ps
- Voltage Supply Modes:
  $V_{DD}/V_{DDA}/V_{DDO}$
  3.3/3.3/3.3
  3.3/3.3/2.5
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS87604I
28-Lead TSSOP, 240-MIL
6.1mm x 9.7mm x 0.92mm
body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Core supply pin.
2	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels.
3, 9, 20, 21	GND	Power		Power supply ground.
4	FB_OUT	Output		Feedback output. Connect to FB_IN. LVCMOS / LVTTL interface levels.
5	REF_OUT	Output		Reference clock output. LVCMOS / LVTTL interface levels.
6, 12	V_{DDO}	Power		Output supply pin
7, 8, 10, 11	Q3, Q2, Q1, Q0	Output		Clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
13	PLL_SEL	Input	Pullup	Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.
14	V_{DDA}	Power		Analog supply pin. See Applications Note for filtering.
15	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or reference clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_IN when LOW. LVCMOS / LVTTL interface levels.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
18	REF_IN	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
19, 22, 24	nc	Unused		No connect.
23	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
25, 26	DIV_SEL0, DIV_SEL1	Input	Pulldown	Selects divide value for clock outputs as described in Table 3. LVCMOS / LVTTL interface levels.
27, 28	FBDIV_SEL0, FBDIV_SEL1	Input	Pulldown	Selects divide value for reference clock output and feedback output. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor				51	kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51	kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			9	pF
		V_{DD}, V_{DDA} = 3.465V; V_{DDO} = 2.625V			11	pF
R_{OUT}	Output Impedance			15		Ω

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs	Outputs	
MR	**Q0:Q3**	**FB_OUT, REF_OUT**
1	LOW	LOW
0	Active	Active

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
XTAL_SEL	**PLL Input**
0	REF_IN
1	XTAL Oscillator

TABLE 3D. CONTROL FUNCTION TABLE

Inputs					Outputs		
					PLL_SEL=1	Frequency	
FBDIV_SEL1	**FBDIV_SEL0**	**DIV_SEL1**	**DIV_SEL0**	**Reference Frequency Range (MHz)**	**Q0:Q3**	**Q0:Q3 (MHz)**	**FB_OUT (MHz)**
0	0	0	0	16.67 - 41.67	x 4	66.68 - 166.68	16.67 - 41.67
0	0	0	1	16.67 - 41.67	x 3	50 - 125	16.67 - 41.67
0	0	1	0	16.67 - 41.67	x 2	33.34 - 83.34	16.67 - 41.67
0	0	1	1	16.67 - 41.67	x 1	16.67 - 41.67	16.67 - 41.67
0	1	0	0	12.5 - 31.25	x 5.33	66.63 - 166.56	12.5 - 31.25
0	1	0	1	12.5 - 31.25	x 4	50 - 125	12.5 - 31.25
0	1	1	0	12.5 - 31.25	x 2.667	33.34 - 83.34	12.5 - 31.25
0	1	1	1	12.5 - 31.25	x 1.33	16.63 - 41.56	12.5 - 31.25
1	0	0	0	10 - 25	x 6.667	66.67 - 166.68	10 - 25
1	0	0	1	10 - 25	x 5	50 - 125	10 - 25
1	0	1	0	10 - 25	x 3.33	33.30 - 83.25	10 - 25
1	0	1	1	10 - 25	x 1.66	16.60 - 41.50	10 - 25
1	1	0	0	8.33 - 20.83	x 8	66.64 - 166.64	8.33 - 20.83
1	1	0	1	8.33 - 20.83	x 6	50 - 125	8.33 - 20.83
1	1	1	0	8.33 - 20.83	x 4	33.32 - 83.32	8.33 - 20.83
1	1	1	1	8.33 - 20.83	x 2	16.66 - 41.66	8.33 - 20.83

NOTE: VCO frequency range for all configurations above is 250MHz to 500MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	49.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				185	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				20	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR, DIV_ SEL0, DIV_SEL1, FBDIV_SEL0, FBDIV_SEL1, XTAL_SEL, FB_IN, PLL_SEL		2		V_{DD} + 0.3	V
		REF_IN		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	MR, DIV_ SEL0, DIV_SEL1, FBDIV_SEL0, FBDIV_SEL1, XTAL_SEL, FB_IN, PLL_SEL		-0.3		0.8	V
		REF_IN		-0.3		1.3	V
I_{IH}	Input High Current	DIV_ SEL0, DIV_SEL1, FBDIV_SEL0, FBDIV_SEL1, MR, FB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		XTAL_SEL, PLL_SEL	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_ SEL0, DIV_SEL1, FBDIV_SEL0, FBDIV_SEL1, MR, FB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		XTAL_SEL, PLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DD} = V_{IN}$ = 3.465V	2.6			V
			$V_{DD} = V_{IN}$ = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		38	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance			7		pF

TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Reference Frequency		8.33		41.67	MHz

TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1	FREF = 25MHz	0	160	325	ps
*t*sk(o)	Output Skew; NOTE 2, 5				65	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; 5				120	ps
*t*jit(per)	Period Jitter, RMS; NOTE 3, 5, 6				20	ps
*t*sl(o)	Slew Rate		1		4	V/ns
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle; NOTE 4		48		52	%

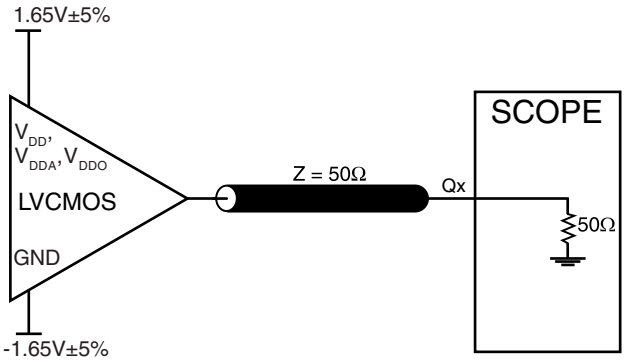
All parameters measured with feedback and output dividers set to DIV by 12 unless otherwise noted.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured at $V_{DD}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Jitter performance using LVCMOS inputs.
NOTE 4: Measured using REF_IN. For XTAL input, refer to Application Note.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: This parameter is defined as an RMS value.

TABLE 7B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

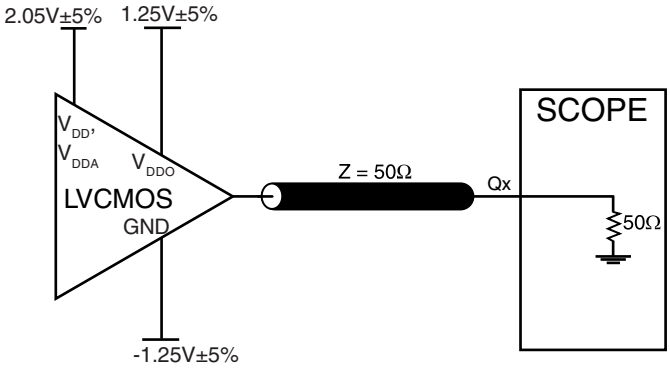
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1	FREF = 25MHz	-365	-105	160	ps
*t*sk(o)	Output Skew; NOTE 2, 5				50	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; 5				170	ps
*t*jit(per)	Period Jitter, RMS; NOTE 3, 5, 6				20	ps
*t*sl(o)	Slew Rate		1		4	V/ns
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle; NOTE 4		48		52	%

See Table 7A for notes.

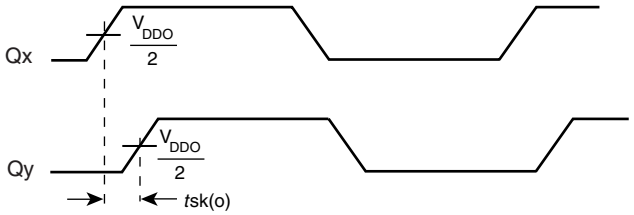
PARAMETER MEASUREMENT INFORMATION



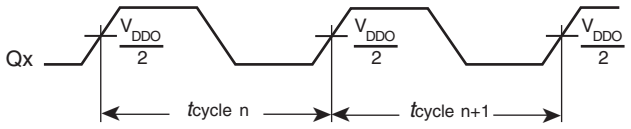
3.3V OUTPUT LOAD AC TEST CIRCUIT



3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



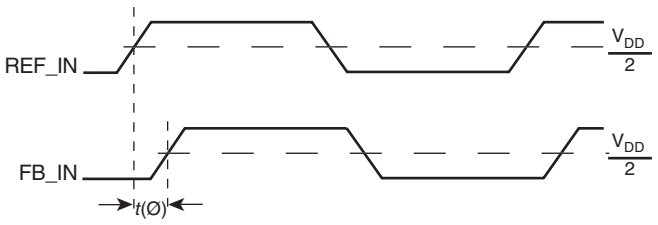
OUTPUT SKEW



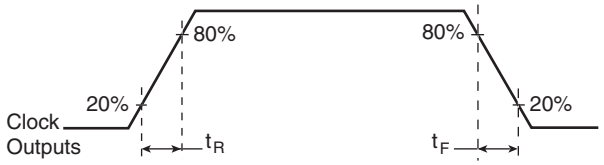
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

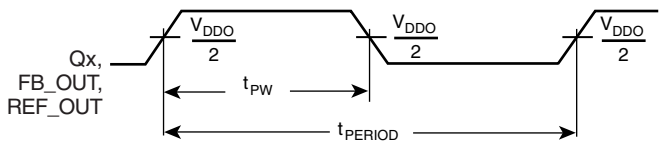
CYCLE-TO-CYCLE JITTER



STATIC PHASE OFFSET



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT PULSE WIDTH/PULSE WIDTH PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87604I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

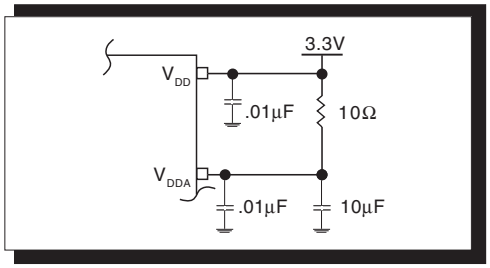


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS87604I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the frequency ppm error. The optimum C1 and C2 values can be slightly adjusted for optimum frequency accuracy.

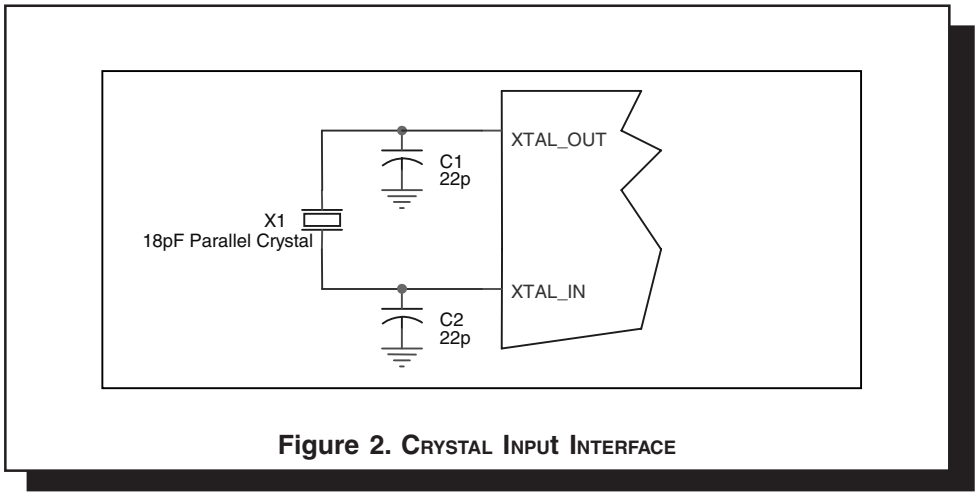


Figure 2. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87604I is: 5495

PACKAGE OUTLINE - G SUFFIX FOR 28 LEAD TSSOP

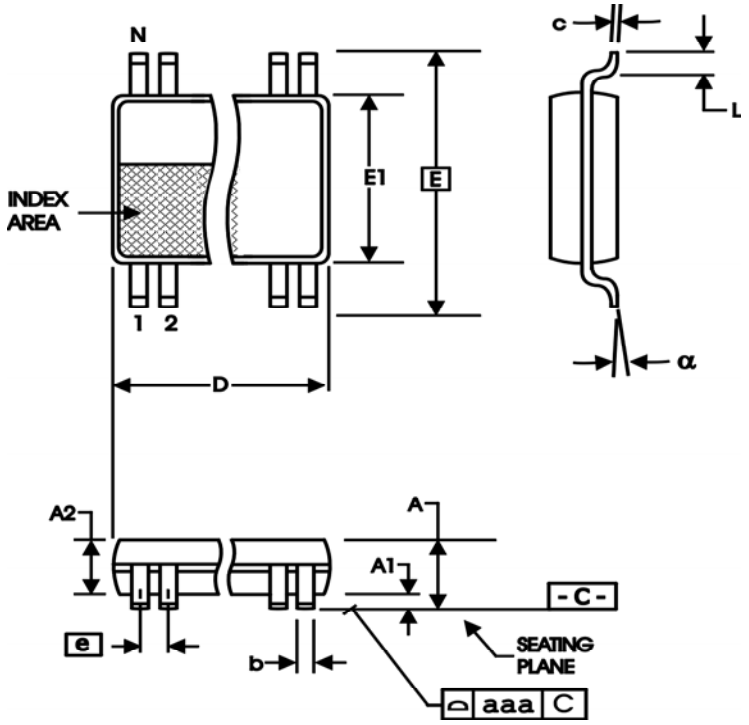


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	8.10 BASIC	
E1	6.00	6.20
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87604AGI	ICS87604AGI	28 Lead TSSOP	tube	-40°C to 85°C
ICS87604AGIT	ICS87604AGI	28 Lead TSSOP	1000 tape & reel	-40°C to 85°C
ICS87604AGILF	ICS87604AGILF	28 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS87604AGILFT	ICS87604AGILF	28 Lead "Lead-Free" TSSOP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T7A & T7B	5	AC Characteristics Tables - corrected note sequence.	3/18/05
A	10	10	Ordering Information Table - added marking.	4/12/05