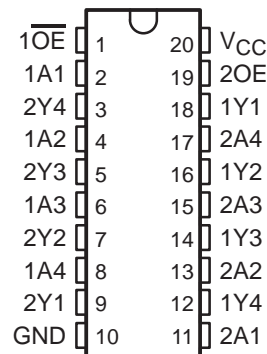


SN74LVC241A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS343E – MARCH 1994 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC241A is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'LVC240A and 'LVC244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{OE} (active-low output-enable) inputs, and complementary OE and \overline{OE} inputs.

The SN74LVC241A is organized as two 4-bit line drivers with separate output-enable ($1\overline{OE}$, 2OE) inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC241A is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW



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 **TEXAS
INSTRUMENTS**

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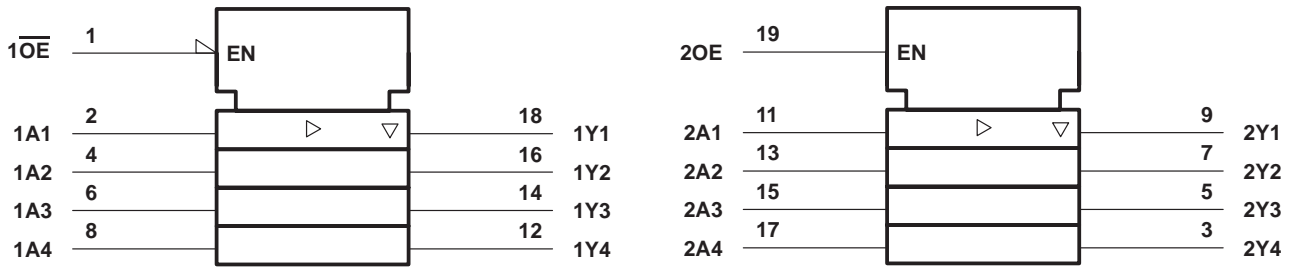
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FUNCTION TABLES

INPUTS		OUTPUT
1OE	1A	1Y
L	H	H
L	L	L
H	X	Z

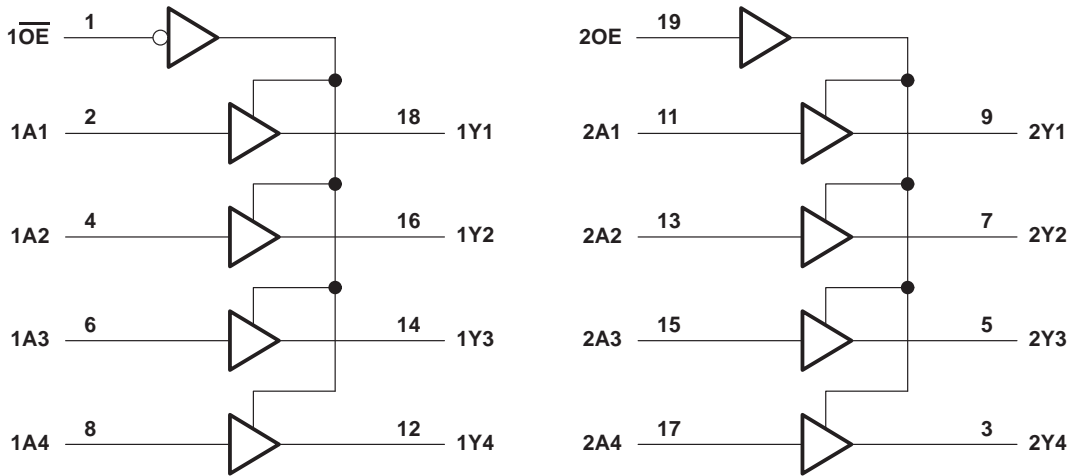
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to 2.7 V		0.7	
	$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3 state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -8 mA	2.3 V	1.7			
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 0 to 5.5 V	3.6 V			±5	μA
I _{off}	V _I or V _O = 5.5 V	0			±10	μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND	3.6 V	I _O = 0		10	μA
	3.6 V ≤ V _I ≤ 5.5 V‡				10	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V				pF
C _o	V _O = V _{CC} or GND	3.3 V				pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y									ns
t _{en}	$\overline{\text{OE}}$ or OE	Y									ns
t _{dis}	$\overline{\text{OE}}$ or OE	Y									ns

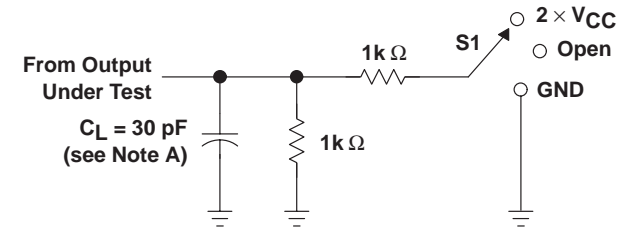
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		TYP	TYP	TYP	TYP			
C _{pd}	Power dissipation capacitance per buffer/driver	f = 10 MHz	Outputs enabled					pF
	Outputs disabled							

PRODUCT PREVIEW



PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

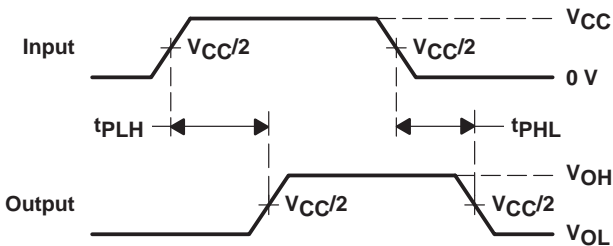


LOAD CIRCUIT

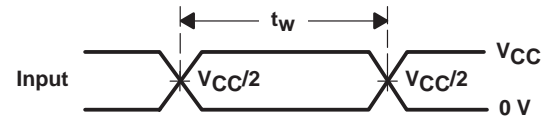
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	Open



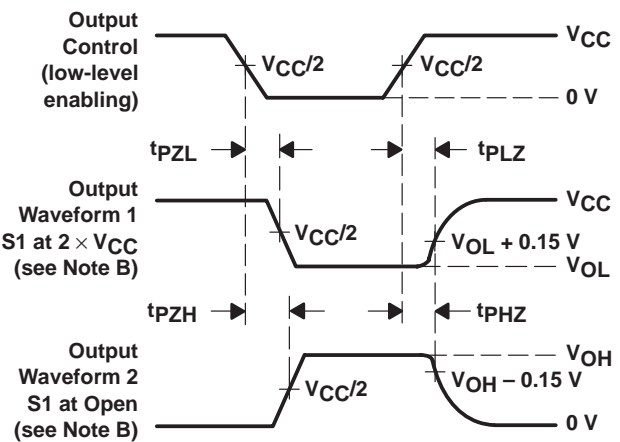
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

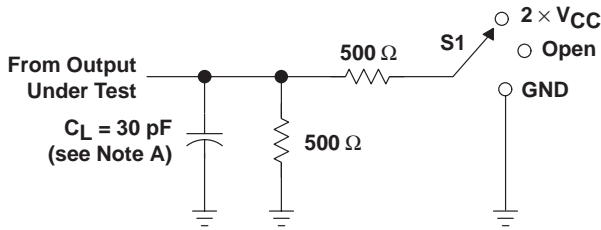
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SN74LVC241A
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WITH 3-STATE OUTPUTS

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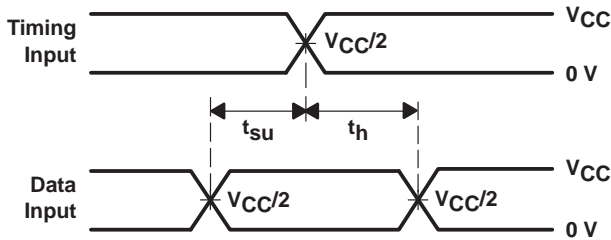
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

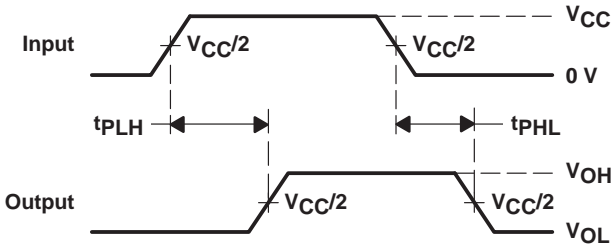


LOAD CIRCUIT

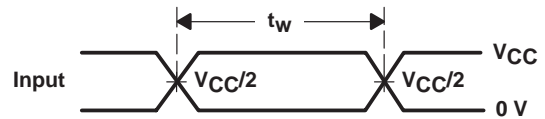
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



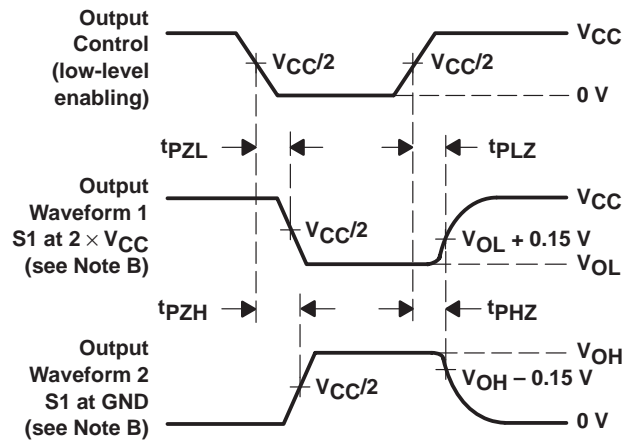
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



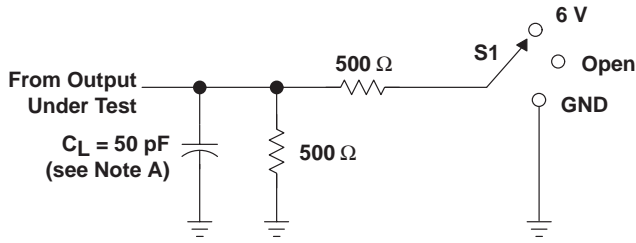
**VOLTAGE WAVEFORMS
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 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

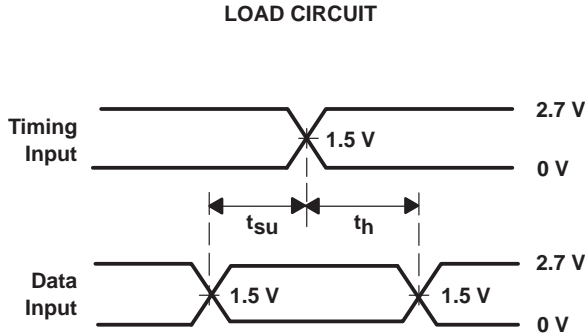
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

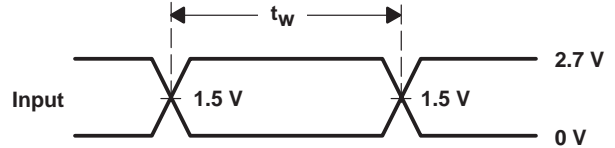


LOAD CIRCUIT

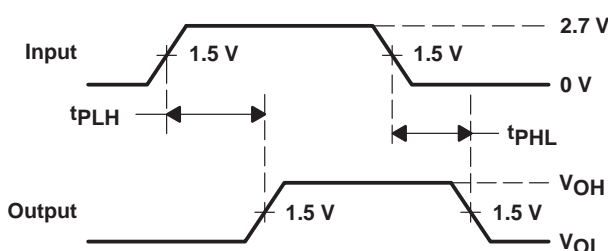
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



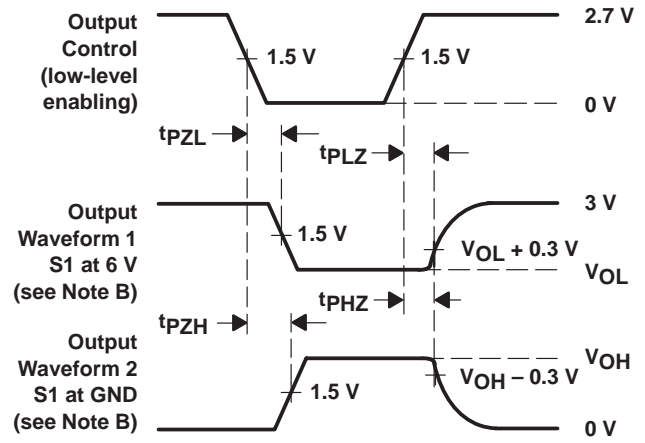
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
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**VOLTAGE WAVEFORMS
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 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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