Description

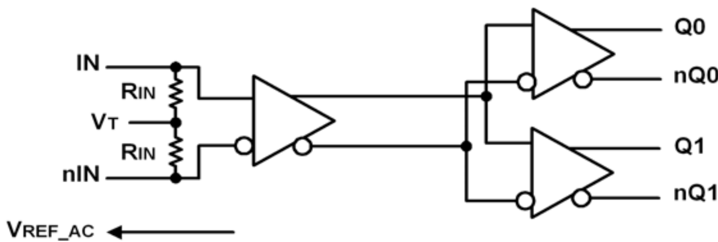
The IDT8S54011I is a high speed 1-to-2 Differential-to-CML Fanout Buffer. The IDT8S54011I is optimized for high speed and very low output skew, making it suitable for use in demanding applications requiring only the highest performing devices. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVDS, LVPECL and CML to be easily interfaced to the input with minimal use of external components.

The IDT8S54011I is packaged in a small 3 x 3 mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

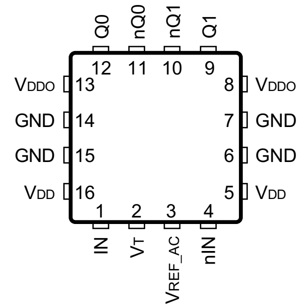
Features

- Two differential CML output pairs
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 3.2GHz
- Output skew: 5ps (typical)
- Part-to-part skew: 100ps (maximum)
- Additive phase jitter, RMS: 0.059ps (typical)
- Propagation delay: 225ps (typical)
- Operating supply modes:
  Core/Output
  2.5V/1.8V
  2.5V/1.2V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



IDT8S54011I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
NL Package
Top View

Table 1. Pin Descriptions

Number	Name	Type	Description
1	IN	Input	Non-inverting differential clock input.
2	V_T	Input	Termination input.
3	V_{REF_AC}	Output	Reference voltage for AC-coupled applications.
4	nIN	Input	Inverting differential clock input.
5, 16	V_{DD}	Power	Power supply pins.
6, 7, 14, 15	GND	Power	Power supply ground.
8, 13	V_{DDO}	Power	Output supply pins.
9, 10	Q1, nQ1	Output	Differential output pair. CML interface levels.
11, 12	nQ0, Q0	Output	Differential output pair. CML interface levels.

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.
These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V (CML mode, GND = 0V)
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 20mA 40mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 2A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.1V, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.7	1.8	1.9	V
I_{DD}	Power Supply Current				38	mA
I_{DDO}	Output Supply Current	Outputs are terminated with 50Ω to V_{DDO}			40	mA

Table 2B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.2V ± 5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}	Power Supply Current				38	mA
I_{DDO}	Output Supply Current	Outputs are terminated with 50Ω to V_{DDO}			40	mA

Table 2C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	IN, nIN	IN to V_T, nIN to V_T	40	50	60	Ω
V_{IH}	Input High Voltage	IN, nIN		1.2		V_{DD}	V
V_{IL}	Input Low Voltage	IN, nIN		0.2		V_{IH} – 0.1	V
V_{IN}	Input Voltage Swing; NOTE 1			0.1		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.2		2.0	V
V_{T_IN}	Voltage between IN and V_T	IN, nIN				1.28	V
V_{REF_AC}	Bias Voltage			V_{DD} – 1.31	V_{DD} – 1.28	V_{DD} – 1.25	V

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing* diagram.

Table 2D. CML DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.1V or 1.2V ± 5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OUT}	Output Voltage Swing		300	390	475	mV
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} – 0.02	V_{DDO} – 0.01	V_{DDO}	V
V_{DIFF_OUT}	Differential Output Voltage Swing		600	780	950	mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

NOTE 1: Outputs terminated with 50Ω to V_{DDO}.

AC Electrical Characteristics

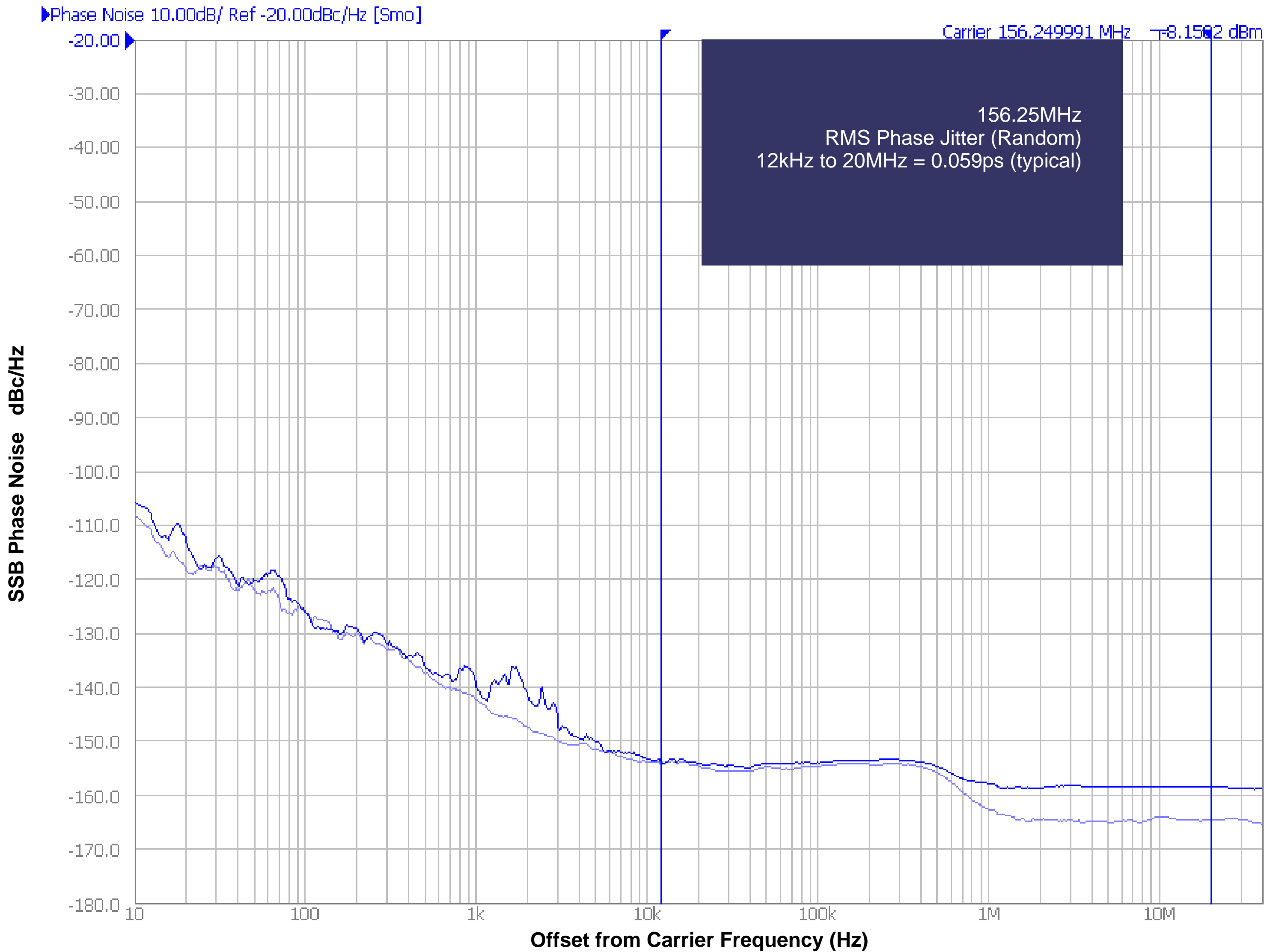
Table 3. AC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.1V or 1.2V ± 5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	V_{OUT} > 200mV			3.2	GHz
t_{PD}	Propagation Delay; NOTE 1		150	225	300	ps
*t*sk(o)	Output Skew; NOTE 2, 3			3	15	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				100	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	156.25MHz, Integration Range: 12kHz - 20MHz		0.059	0.087	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	30		120	ps
odc	Output Duty Cycle		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at $f_{OUT} \leq$ 1.5GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

Additive Phase Jitter

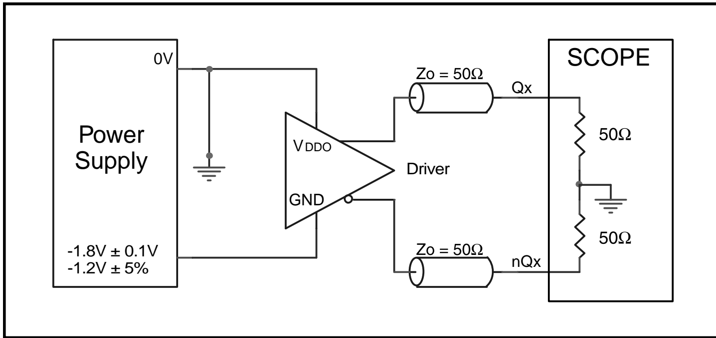
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



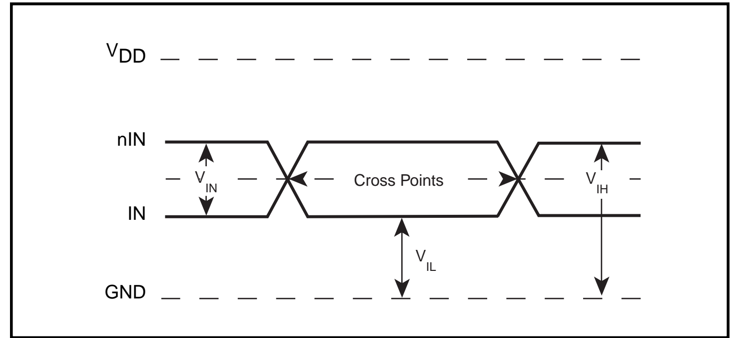
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzell 156.25MHz Oscillator as the input source.

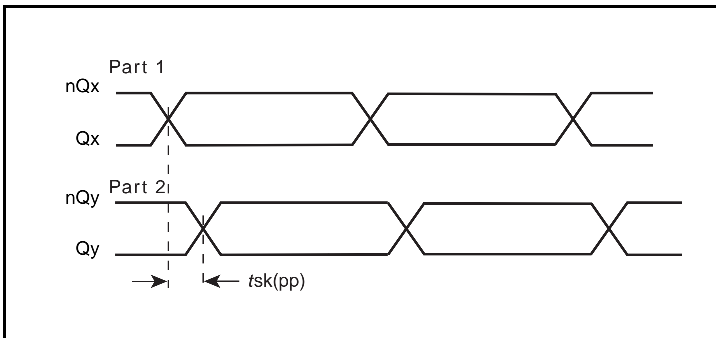
Parameter Measurement Information



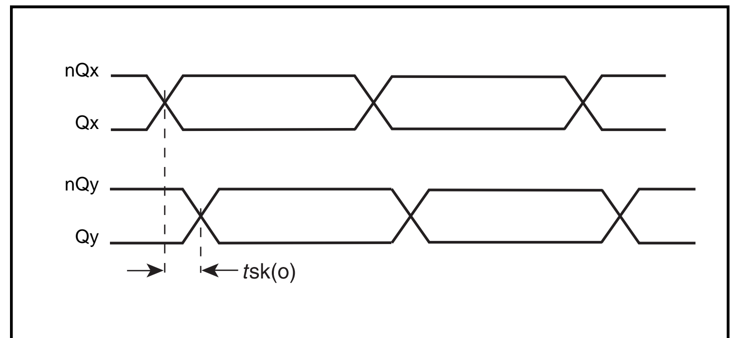
CML Output Load AC Test Circuit



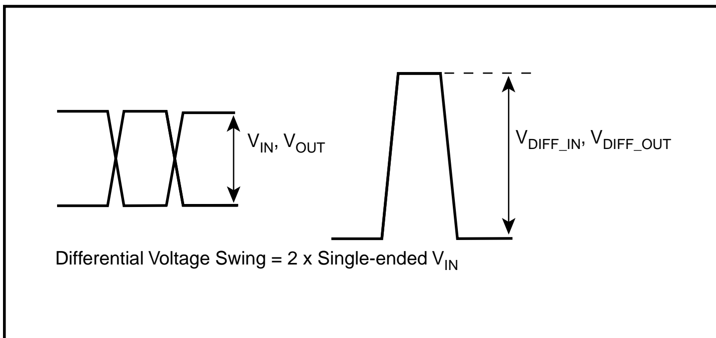
Differential Input Level



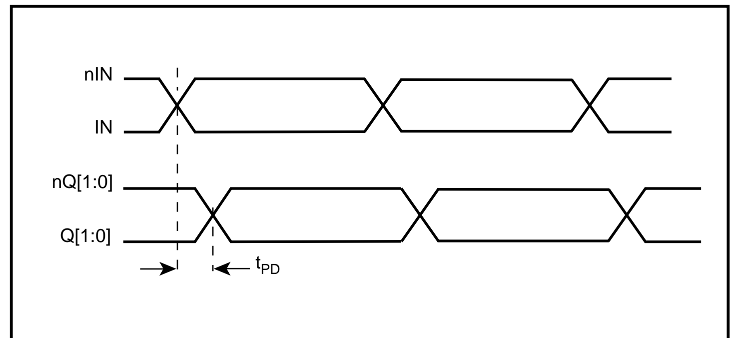
Part-to-Part Skew



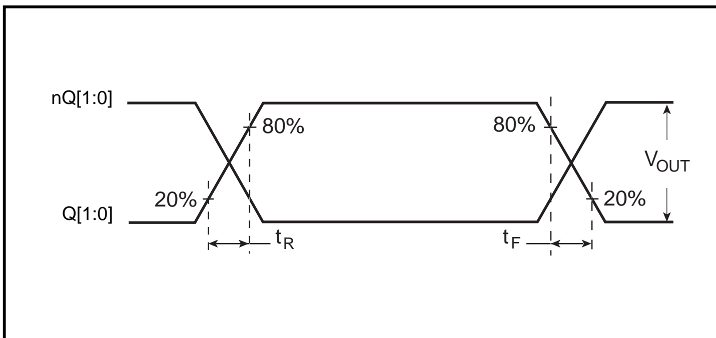
Output Skew



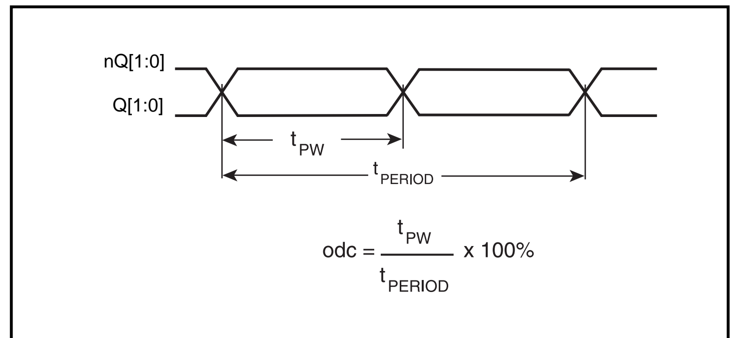
Single-ended & Differential Voltage Swing



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

© 2019 Renesas Electronics Corporation

Applications Information

2.5V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 1A to 1D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

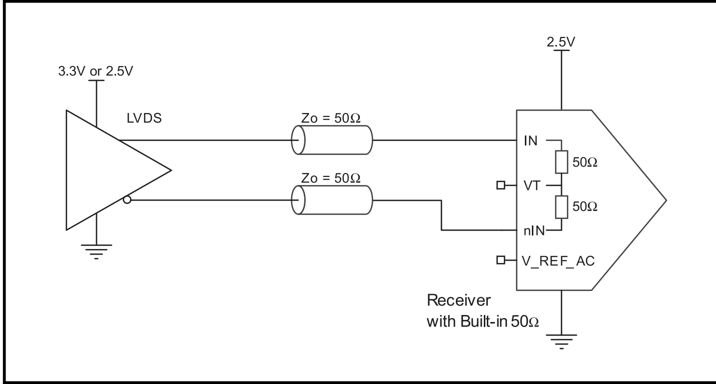


Figure 1A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

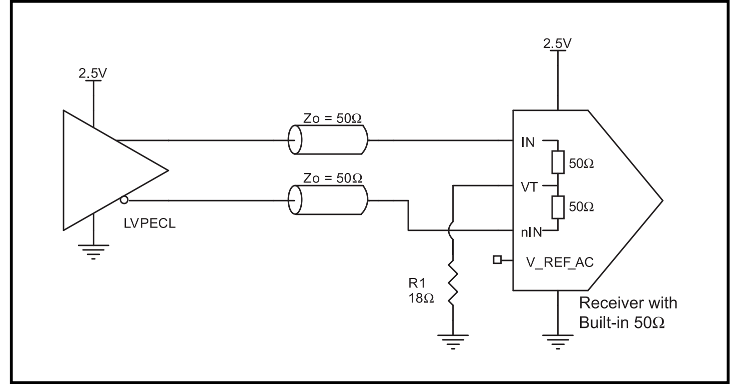


Figure 1B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

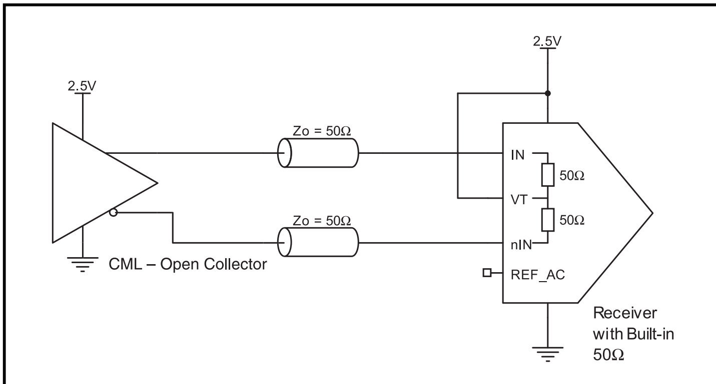


Figure 1C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

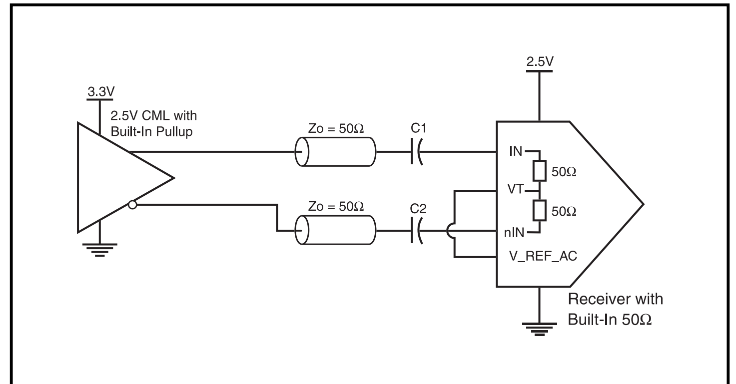


Figure 1D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

© 2019 Renesas Electronics Corporation

CML Termination

Figure 2 shows an example of the termination for a CML driver. In this example, the transmission line characteristic impedance is 50Ω. The R1 and R2 50Ω matched load terminations are pulled up to V_{DDO}. The matched loads are located close to the receiver.

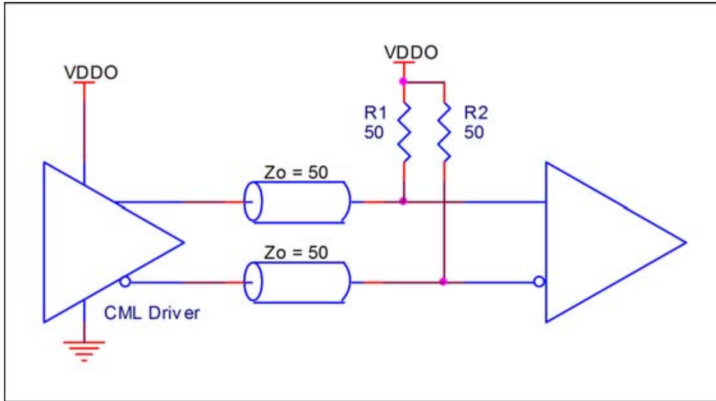


Figure 2. CML Termination Example

Recommendations for Unused Output Pins

Outputs

CML Outputs

All unused CML outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

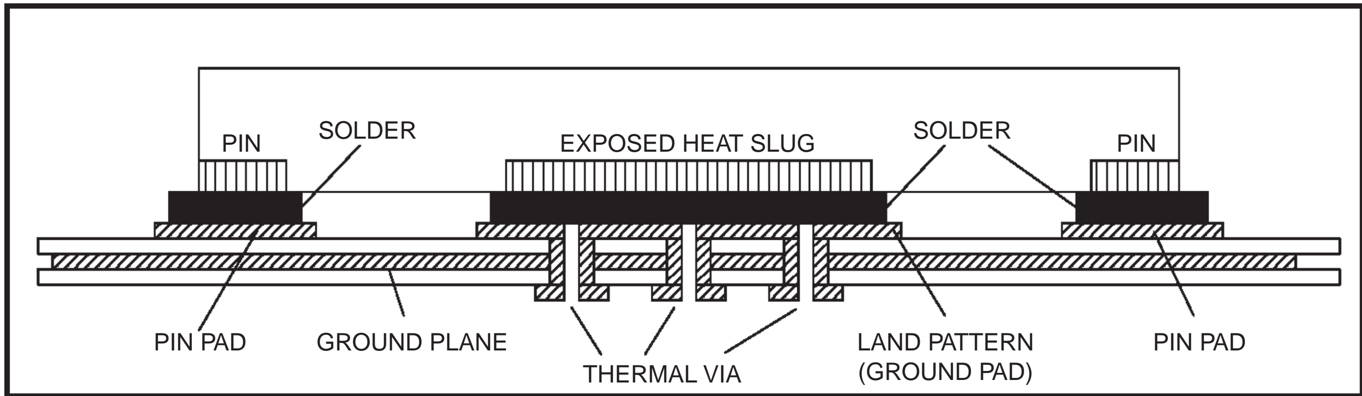


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

© 2019 Renesas Electronics Corporation

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8S54011I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8S54011I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, and V_{DDO} = 1.8V +0.1V = 1.9V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX}$ = V_{DD_MAX} * I_{DD} = 2.625V * 38mA = **99.75mW**
- Power $(outputs)_{MAX}$ = V_{DDO_MAX} * I_{DDO} = 1.9V * 40mA = **76mW**
- Power $(load)_{MAX}$ = **14.25mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 14.25mW = **28.5mW**
- Power Dissipation for internal termination R_T
  Power $(R_{IN})_{MAX}$ = $(V_{IN_MAX})^2$ / R_{IN_MIN} = $(1.0V)^2$ / 80Ω = **12.5mW**

Total Power$_{_MAX}$ (All outputs switching) = 99.75mW + 76mW + 28.5mW + 12.5mW = **216.75mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.216W * 74.7°C/W = 101.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 4. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

© 2019 Renesas Electronics Corporation

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the CML driver output pair. The CML output circuit and termination are shown in Figure 4.

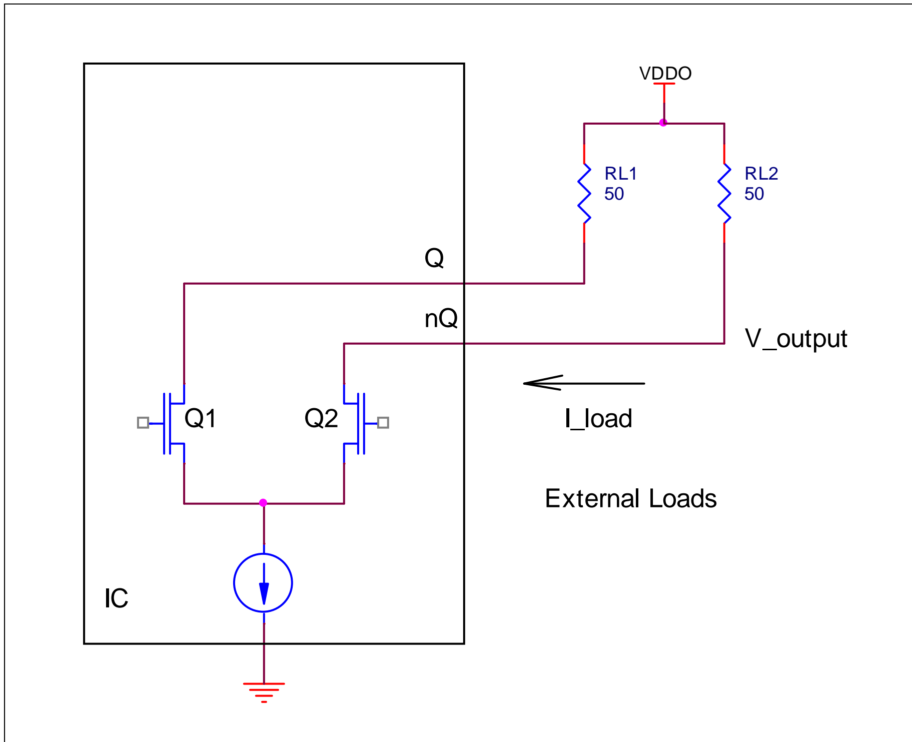


Figure 4. CML Driver Circuit and Termination

To calculate worst case power dissipation due to the load, use the following equations.

Output Driver Power Dissipation:

Pd_L = I_Load * V_Output

$= (V_{OUT_MAX}/R_L) * (V_{DDO_MAX} - V_{OUT_MAX})$

$= (0.475V/50\Omega) * (1.9V - 0.475V)$

= 13.5mW

Power dissipation when the output driver is logic HIGH:

Pd_H = I_Load * V_Output

$= (0.02V/50\Omega) * (1.9V - 0.02V)$

= 0.75mW

Total Power Dissipation per output pair = Pd_H + Pd_L = **14.25mW**

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for IDT8S54011I is: 328

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 6. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S54011ANLGI	011AI	“Lead-Free” 16 Lead VFQFN	Tray	-40°C to 85°C
8S54011ANLGI8	011AI	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

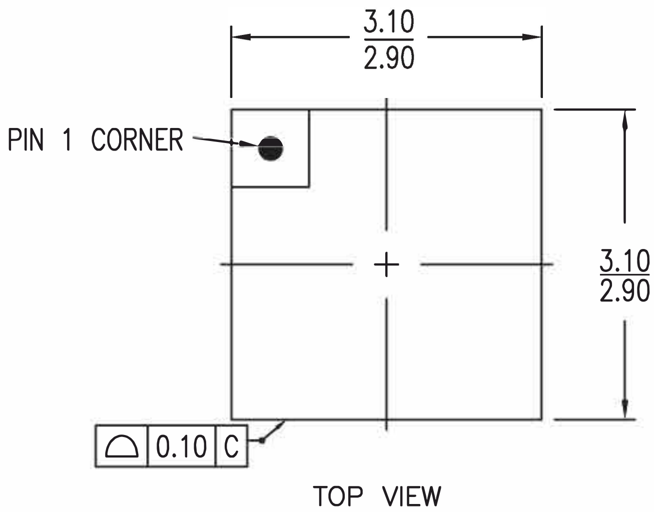
Revision Date	Description of Change
September 21, 2017	Updated the package outline drawings; however, no mechanical changes Completed other minor improvements
August 2, 2012	Initial release.

© 2019 Renesas Electronics Corporation

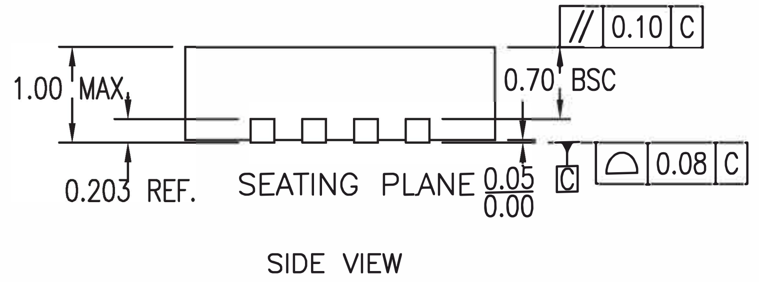
16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

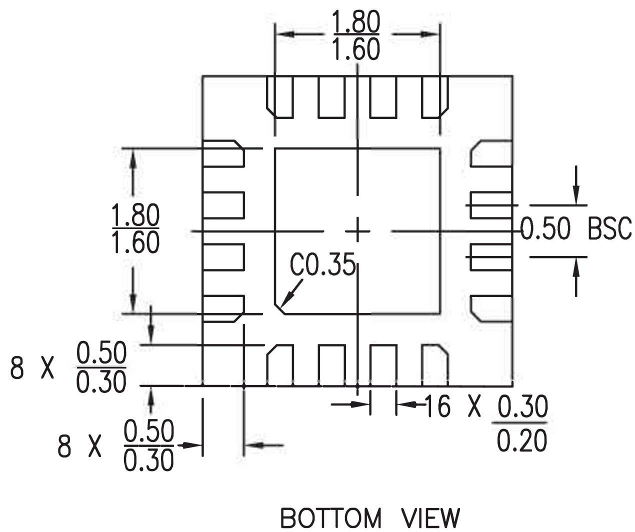
NL/NLG16P2, PSC-4169-02, Rev 03, Page 1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES

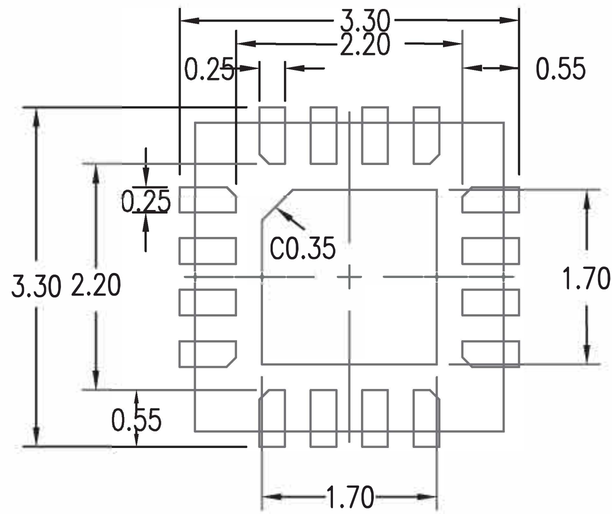
© 2019 Renesas Electronics Corporation

RENESAS

16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

NL/NLG16P2, PSC-4169-02, Rev 03, Page 2



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

© 2020 Renesas Electronics Corporation. All rights reserved.