



# Synchronous 4-Bit Decade Counter (Asynchronous Clear)

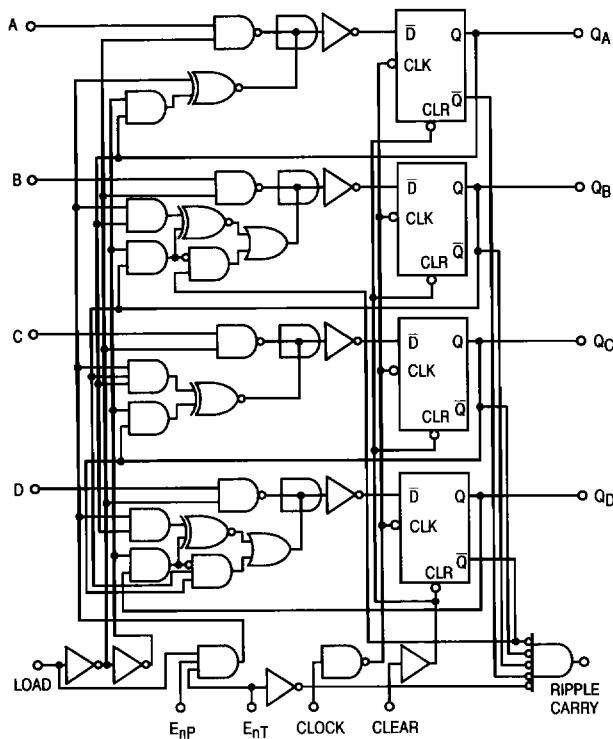
ELECTRICALLY TESTED PER:  
MIL-M-38510/31503

The 'LS160A is a high-speed 4-bit synchronous counter. It is edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The 'LS160A can count modulo 10 (BCD).

The 'LS160A has an asynchronous Master Reset (Clear) input that overrides, and is independent of the clock and all other control inputs.

- Synchronous Counting and Loading
- Two Count Enable Inputs For High-Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Typical Count Rate of 35 MHz

LOGIC DIAGRAM



## Military 54LS160A



AVAILABLE AS:

- 1) JAN: JM38510/31503BXA
- 2) SMD: 7700901
- 3) 883: 54LS160A/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

| FUNCT. | DIL<br>620-09 | FLATS<br>650-05 | LCC<br>756A-02 | BURN-IN<br>(COND. A) |
|--------|---------------|-----------------|----------------|----------------------|
| CLR    | 1             | 1               | 2              | GND                  |
| CLK    | 2             | 2               | 3              | VCC                  |
| A      | 3             | 3               | 4              | VCC                  |
| B      | 4             | 4               | 5              | VCC                  |
| C      | 5             | 5               | 7              | VCC                  |
| D      | 6             | 6               | 8              | VCC                  |
| EnP    | 7             | 7               | 9              | VCC                  |
| GND    | 8             | 8               | 10             | GND                  |
| Ld     | 9             | 9               | 12             | VCC                  |
| EnT    | 10            | 10              | 13             | VCC                  |
| QD     | 11            | 11              | 14             | OPEN                 |
| QC     | 12            | 12              | 15             | OPEN                 |
| QB     | 13            | 13              | 17             | OPEN                 |
| QA     | 14            | 14              | 18             | OPEN                 |
| RC     | 15            | 15              | 19             | OPEN                 |
| VCC    | 16            | 16              | 20             | VCC                  |

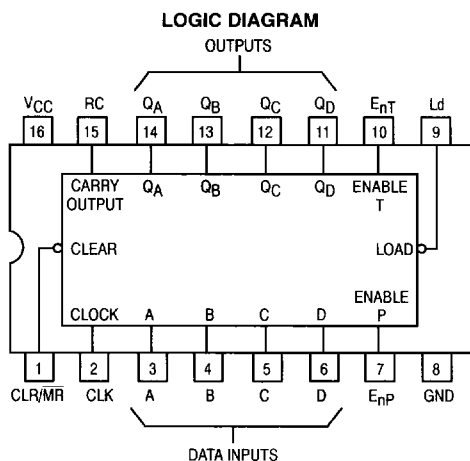
BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

| Ld | EnT | EnP | Action on the Rising<br>Clock Edge (↑) |
|----|-----|-----|--|
| X  | X   | X   | Reset (Clear)                          |
| L  | X   | X   | Load (D <sub>n</sub> -Q <sub>n</sub> ) |
| H  | H   | H   | Count (Increment)                      |
| H  | L   | X   | No Change (Hold)                       |
| H  | X   | L   | No Change (Hold)                       |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

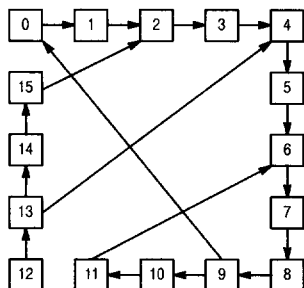
5



| Pin Names                      |   | Loading (Note b) |             |
|--------------------------------|---|------------------|-------------|
|                                |   | HIGH             | LOW         |
| Load                           | Parallel Enable (Active LOW)                  | 1.0 U.L.         | 0.5 U.L.    |
| A-D                            | Parallel Inputs (Data Inputs)                 | 0.5 U.L.         | 0.25 U.L.   |
| EN <sub>P</sub>                | Count Enable Parallel Input                   | 0.5 U.L.         | 0.25 U.L.   |
| EN <sub>T</sub>                | Count Enable Trickle Input                    | 1.0 U.L.         | 0.5 U.L.    |
| CLK                            | Clock (Active HIGH Going Edge) Input          | 0.5 U.L.         | 0.25 U.L.   |
| CLR                            | Master Reset (Active LOW) Input               | 1.0 U.L.         | 0.25 U.L.   |
| Q <sub>A</sub> -Q <sub>D</sub> | Parallel Outputs (Note b)                     | 10 U.L.          | 5(2.5) U.L. |
| RC                             | Terminal Count (Ripple Carry) Output (Note b) | 10 U.L.          | 5(2.5) U.L. |

**NOTES:**

- a. One TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

**STATE DIAGRAM****LOGIC EQUATIONS**

Count Enable =  $E_{nP} \cdot E_{nT} \cdot Ld$   
 RC for LS160A =  $E_{nT} \cdot Q_A \cdot \bar{Q}_B \cdot \bar{Q}_C \cdot Q_D$   
 Preset =  $\bar{Ld} \cdot CLK +$  (rising clock edge)  
 Reset =  $\bar{CLR}$

**NOTE:**

The LS160A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

**FUNCTIONAL DESCRIPTION**

The 'LS160A is a 4-bit synchronous counter with a synchronous Parallel Enable (Load) feature. The counter consists of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CLK). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs – Parallel Enable (Ld), Count Enable Parallel (EN<sub>P</sub>) and Count Enable Trickle (EN<sub>T</sub>) – select the mode of operation as shown in the table below. The Count Mode is enabled when the EN<sub>P</sub>, EN<sub>T</sub>, and Ld inputs are HIGH. When the Ld is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the EN<sub>P</sub> or EN<sub>T</sub> can be used to inhibit the count sequence. With the Ld held HIGH, a LOW on either the EN<sub>P</sub> or EN<sub>T</sub> inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (EN<sub>P</sub> • EN<sub>T</sub>) allows synchronous cascading

without external gating and without delay accumulation over any practical number of bits or digits.

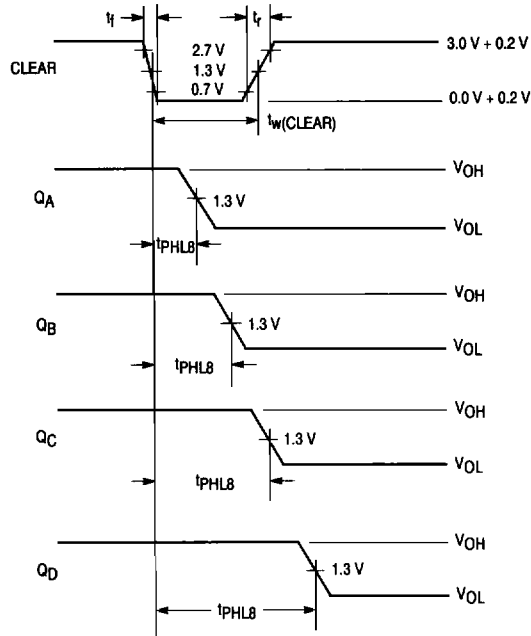
The Terminal Count (RC) output is HIGH when the Counter Enable Trickle (EN<sub>T</sub>) input is HIGH while the counter is in its maximum count state (HLLH for BCD counters, HHHH for Binary counters). Note that RC is fully decoded and will, therefore, be HIGH only for one count state.

The 'LS160A counts modulo 10 following a binary coded decimal (BCD) sequence. They generate a RC output when the EN<sub>T</sub> input is HIGH while the counter is in the state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generate a RC output.

The Master Reset (MR) of the 'LS160A is asynchronous. When the MR is LOW, it overrides all other input conditions and sets the outputs LOW. The MR pin should never be left open. If not used, the MR pin should be tied through a resistor to V<sub>CC</sub>, or to a gate output which is permanently set to a HIGH logic level.

54LS160A

VOLTAGE WAVEFORM 1

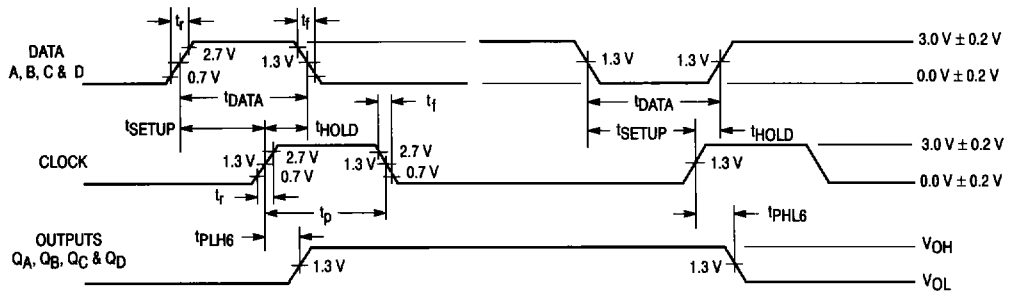


NOTE:

The Clear pulse generator has the following characteristics:  
 $V_{gen} = 3.0\text{ V}$ ,  $t_r \leq 15\text{ ns}$ ,  $t_f \leq 6.0\text{ ns}$ ,  $t_w(\text{Clear}) = 20\text{ ns}$ .

5

VOLTAGE WAVEFORM 2

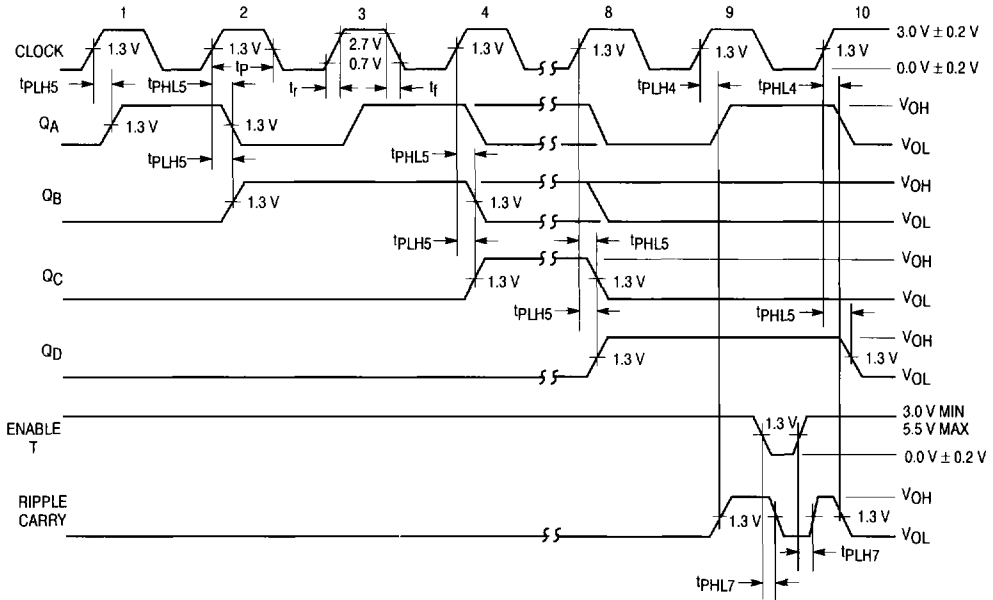


NOTE:

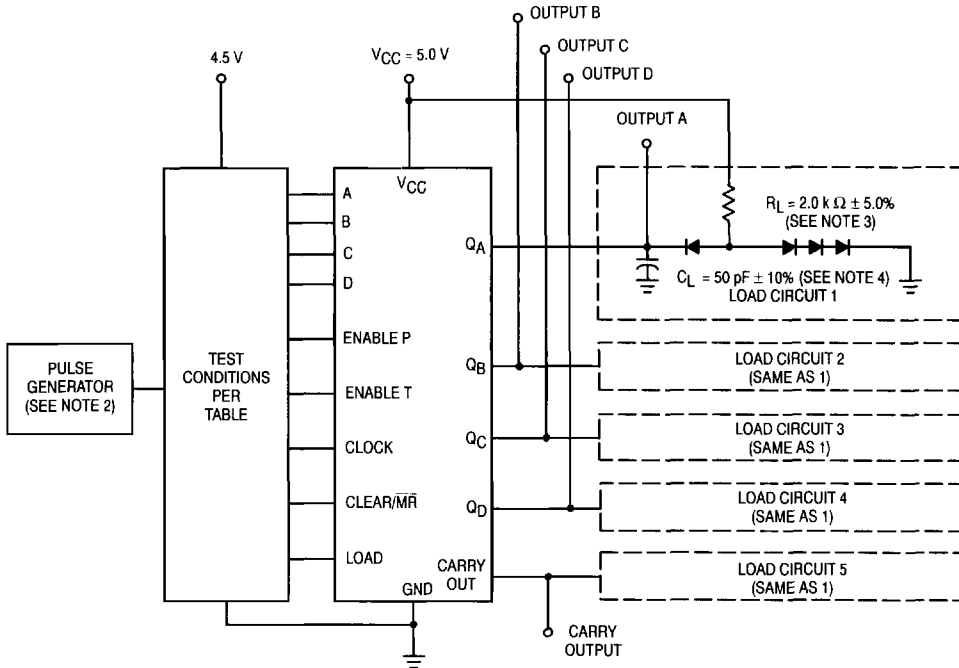
The data pulse generator has the following characteristics:  
 $V_{gen} = 3.0\text{ V}$ ,  $t_r \leq 15\text{ ns}$ ,  $t_f \leq 6.0\text{ ns}$ ,  $t_{DATA} = 30\text{ ns}$ ,  $t_{SETUP} = 20\text{ ns}$ ,  
 $t_{HOLD} = 10\text{ ns}$ .

54LS160A

VOLTAGE WAVEFORM 3



TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-180

## 54LS160A

| Symbol           | Parameter                    | Limits     |      |             |      |             |      | Unit | Test Condition<br>(Unless Otherwise Specified)   |
|------------------|------------------------------|------------|------|-------------|------|-------------|------|------|--|
|                  |                              | + 25°C     |      | + 125°C     |      | - 55°C      |      |      |  |
|                  |                              | Subgroup 1 |      | Subgroup 2  |      | Subgroup 3  |      |      |  |
|                  |                              | Min        | Max  | Min         | Max  | Min         | Max  |      |  |
| V <sub>OH</sub>  | Logical "1" Output Voltage   | 2.5        |      | 2.5         |      | 2.5         |      | V    | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, CR = 4.5 V, E <sub>NP</sub> = open, CP = (See Note 7), V <sub>IH</sub> = 2.0 V, E <sub>NT</sub> = 2.0 V, L <sub>d</sub> = GND. |
| V <sub>OL</sub>  | Logical "0" Output Voltage   |            | 0.4  |             | 0.4  |             | 0.4  | V    | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IL</sub> = 0.7 V, L <sub>d</sub> = GND, CLK = (See Note 7), CR = 4.5 V, E <sub>NP</sub> = open, E <sub>NT</sub> = 0.7 V. |
| V <sub>IC</sub>  | Input Clamping Voltage       |            | -1.5 |             |      |             |      | V    | V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.  |
| I <sub>IH</sub>  | Logical "1" Input Current    |            | 20   |             | 20   |             | 20   | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, (other inputs are open).   |
| I <sub>IH</sub>  | Logical "1" Input Current    |            | 40   |             | 40   |             | 40   | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V (other inputs are open), (CLK, L <sub>d</sub> & E <sub>NT</sub> are open).  |
| I <sub>IHH</sub> | Logical "1" Input Current    |            | 100  |             | 100  |             | 100  | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V (other inputs are open).   |
| I <sub>IHH</sub> | Logical "1" Input Current    |            | 200  |             | 200  |             | 200  | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V (other inputs are open), (CLK, L <sub>d</sub> & E <sub>NP/T</sub> ) = GND or 5.5 V.  |
| I <sub>IL1</sub> | Logical "0" Input Current    | -150       | -380 | -150        | -380 | -150        | -380 | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, L <sub>d</sub> = 4.5 V, (other inputs are open), E <sub>NT</sub> = 4.5 V, CLK & CLR are open, E <sub>NP</sub> = 0.4 V.           |
| I <sub>IL2</sub> | Logical "0" Input Current    | 0          | -100 | 0           | -100 | 0           | -100 | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, L <sub>d</sub> = open or GND, (other inputs are open).   |
| I <sub>IL3</sub> | Logical "0" Input Current    | -160       | -400 | -160        | -400 | -160        | -400 | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, E <sub>NT</sub> /E <sub>NP</sub> = 4.5 V, (other inputs are open), L <sub>d</sub> = 0.4 V.                                       |
| I <sub>IL4</sub> | Logical "0" Input Current    | -300       | -760 | -300        | -760 | -300        | -760 | μA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, L <sub>d</sub> & E <sub>NP</sub> = 4.5 V or open, other inputs are open.   |
| I <sub>OS</sub>  | Output Short Circuit Current | -15        | -100 | -15         | -100 | -15         | -100 | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V (other inputs are open), L <sub>d</sub> = GND, V <sub>OUT</sub> = GND, CLK = (See Note 7), CR = 4.5 V, E <sub>NT/P</sub> = open.  |
| I <sub>CCH</sub> | Power Supply Current Off     |            | 31   |             | 31   |             | 31   | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs), L <sub>d</sub> = 5.5 V or GND.  |
| I <sub>CCL</sub> | Power Supply Current Off     |            | 32   |             | 32   |             | 32   | mA   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs), CLK = GND or 5.5 V.   |
| V <sub>IH</sub>  | Logical "1" Input Voltage    | 2.0        |      | 2.0         |      | 2.0         |      | V    | V <sub>CC</sub> = 4.5 V.   |
| V <sub>IL</sub>  | Logical "0" Input Voltage    |            | 0.7  |             | 0.7  |             | 0.7  | V    | V <sub>CC</sub> = 4.5 V.   |
|                  | Functional Tests             | Subgroup 7 |      | Subgroup 8A |      | Subgroup 8B |      |      | per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.  |

54LS160A

| Symbol                                 | Parameter   | Limits     |          |             |          |             |          | Unit | Test Condition<br>(Unless Otherwise Specified)  |
|--|---|------------|----------|-------------|----------|-------------|----------|------|---|
|  |   | + 25°C     |          | + 125°C     |          | - 55°C      |          |      |   |
|  |   | Subgroup 9 |          | Subgroup 10 |          | Subgroup 11 |          |      |   |
|  |   | Min        | Max      | Min         | Max      | Min         | Max      |      |   |
| t <sub>PHL4</sub><br>t <sub>PHL4</sub> | Propagation Delay<br>/Data-Output<br>CLK to Carry Out             | 3.0<br>—   | 40<br>35 | 3.0<br>—    | 56<br>51 | 3.0<br>—    | 56<br>51 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PLH4</sub><br>t <sub>PLH4</sub> | Propagation Delay<br>/Data-Output<br>CLK to Carry Out             | 3.0<br>—   | 40<br>35 | 3.0<br>—    | 56<br>51 | 3.0<br>—    | 56<br>51 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PHL5</sub><br>t <sub>PHL5</sub> | Propagation Delay<br>/Data-Output<br>CLK to Q <sub>n</sub>        | 3.0<br>—   | 32<br>27 | 3.0<br>—    | 45<br>40 | 3.0<br>—    | 45<br>40 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PLH5</sub><br>t <sub>PLH5</sub> | Propagation Delay<br>/Data-Output<br>CLK to Q <sub>n</sub>        | 3.0<br>—   | 29<br>24 | 3.0<br>—    | 41<br>36 | 3.0<br>—    | 41<br>36 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PHL6</sub><br>t <sub>PHL6</sub> | Propagation Delay<br>/Data-Output<br>CLK to Q <sub>n</sub>        | 3.0<br>—   | 32<br>27 | 3.0<br>—    | 48<br>43 | 3.0<br>—    | 48<br>43 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PLH6</sub><br>t <sub>PLH6</sub> | Propagation Delay<br>/Data-Output<br>CLK to Q <sub>n</sub>        | 3.0<br>—   | 29<br>24 | 3.0<br>—    | 42<br>37 | 3.0<br>—    | 42<br>37 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PHL7</sub><br>t <sub>PHL7</sub> | Propagation Delay<br>/Data-Output<br>E <sub>nT</sub> to Carry Out | 3.0<br>—   | 19<br>14 | 3.0<br>—    | 28<br>23 | 3.0<br>—    | 28<br>23 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PLH7</sub><br>t <sub>PLH7</sub> | Propagation Delay<br>/Data-Output<br>E <sub>nT</sub> to Carry Out | 3.0<br>—   | 19<br>14 | 3.0<br>—    | 28<br>23 | 3.0<br>—    | 28<br>23 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| t <sub>PHL8</sub><br>t <sub>PHL8</sub> | Propagation Delay<br>/Data-Output<br>CLR to Q <sub>n</sub>        | 3.0<br>—   | 33<br>28 | 3.0<br>—    | 46<br>41 | 3.0<br>—    | 46<br>41 | ns   | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |
| f <sub>MAX</sub><br>f <sub>MAX</sub>   | Maximum Clock<br>Frequency  | 22<br>25   |          | 22<br>—     |          | 22<br>—     |          | MHz  | V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.<br>V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF. |

NOTES:

1. Voltage measurements are made with respect to ground terminal.
2. The pulse generator has the following characteristics:  
V<sub>GEN</sub> = 3.0 V, t<sub>r</sub> = 6.0 ns, t<sub>f</sub> = 6.0 ns, t<sub>p</sub> = 0.5 μs, PRR ≤ 1.0 MHz, Z<sub>OUT</sub> = 50 Ω.
3. All diodes are 1N3064 or equivalent.
4. C<sub>L</sub> = 50 pF ± 10%, including scope probe and jig capacitance.
5. f<sub>MAX</sub>: t<sub>r</sub> = t<sub>f</sub> ≤ 6.0 ns.
6. The limits specified for C<sub>L</sub> = 15 pF are guaranteed but not tested.
7. Apply one pulse prior to measurement as follows:

