32K x 8 SRAM

MSM832 - 70/85/10

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Description

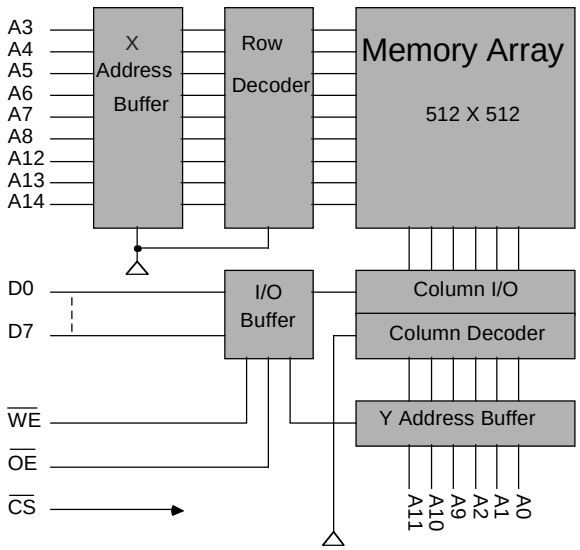
The MSM832 is a Static RAM organised as 32K x 8 available with access times of 70,85 or 100 ns. The device is available in two ceramic package options. It features completely static operation with a low power standby mode and is 3.0V battery back-up compatible. It is directly TTL compatible and has common data inputs and outputs.
The device may be screened in accordance with MIL-STD-883.

32,768 x 8 CMOS Static RAM

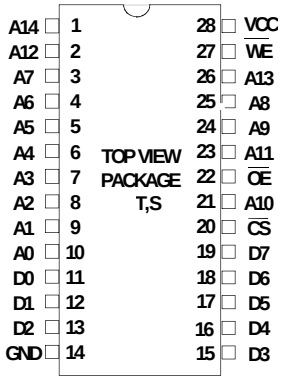
Features

- Fast Access Times of 70/85/100 ns.
- JEDEC Standard footprint.
- Low Power Operation : 550 mW (max)
- Low Power Standby : 2.2 mW (max) -L version.
- Low Voltage Data Retention.
- Directly TTL compatible.
- Completely Static Operation.

Block Diagram



Pin Definitions



Package Details

Pin Count	Description	Package Type
28	0.3" Dual-in-line (SKINNY DIP)	T
28	0.6"Dual-in-Line (DIP)	S

Pin Functions

A0-A14	Address inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{cc}	Power(+5V)
GND	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (Suffix **I**)
	T_{AM}	-55	-	125	°C (Suffix **M, MB**)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-4	-	4	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} , $V_{I/O}$= V_{SS} to V_{CC} , $\overline{WE}$=V_{IL}	-4	-	4	µA
Average Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	-	100	mA
Standby Supply Current	I_{SB1}	$\overline{CS}$=V_{IH}, Min Cycle.	-	-	3	mA
-L Version	I_{SB2}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	-	400	uA
Output Voltage	V_{OL}	I_{OL}= 2.1 mA	-	-	0.4	V
	V_{OH}	I_{OH}= -1.0 mA	2.4	-	-	V

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Capacitance	C_{IN}	V_{IN} = 0V	-	-	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$= 0V	-	-	10	pF

Note: This parameter is not 100% tested.

Operating Modes

The table below shows the logic inputs required to control the MSM832 SRAM.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	V_{CC} *Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	I_{SB1},I_{SB2}	High Z	Power Down
OutputDisable	0	1	1	I_{CC}	High Z	
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	X	0	I_{CC}	D_{IN}	Write Cycle

1 = V_{IH}, 0 = V_{IL}, X = Don't Care

Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

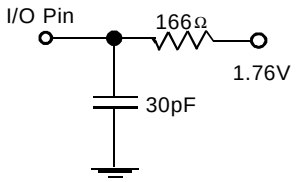
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}\geq V_{CC}$-0.2V, $V_{IN}\geq$0V	2.0	-	-	V
Data Retention Current -L Version	I_{CCDR2}	V_{CC}=3.0V, $\overline{CS}\geq V_{CC}$-0.2V, $V_{IN}\geq$0V	-	-	600	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC} (1)	-	-	ns

Notes (1) t_{RC} = Read Cycle Time

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 3ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{cc}=5V±10%

Output Load



AC OPERATING CONDITIONS

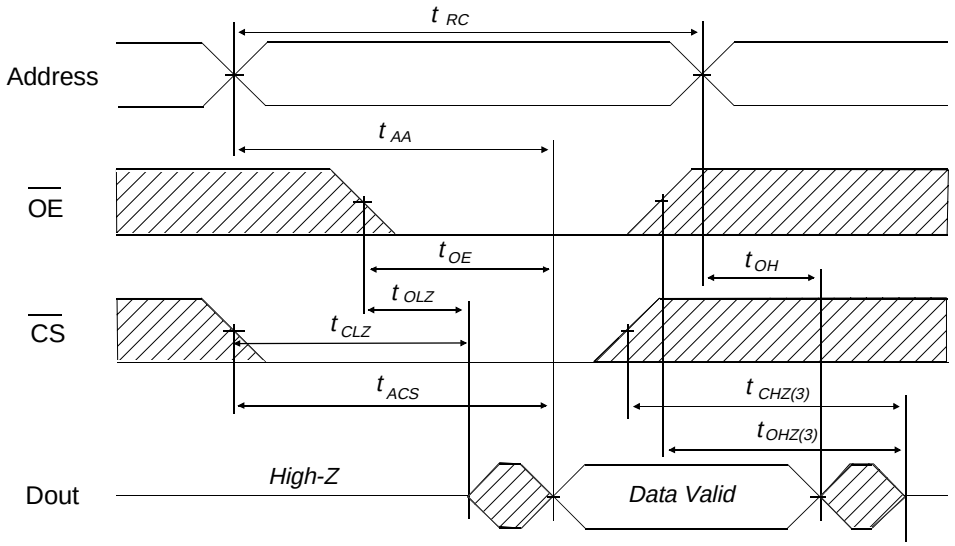
Read Cycle

Parameter	Symbol	70 min	70 max	85 min	85 max	10 min	10 max	Unit
Read Cycle Time	t_{RC}	70	-	85	-	100	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	ns
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	ns
Output Enable to Output Valid	t_{OE}	-	40	-	45	-	50	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	5	-	5	-	ns
Chip Deselection to Output in High Z(3)	t_{CHZ}	0	35	0	35	0	45	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	35	0	35	0	45	ns

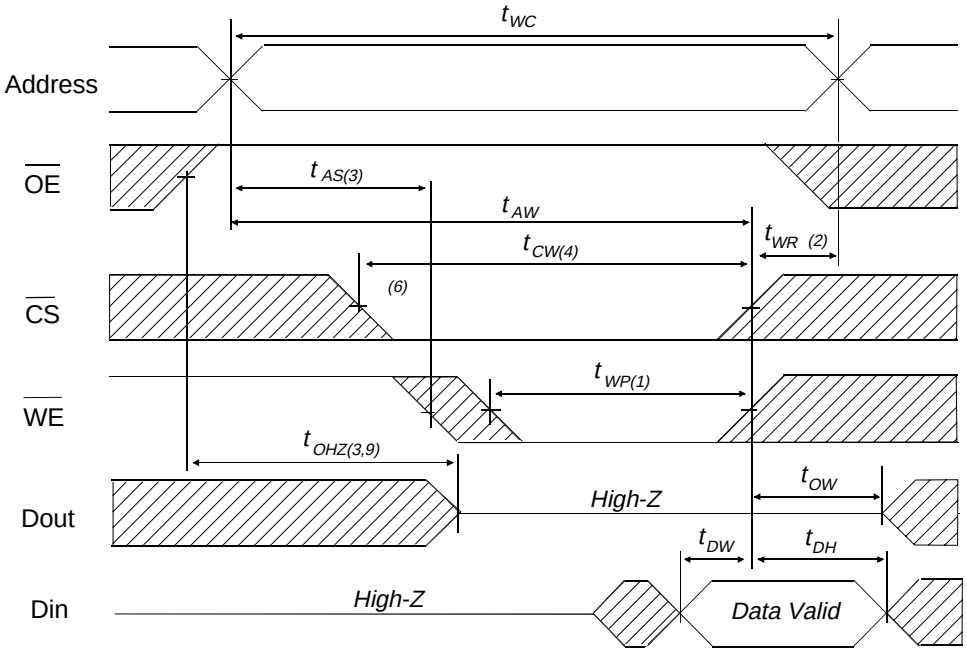
Write Cycle

Parameter	Symbol	70 min.	70 max	85 min.	85 max	10 min	10 max	Unit
Write Cycle Time	t_{WC}	70	-	85	-	100	-	ns
Chip Selection to End of Write	t_{CW}	65	-	75	-	80	-	ns
Address Valid to End of Write	t_{AW}	65	-	75	-	80	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	60	-	60	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	30	0	30	0	35	ns
Data to Write Time Overlap	t_{DW}	40	-	40	-	40	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	25	0	30	0	35	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

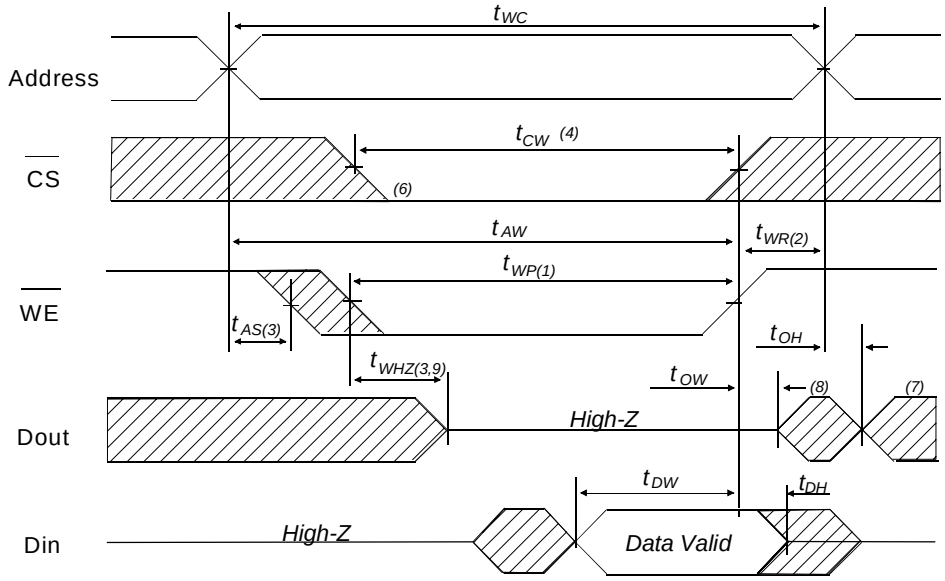
Read Cycle Timing Waveform (1)



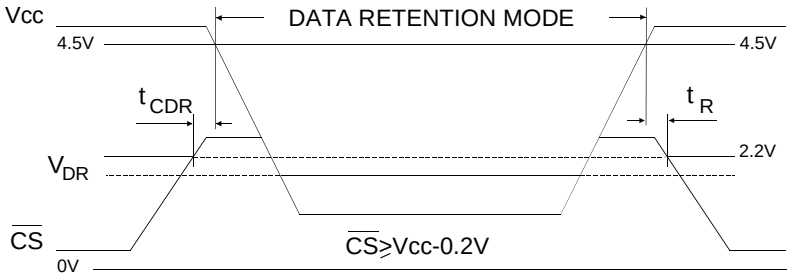
Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



Data Retention Waveform



AC Write Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

(6) Dout is in the same phase as written data of this write cycle.

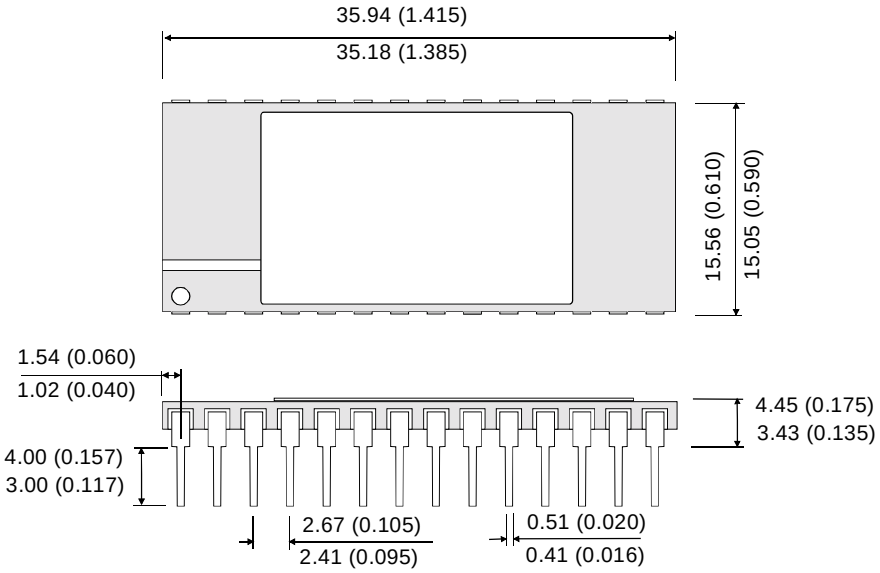
(7) Dout is the read data of next address.

(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

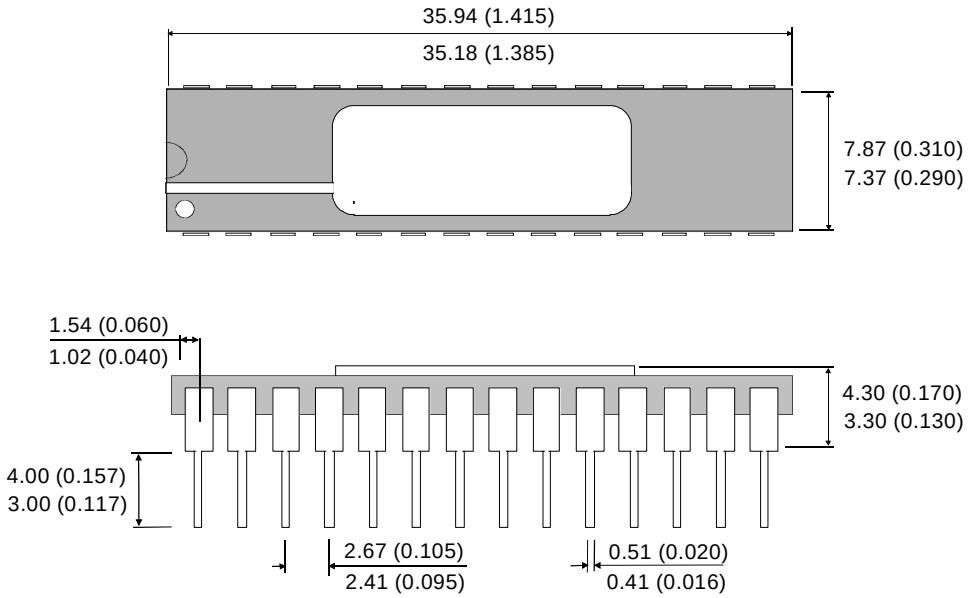
(9) t_{WHZ} and t_{OHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

PACKAGE DETAILS dimensions in mm (inches)

28 pin 0.6" Dual-In-Line (DIL) - 'S' Package



28 pin 0.3" Dual-in-Line (SKINNY) - 'T' Package



SCREENING

Military Screening Procedure

The Component Screening Flow for high reliability parts in accordance with Mil-883 method 5004 is shown below:

MB COMPONENT SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65˚C to +150˚C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25˚C	100%
Burn-in	Method 1015,Condition D,T_A=+125˚C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25˚C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

ORDERING INFORMATION

MSM832SLMB - 85

Speed	70	= 70 ns
	85	= 85 ns
	10	= 100 ns
Temp. range/screening	Blank	= Commercial
	I	= Industrial
	M	= Military
	MB	= Screened in accordance with MIL-STD-883
Power Option	Blank	= Standard Power
	L	= Low Power
Package		
	T	= 28 pin 0.3" SKINNY DIP
	S	= 28 pin 0.6" DIL
Memory Organisation	832	= 32K x 8 SRAM