MOTOROLA

Military 54F160A

Advance Information

Synchronous 4-Bit Decade Counter (Asynchronous Master Reset)

ELECTRICALLY TESTED PER:
MIL-M-38510/34401

The 54F160A and 54F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for applications in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 54F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 54F162A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 54F160A and 54F162A are high-speed versions of the 54F160 and F162.

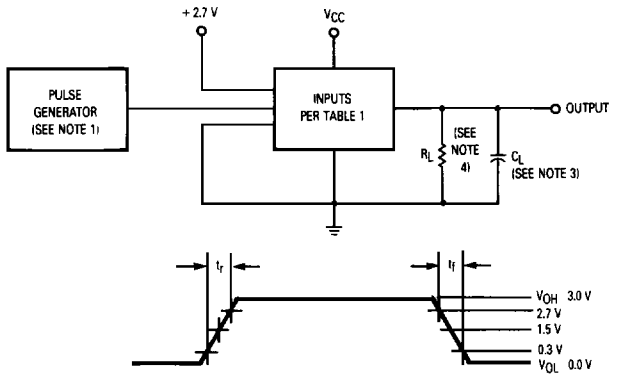
- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz

AVAILABLE AS:

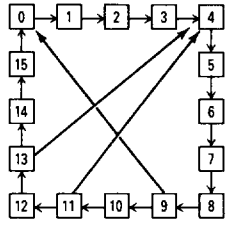
1) JAN: *
2) SMD: *
3) 883C: *

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

TEST CIRCUIT AND WAVEFORMS



STATE DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{MR}$	1	1	2	GND
CP	2	2	3	V_{CC}
P_0	3	3	4	V_{CC}
P_1	4	4	5	V_{CC}
P_2	5	5	7	V_{CC}
P_3	6	6	8	V_{CC}
CEP	7	7	9	V_{CC}
GND	8	8	10	GND
$\overline{PE}$	9	9	12	V_{CC}
CET	10	10	13	V_{CC}
Q_3	11	11	14	OPEN
Q_2	12	12	15	OPEN
Q_1	13	13	17	OPEN
Q_0	14	14	18	OPEN
TC	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

MR	PE	CET	CEP	Action on the Rising Clock Edge (⌐¬)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P_n–Q_n)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION

The 54F160A and 54F162A count modulo 10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 54F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (54F160A), synchronous reset (54F162A), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, 54F160A), Synchronous Reset ($\overline{SR}$, 54F162A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (54F160A) or $\overline{SR}$ (54F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

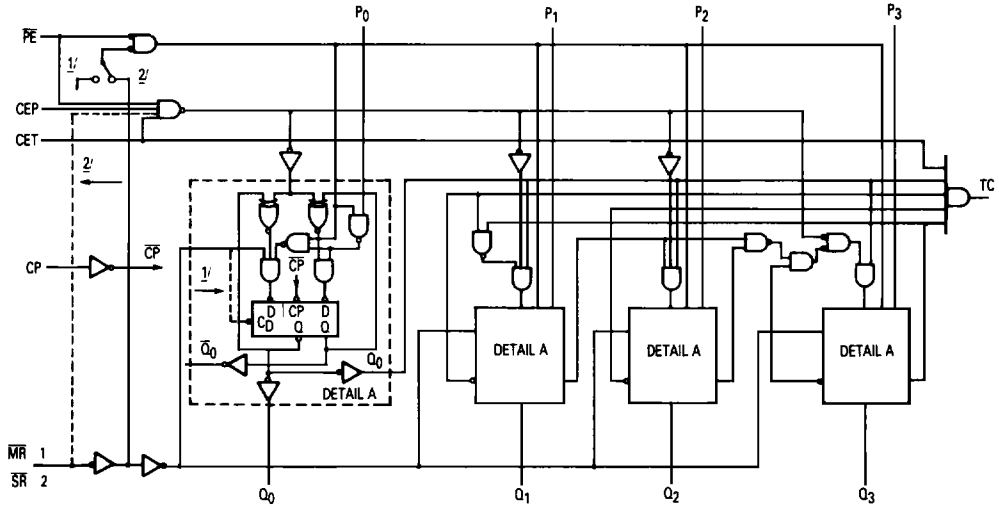
The 54F160A and 54F162A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 54F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 54F160A and 54F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$

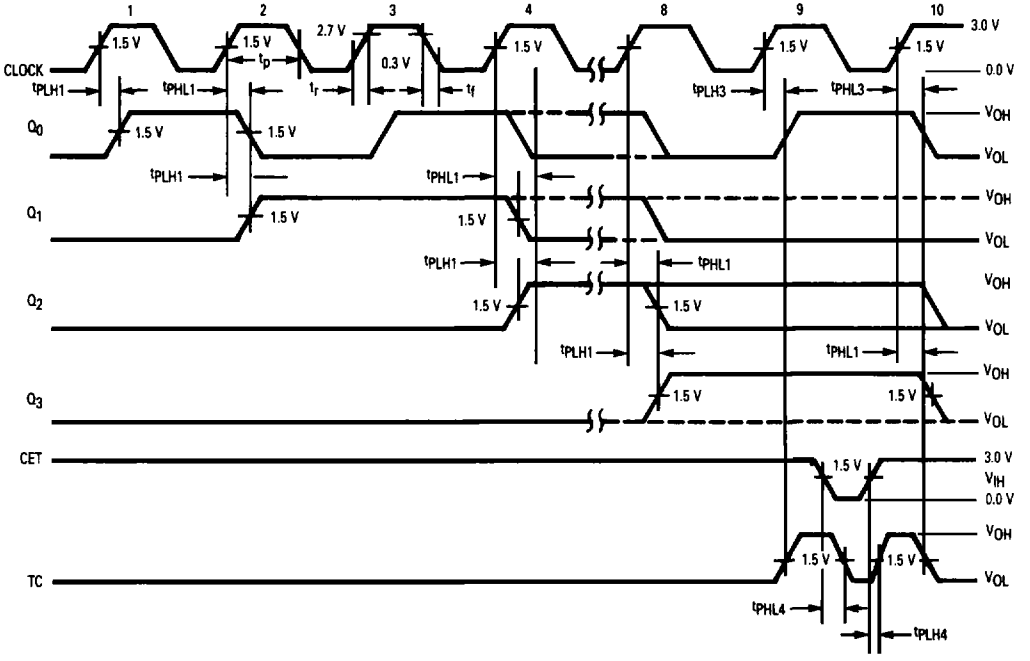
$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

LOGIC DIAGRAM



NOTES:
1 for F160A
2 for F162A

VOLTAGE WAVEFORMS



NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{out} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. C_L = 50 pF $\pm$ 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. R_L = 499 $\Omega \pm$ 5.0%.
5. Voltage measurements are to be made with respect to network ground terminal.

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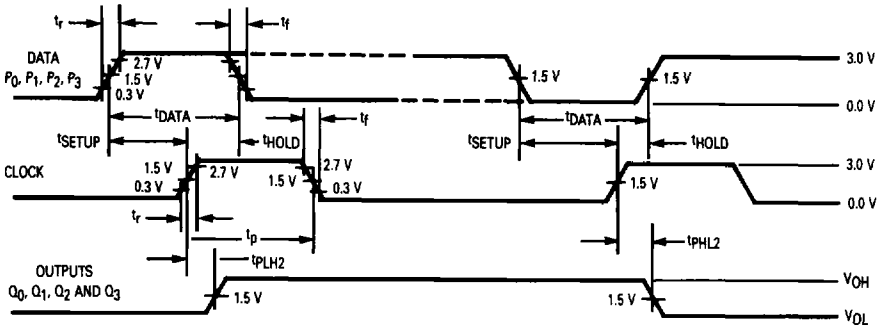
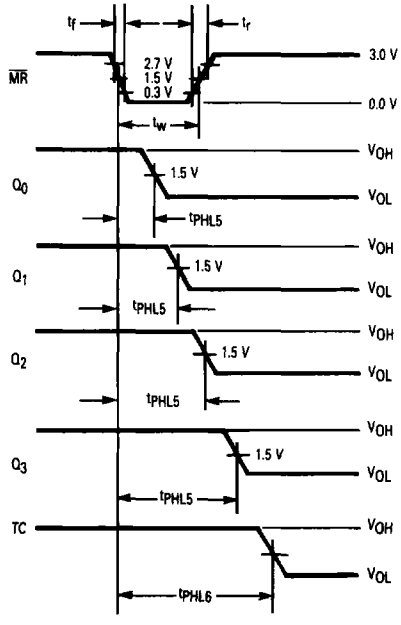
WAVEFORMS



NOTE:
The data pulse generator has the following characteristics:
V_{GEN} = 3.0 V, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, t_{DATA} = 7.0 ns, t_{SETUP} = 5.0 ns, t_{HOLD} = 2.0 ns.



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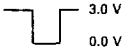
Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, $\overline{PE}$ = 0.8 V, $\overline{MR}$ & CP = (See Note 1), CET = 5.5 V or 2.0 V, CEP = 5.5 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, $\overline{PE}$ = 0.8 V, $\overline{MR}$ = (See Note 1) or 5.5 V, CEP = 5.5 V, CET = 0.8 V or 5.5 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs = 5.5 V.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, $\overline{PE}$ = 5.5 V, 0 V or (2.7 V), CEP & CET = 0 V or (2.7 V), other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, $\overline{PE}$ = open, 0 V or (7.0 V), other inputs are open.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, $\overline{PE}$ & CET = open or (5.5 V), other inputs are open.
I_{IL}	Logical "0" Input Current	−0.5	−1.2	−0.5	−1.2	−0.5	−1.2	mA	V_{CC} = 5.5 V, V_{IN} (CET & $\overline{PE}$) = 5.5 V, other inputs are open.
I_{OS}	Short Circuit Output Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V or open, V_{OUT} = 0 V, $\overline{PE}$ = 0 V, CEP & CET = 5.5 V, $\overline{MR}$ & CP = (See Note 1).
I_{CC}	Power Supply Current Off		55		55		55	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 4.5 V, **(Repeat at)**, V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

NOTE:

1. Apply 

Before measurement

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q_n	3.5	10	3.5	11.5	3.5	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output CP to Q_n	3.5	7.5	3.5	9.0	3.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output CP to Q_n	3.5	8.5	3.0	10	3.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CP to Q_n	3.5	8.5	3.0	10	3.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output CP to TC	4.5	14	4.0	15.5	4.0	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output CP to TC	4.5	14	4.0	16.5	4.0	16.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output CET to TC	2.5	7.5	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output CET to TC	2.5	7.5	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output $\overline{MR}$ to Q_n	5.5	12.5	5.5	14	5.5	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{MR}$ to TC	4.5	10.5	4.5	12.5	4.5	12.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
f_{MAX}	Maximum Clock Frequency	90		70		70		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

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