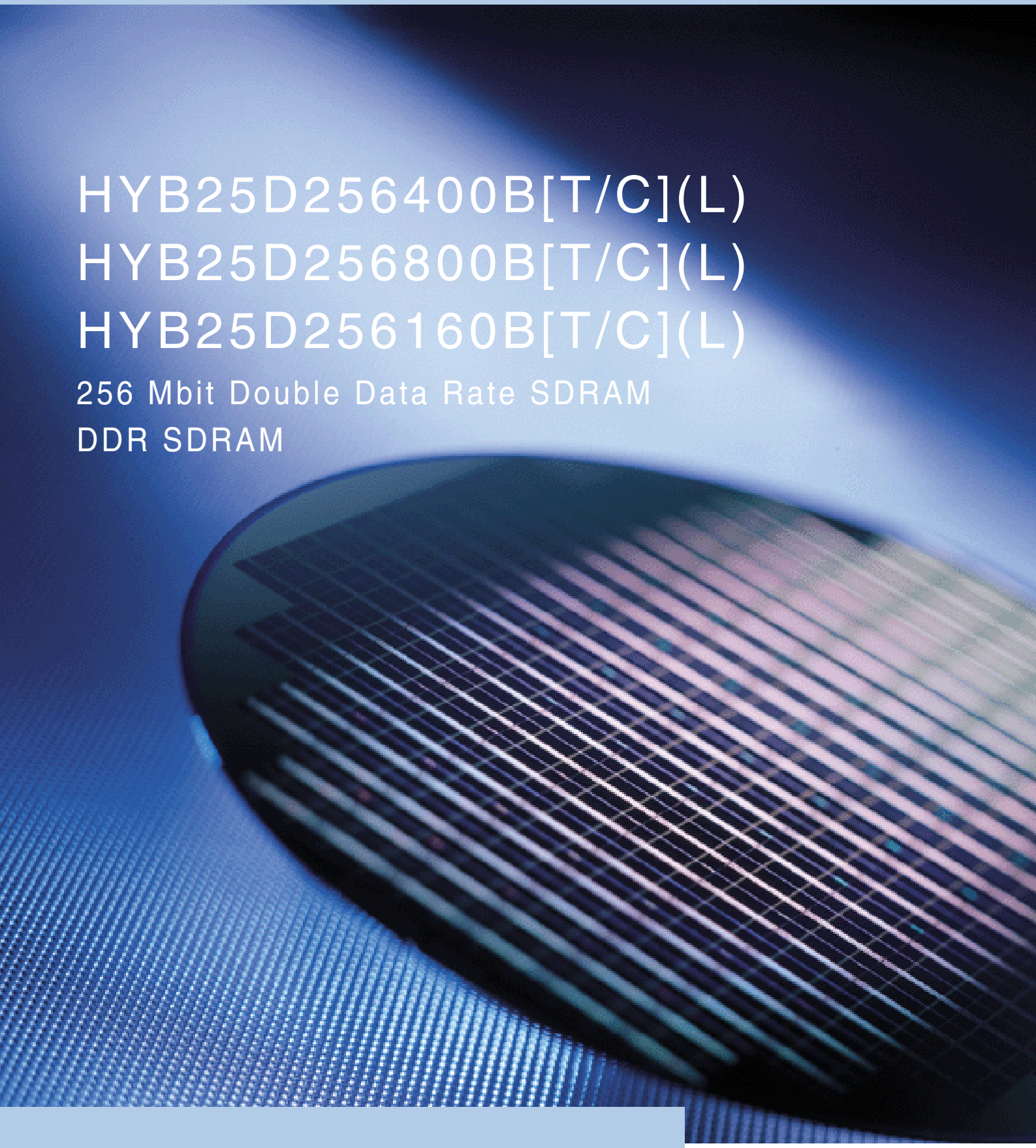
HYB25D256400B[T/C](L)
HYB25D256800B[T/C](L)
HYB25D256160B[T/C](L)

256 Mbit Double Data Rate SDRAM
DDR SDRAM



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Edition 2004-07

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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Revision History:	**Rev. 1.21**	**2004-07**
Previous Version:	Rev. 1.2	2004-02

Page	Subjects (major changes since last revision)
61,**63**	changed tDQSSmin to 1.25 and tDQSSmax 0.75

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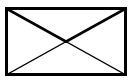


1 Overview

1.1 Features

- Double data rate architecture: two data transfers per clock cycle.
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver.
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst Lengths: 2, 4, or 8
- CAS Latency: 2, 2.5, 3
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 7.8 µs Maximum Average Periodic Refresh Interval (8K refresh)
- 2.5V (SSTL_2 compatible) I/O
- V_{DDQ} = 2.5 V ± 0.2 V (DDR200, DDR266, DDR333); V_{DDQ} = 2.6 V ± 0.1 V (DDR400)
- V_{DD} = 2.5 V ± 0.2 V (DDR200, DDR266, DDR333); V_{DD} = 2.6 V ± 0.1 V (DDR400)
- P-TSOPII-66-1 package
- P-TFBGA-60-2 package with 3 depopulated rows (12 mm × 8 mm^2).

Table 1 Performance

Part Number Speed Code			-5	–6	-7F	–7	–8	Unit
Speed Grade	Component		DDR400B	DDR333B	DDR266	DDR266A	DDR200	—
	Module		PC3200-3033	PC2700–2533	PC2100-2022	PC2100-2033	PC1600-2022	—
max. Clock Frequency	@CL3	f_{CK3}	200	166	–	–	–	MHz
	@CL2.5	$f_{CK2.5}$	166	166	143	143	125	MHz
	@CL2	f_{CK2}	133	133	133	133	100	MHz

Table 2

1.2 Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single $2n$-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 256Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Table 3 Ordering Information

Part Number [1)]	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25D256800BT(L)-5	x8	3 - 3 - 3	200	2.5 - 3 - 3	166	DDR400B	P-TSOPII-66-1
HYB25D256160BT(L)-5	×16	2.5 - 3 - 3	166	2 - 3 - 3	133	DDR333	
HYB25D256400BT(L)-6	×4						
HYB25D256800BT(L)-6	×8						
HYB25D256160BT(L)-6	×16						
HYB25D256400BT(L)-7	×4		143		133	DDR266A	
HYB25D256800BT(L)-7	×8						
HYB25D256160BT(L)-7	×16						
HYB25D256400BT(L)-7F	×4		143	2 - 2 - 2	133	DDR266	
HYB25D256800BT(L)-7F	×8						
HYB25D256160BT(L)-7F	×16						
HYB25D256400BT(L)-8	×4		125		100	DDR200	
HYB25D256800BT(L)-8	×8						
HYB25D256160BT(L)-8	×16						
HYB25D256400BC(L)-5	×4	3 - 3 - 3	200	2.5 - 3 - 3	166	DDR400B	P-TFBGA-60-2
HYB25D256400BC(L)-6	×4	2.5 - 3 - 3	166	2 - 3 - 3	133	DDR333	
HYB25D256800BC(L)-6	×8						
HYB25D256160BC(L)-6	×16						
HYB25D256400BC(L)-7	×4		143		133	DDR266A	
HYB25D256800BC(L)-7	×8						
HYB25D256160BC(L)-7	×16						
HYB25D256400BC(L)-7F	×4		143	2 - 2 - 2		DDR266	
HYB25D256800BC(L)-7F	×8						
HYB25D256160BC(L)-7F	×16						
HYB25D256400BC(L)-8	×4		125		100	DDR200	
HYB25D256800BC(L)-8	×8						
HYB25D256160BC(L)-8	×16						

1) HYB: designator for memory components, 25D: DDR-I SDRAMs at Vddq=2.5V, 256: 256Mb density, 400/800/160: Product variations x4, x8 and x16, B: Die revision B, C/T: Package type FBGA and TSOP, L: Low power version (optional) - these components are specifically selected for low IDD6 Self Refresh currents.

2 Pin Configuration

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

(x 4)

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

(x8)

1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VDDQ	DQ7
VREF	VSS	UDM	F	LDM	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

(x 16)

Figure 1 Pin Configuration P-TFBGA-60-2 (Top View - see the balls through the package)

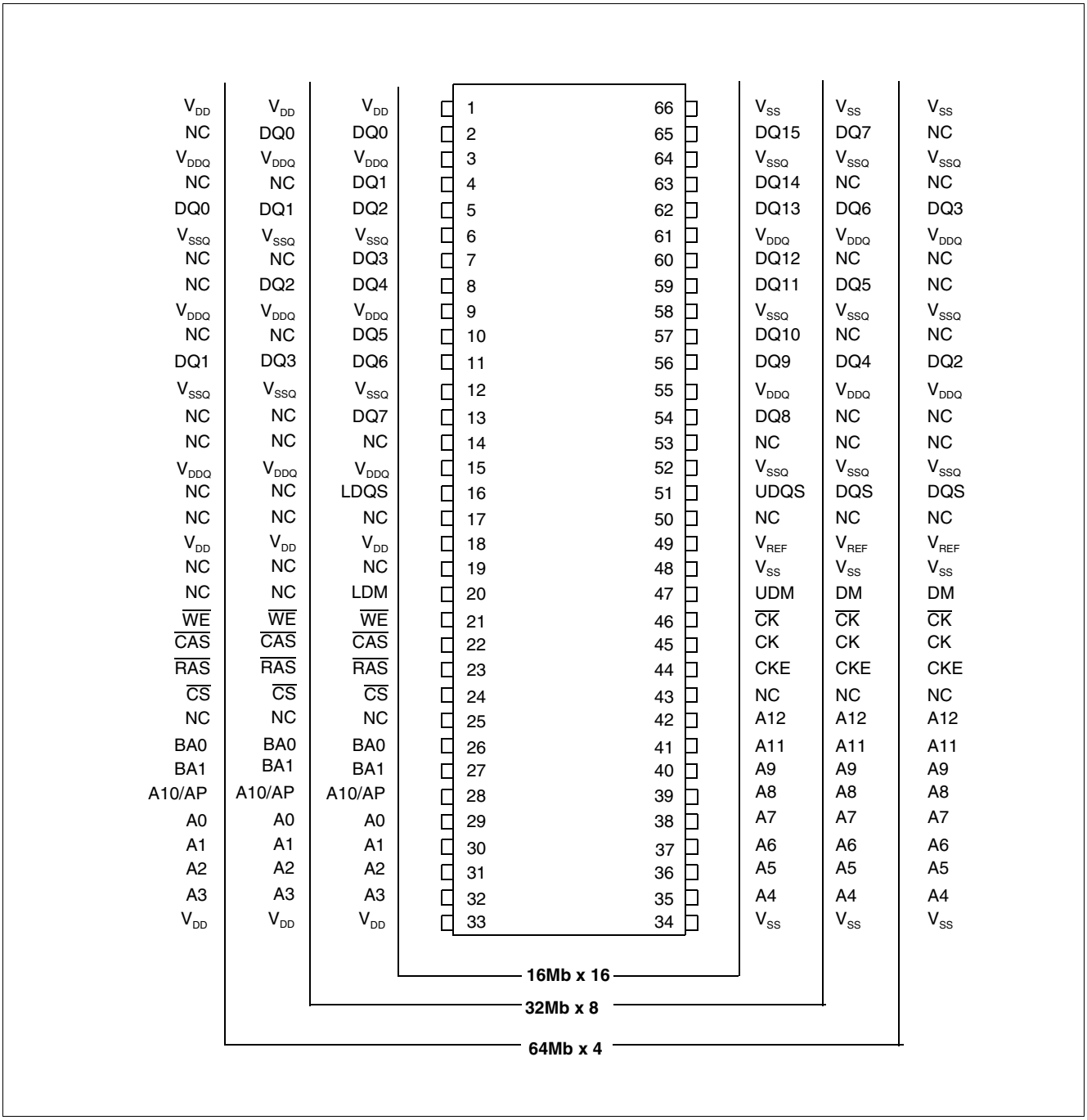


Figure 2 Pin Configuration P-TSOPII-66-1

Table 4 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 – A12	Input	**Address Inputs:** Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
DQ	Input/Output	**Data Input/Output:** Data bus.
DQS	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
NC	–	**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5 V ± 0.2 V/ 2.6V ± 0.1V.
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5 V ± 0.2 V / 2.6V ± 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage:** (V_{DDQ} / 2)

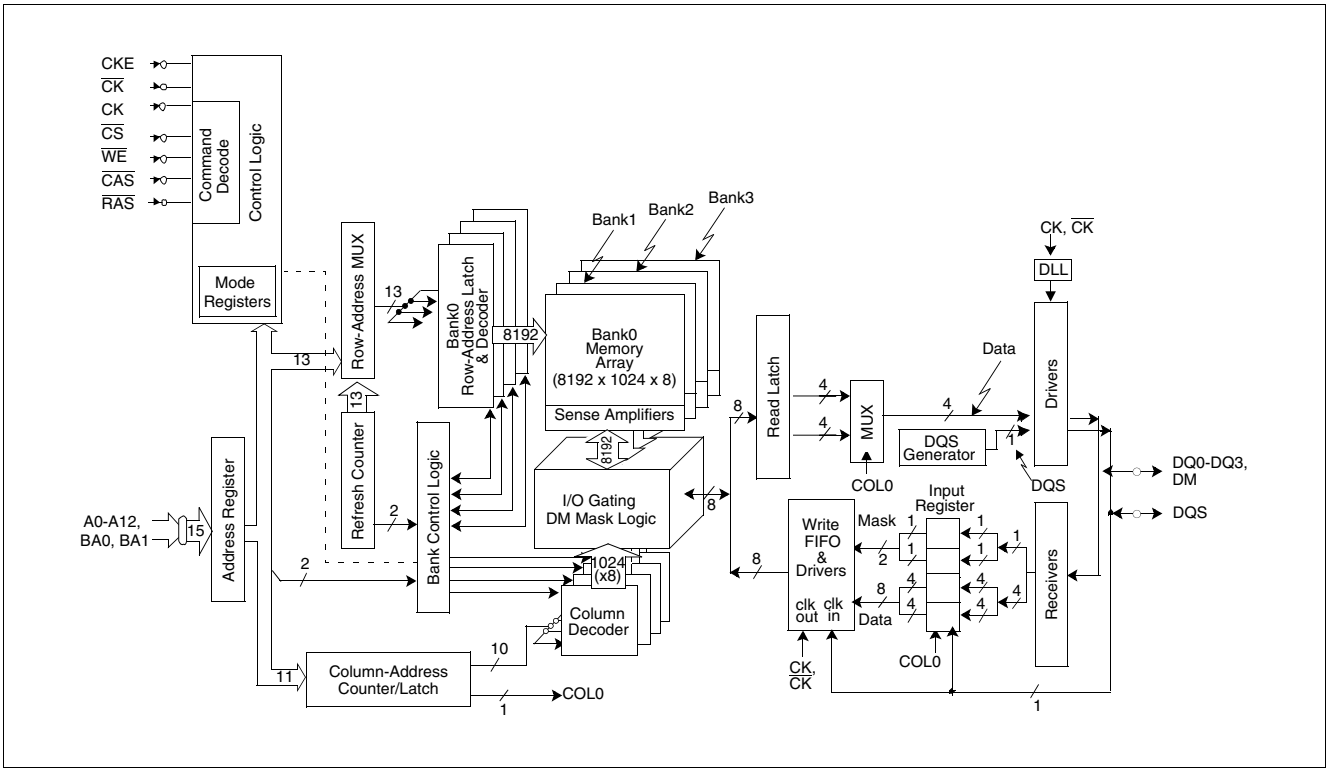


Figure 3 Block Diagram (64Mb × 4)

Notes:

1. *This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.*
2. *DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.*

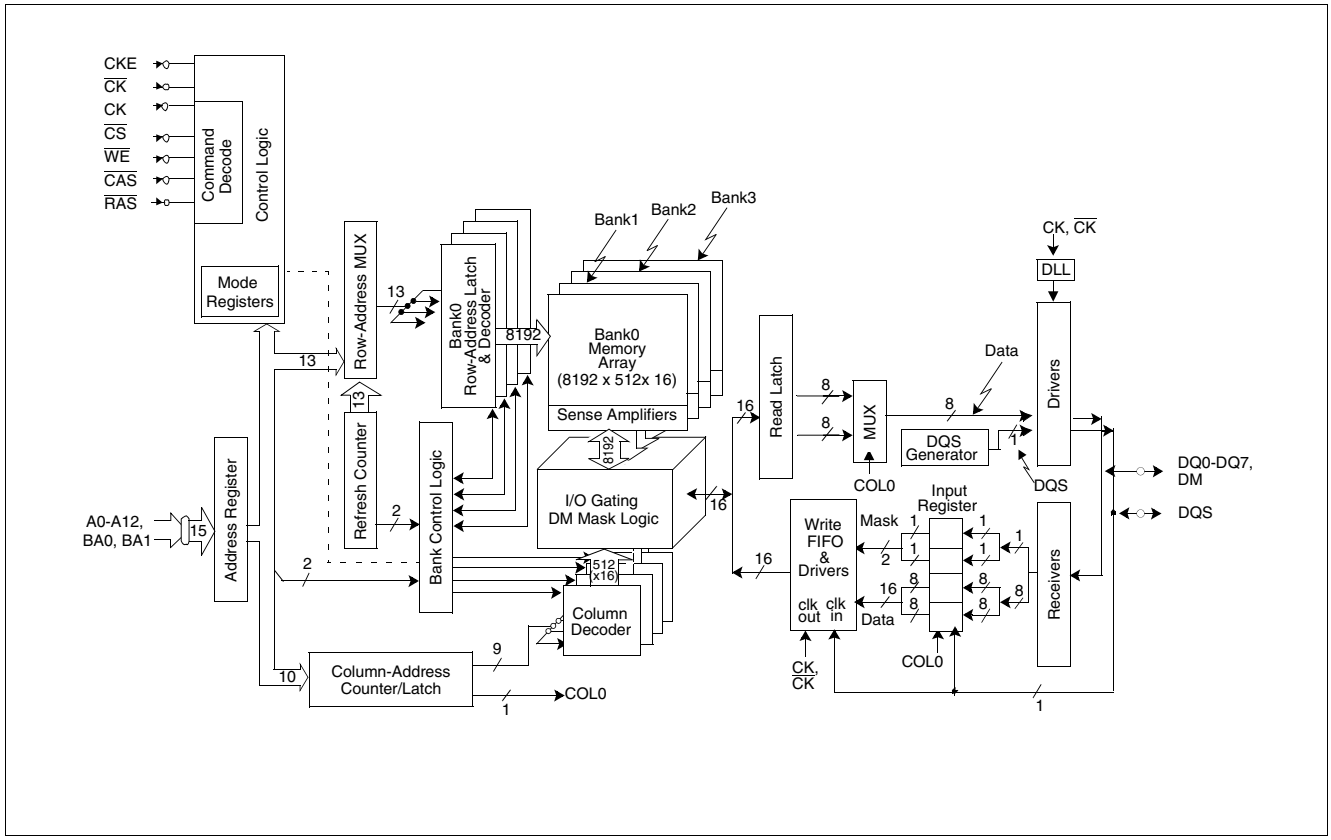


Figure 4 Block Diagram (32Mb × 8)

Notes:

1. *This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.*
2. *DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.*

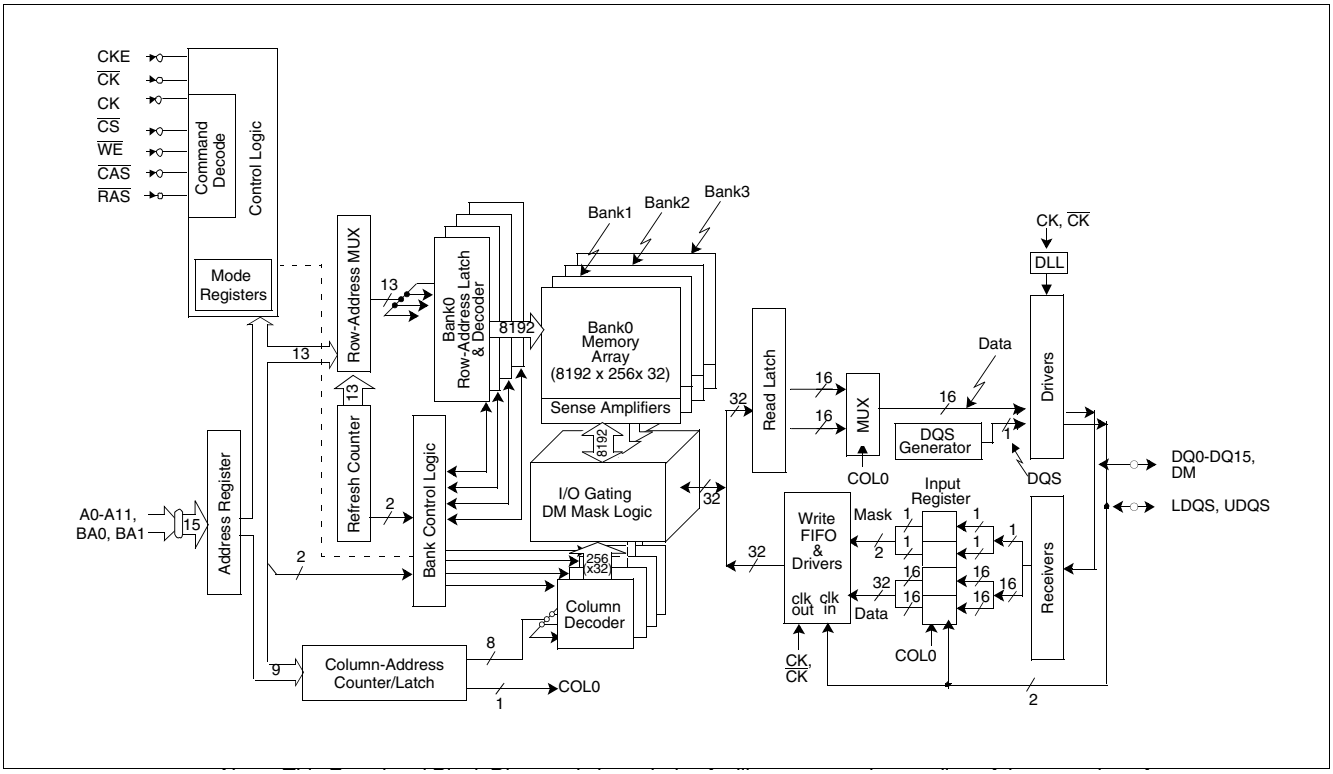


Figure 5 Block Diagram (16Mb × 16)

Notes:

1. *This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.*
2. *UDM and LDM are unidirectional signals (input only), but is internally loaded to match the load of the bidirectional DQ, UDQS and LDQS signals.*

3 Functional Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268, 435, 456 bits. The 256Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a $2n$ prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM consists of a single $2n$-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

3.1 Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following criteria must be met:

No power sequencing is specified during power up or power down given the following criteria:

- V_{DD} *and* V_{DDQ} *are driven from a single power converter output*
- V_{TT} *meets the specification*
- A minimum resistance of 42 Ω limits the input current from the V_{TT} supply into any pin and V_{REF} tracks $V_{DDQ}/2$ or the following relationship must be followed:
- V_{DDQ} *is driven after or with* V_{DD} *such that* $V_{DDQ} < V_{DD} + 0.3$ *V*
- V_{TT} *is driven after or with* V_{DDQ} *such that* $V_{TT} < V_{DDQ} + 0.3$ *V*
- V_{REF} *is driven after or with* V_{DDQ} *such that* $V_{REF} < V_{DDQ} + 0.3$ *V*

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a Deselect or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a Precharge ALL command should be applied. Next a Mode Register Set command should be issued for the Extended Mode Register, to enable the DLL, then a Mode Register Set command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. During the 200 cycles of clock for DLL locking, a Deselect or NOP command must be applied. After the 200 clock cycles, a Precharge ALL command should be applied, placing the device in the “all banks idle” state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

3.2 Mode Register Definition

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

MR
Mode Register Definition **(BA[1:0] = 00_B)**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**OPERATING MODE**						**CL**			**BT**	**BL**		
reg. addr		w						w			w	w		

Field	Bits	Type	Description
BL	[2:0]	w	**Burst Length** Number of sequential bits per DQ related to one read/write command; see **Chapter 3.2.1**. *Note: All other bit combinations are RESERVED.* 001 2 010 4 011 8
BT	3	w	**Burst Type** See **Table 5** for internal address sequence of low order address bits; see **Chapter 3.2.2**. 0 Sequential 1 Interleaved
CL	[6:4]	w	**CAS Latency** Number of full clocks from read command to first data valid window; see **Chapter 3.2.3**. *Note: All other bit combinations are RESERVED.* 010 2 011 (3.0 Optional, not covered by this data sheet) 101 2.5 110 1.5 for DDR200 components only
MODE	[12:3]	w	**Operating Mode** *Note: All other bit combinations are RESERVED.* 0 Normal Operation

3.2.1 Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

3.2.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 5**.

Table 5 Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. *For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.*
3. *For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*

3.2.3 Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2, 2.5 or 3 clocks. CAS latency of 1.5 is an optional feature on this device. If a Read command is registered at clock edge n, and the latency is *m* clocks, the data is available nominally coincident with clock edge n + m (see **Figure 6**). Reserved states should not be used as unknown operation or incompatibility with future versions may result.

3.2.4 Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

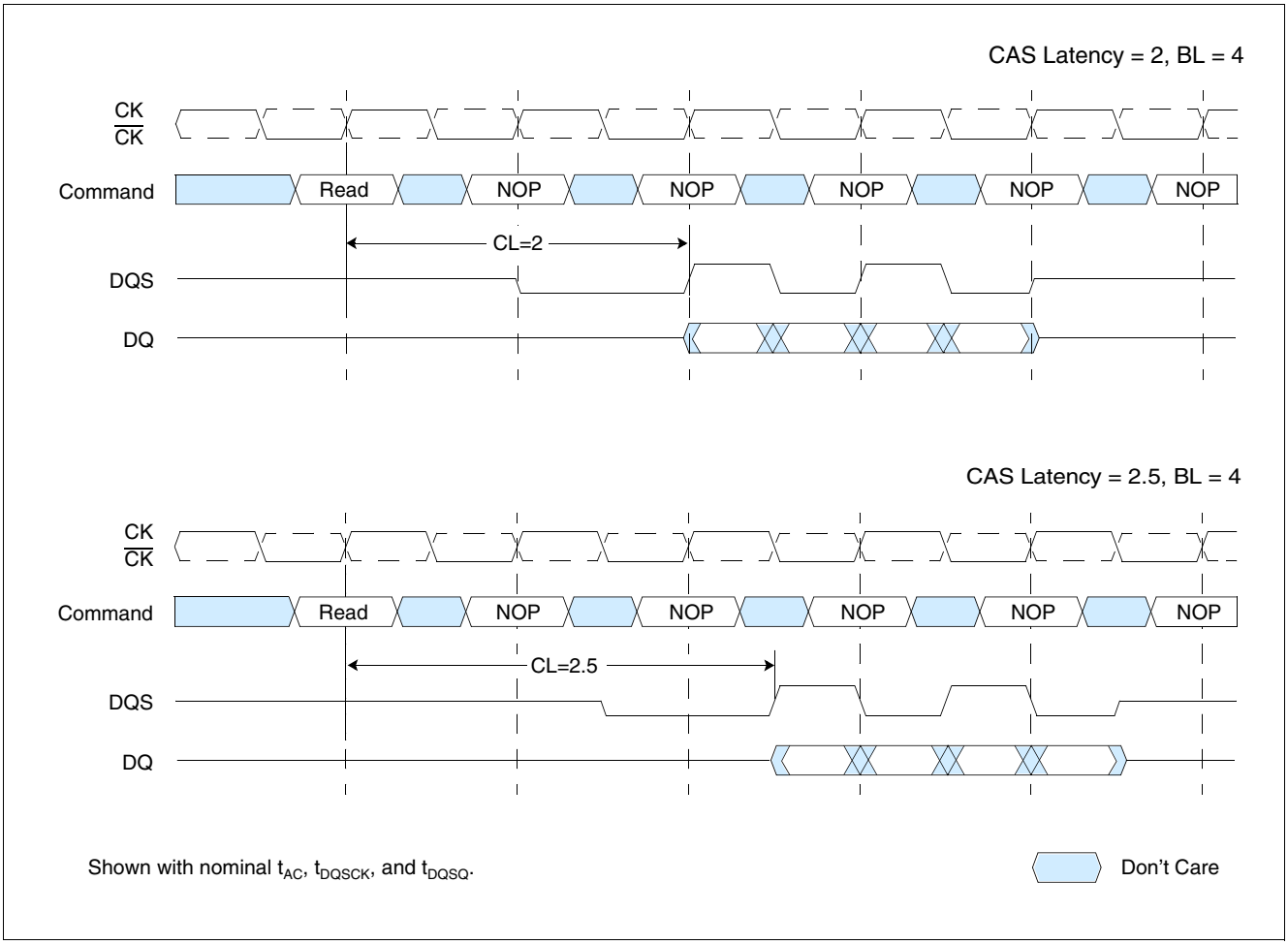


Figure 6 Required CAS Latencies

3.3 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, and output drive strength selection (optional). These functions are controlled via the bits shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

3.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur before a Read command can be issued. This is the reason 200 clock cycles must occur before issuing a Read or Write command upon exit of self refresh operation.

3.3.2 Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. In addition this design version supports a weak driver mode for lighter load and/or point-to-point environments which can be activated during mode register set. I-V curves for the normal and weak drive strength are included in this document.

EMR
Extended Mode Register Definition (BA[1:0] = 01_B)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**OPERATING MODE**										**0**	**DS**	**DLL**
reg. addr		w										w	w	w

Field	Bits	Type	Description
DLL	0	w	**DLL Status** See **Chapter 3.3.1**. 0 Enabled 1 Disabled
DS	1	w	**Drive Strength** See **Chapter 3.3.2**, **Chapter 4.2** and **Chapter 4.3**. 0 Normal 1 Weak
0	2	w	0 must be set to 0
MODE	[12:3]	w	**Operating Mode** *Note: All other bit combinations are RESERVED.* 0 Normal Operation

3.4 Commands

Deselect

The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to a DDR SDRAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set

The mode registers are loaded via inputs A0-A12, BA0 and BA1. See mode register descriptions in the Register Definition section. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 8, j = don't care] for × 16, [i = 9, j = don't care] for × 8 and [i = 9, j = 11] for × 4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for × 8; where [i = 9, j = 11] for × 4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge

The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge functions described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit Precharge command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

Burst Terminate

The Burst Terminate command is used to truncate read bursts (with Auto Precharge disabled). The most recently registered Read command prior to the Burst Terminate command is truncated, as shown in the Operation section of this data sheet.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to CAS Before RAS (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an Auto Refresh command. The 1 Gb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8 µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto Refresh commands can be posted in the system, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9 × 7.8 µs (70.2 µs). This maximum absolute interval is short enough to allow for DLL updates internal to the DDR SDRAM to be restricted to Auto Refresh cycles, without allowing too much drift in t_{AC} between updates.

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are “Don’t Care” during Self Refresh operation.

The procedure for exiting self refresh requires a sequence of commands. CK (and $\overline{CK}$) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Table 6 Truth Table 1a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (NOP)	H	X	X	X	X	NOP	1)9)
No Operation (NOP)	L	H	H	H	X	NOP	1)9)
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1)3)
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1)4)
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1)4)
Burst Terminate	L	H	H	L	X	BST	1)8)
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1)5)
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR/ SR	1)6)7)
Mode Register Set	L	L	L	L	Op-Code	MRS	1)2)

1) CKE is HIGH for all commands shown except Self Refresh.

2) Deselect and NOP are functionally interchangeable.

3) BA0-BA1 provide bank address and A0-A12 provide row address.

4) BA0, BA1 provide bank address; A0-Ai provide column address (where i = 8 for x16, i = 9 for x8 and 9, 11 for x4); A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.

5) Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts.

6) A10 LOW: BA0, BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care”.

7) This command is AUTO REFRESH if CKE is HIGH; Self Refresh if CKE is LOW.

8) Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.

9) BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register).

Table 7 Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data; provided coincident with the corresponding data.

3.5 Operations

3.5.1 Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the DDR SDRAM, a row in that bank must be “opened” (activated). This is accomplished via the Active command and addresses A0-A13, BA0 and BA1 (see **Figure 7**), which decode and select both the bank and the row to be activated. After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}. A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

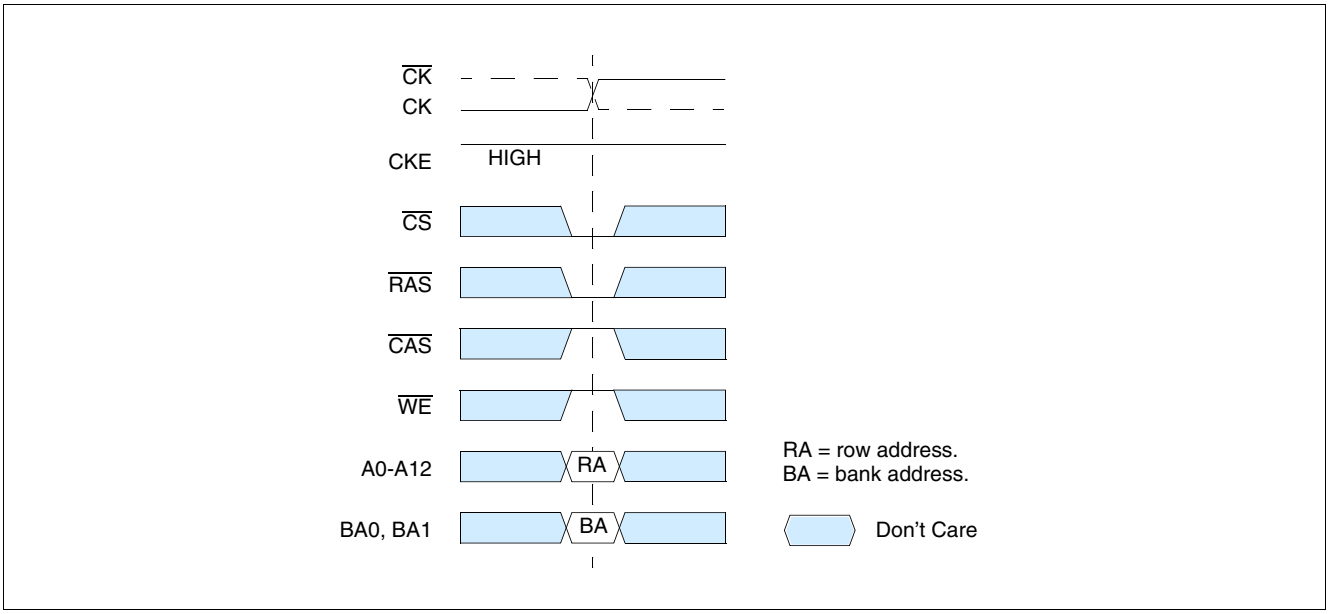


Figure 7 Activating a Specific Row in a Specific Bank

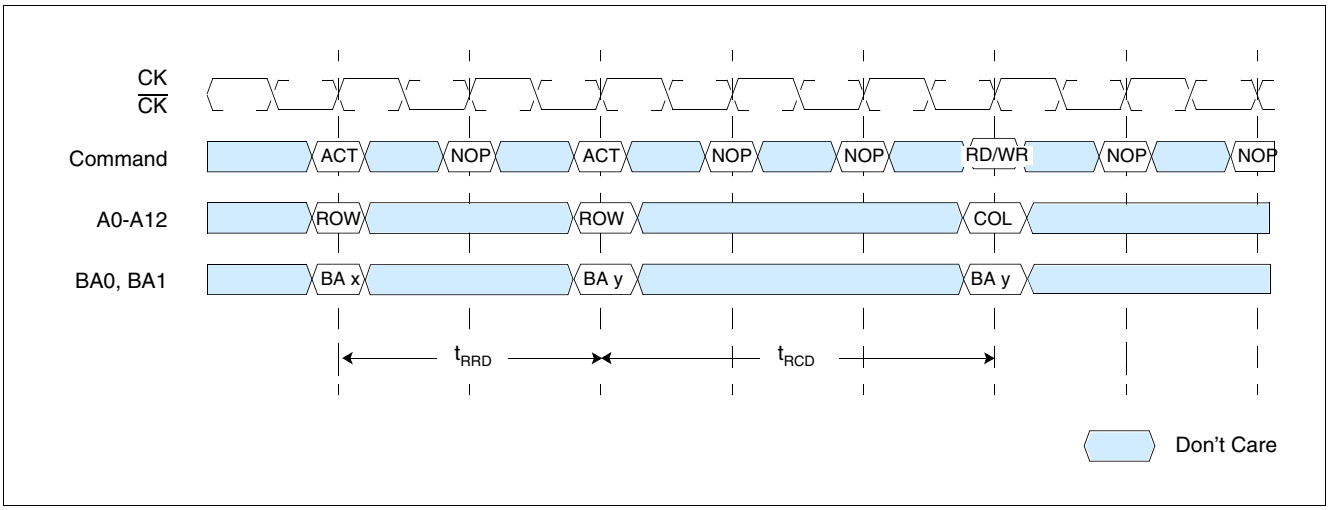


Figure 8 t_{RCD} and t_{RRD} Definition

3.5.2 Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command, as shown on **Figure 9 "Read Command" on Page 25**.

The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and $\overline{CK}$). **Figure 10 "Read Burst: CAS Latencies (Burst Length = 4)" on Page 26** shows general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble. Upon completion of a burst, assuming no other commands have been initiated, the DQs goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown on **Figure 11 "Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)" on Page 27**. A Read command can be initiated on any clock cycle following a previous Read command. Nonconsecutive Read data is illustrated on **Figure 12 "Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)" on Page 28**. Full-speed **Figure 13 "Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)" on Page 29** within a page (or pages) can be performed as shown on **Figure 13**.

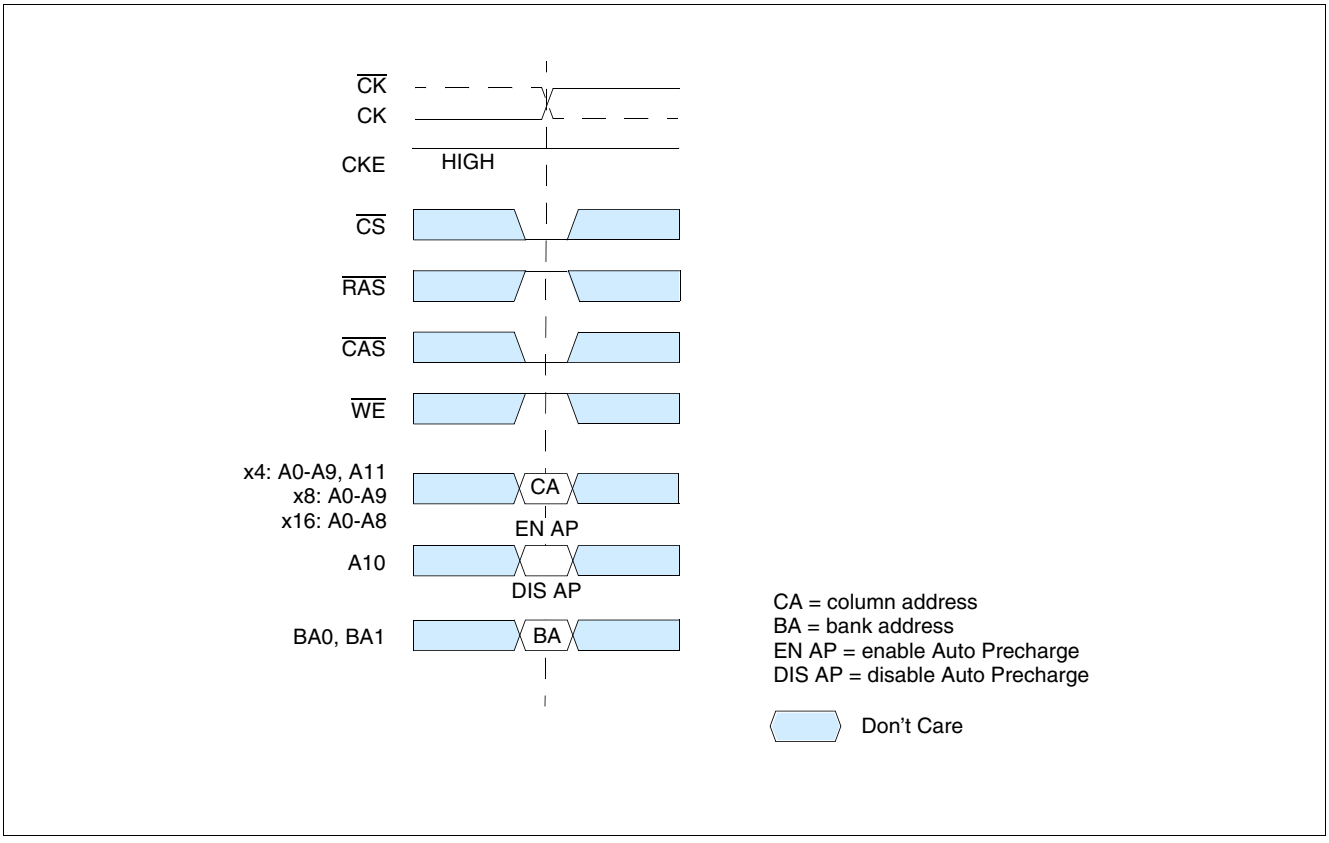
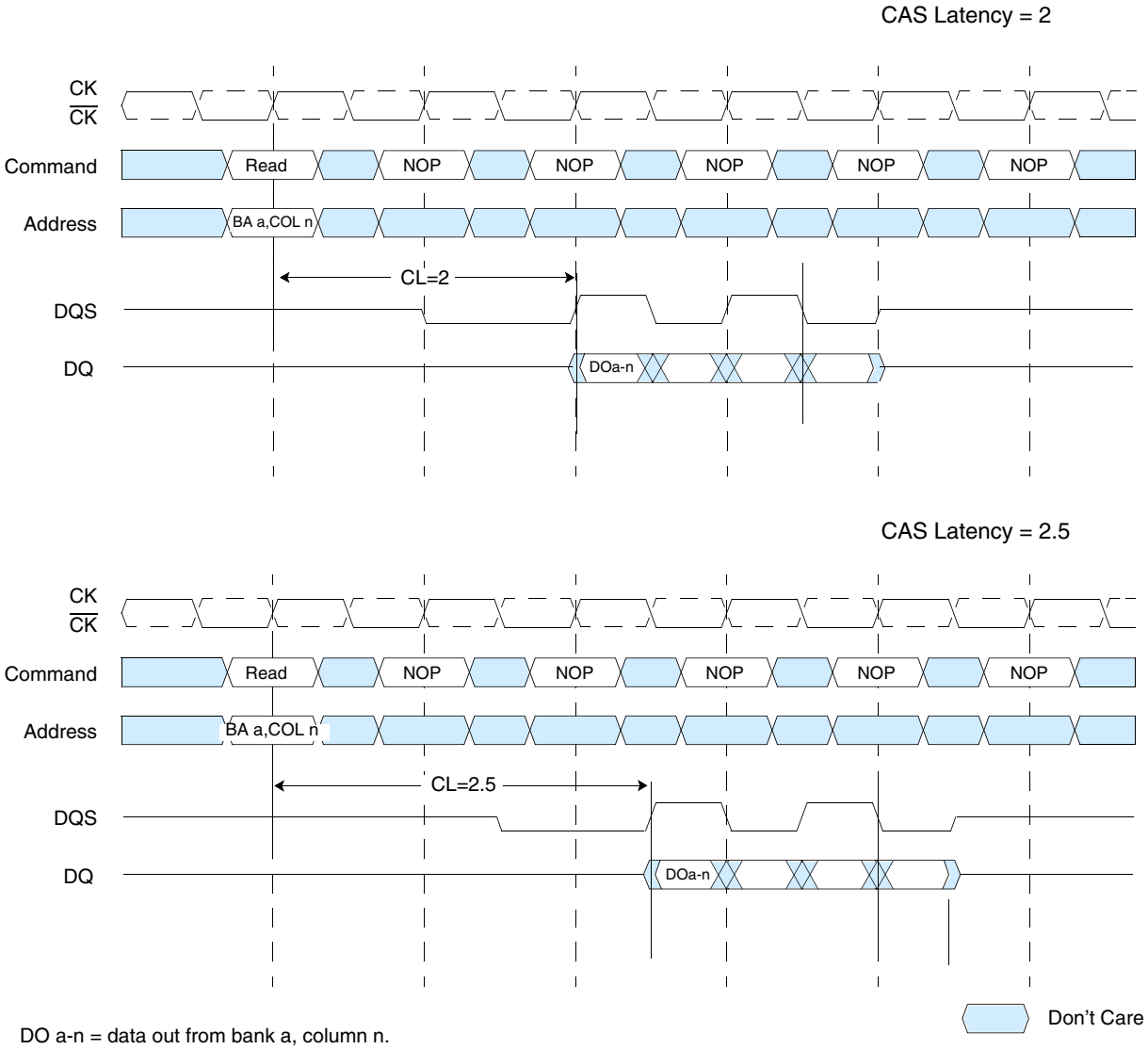
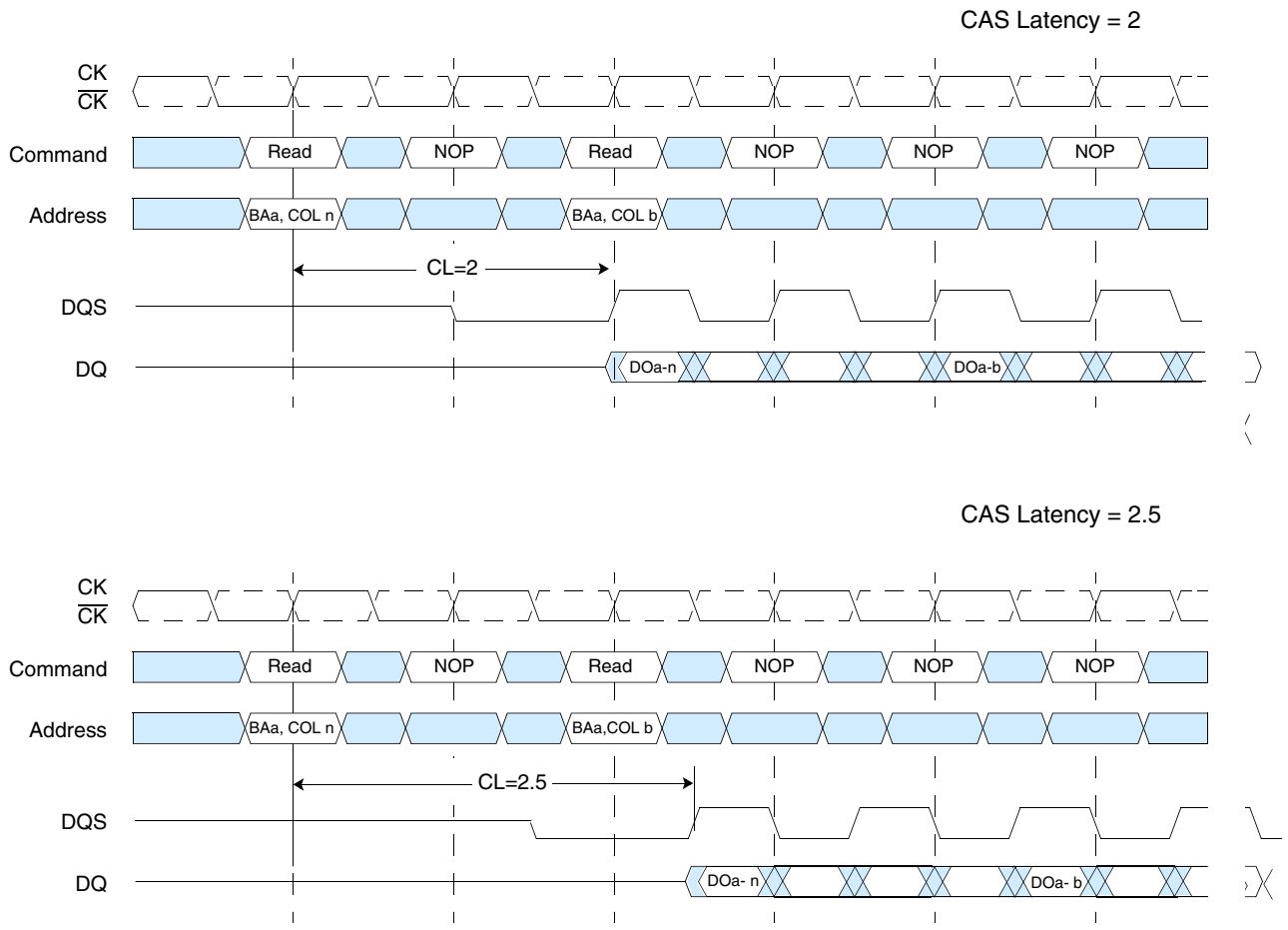


Figure 9 Read Command



DO a-n = data out from bank a, column n.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Figure 10 Read Burst: CAS Latencies (Burst Length = 4)



DO a-n (or a-b) = data out from bank a, column n (or bank a, column b).
When burst length = 4, the bursts are concatenated.
When burst length = 8, the second burst interrupts the first.
3 subsequent elements of data out appear in the programmed order following DO a-n.
3 (or 7) subsequent elements of data out appear in the programmed order following DO a-b.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Figure 11 Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)

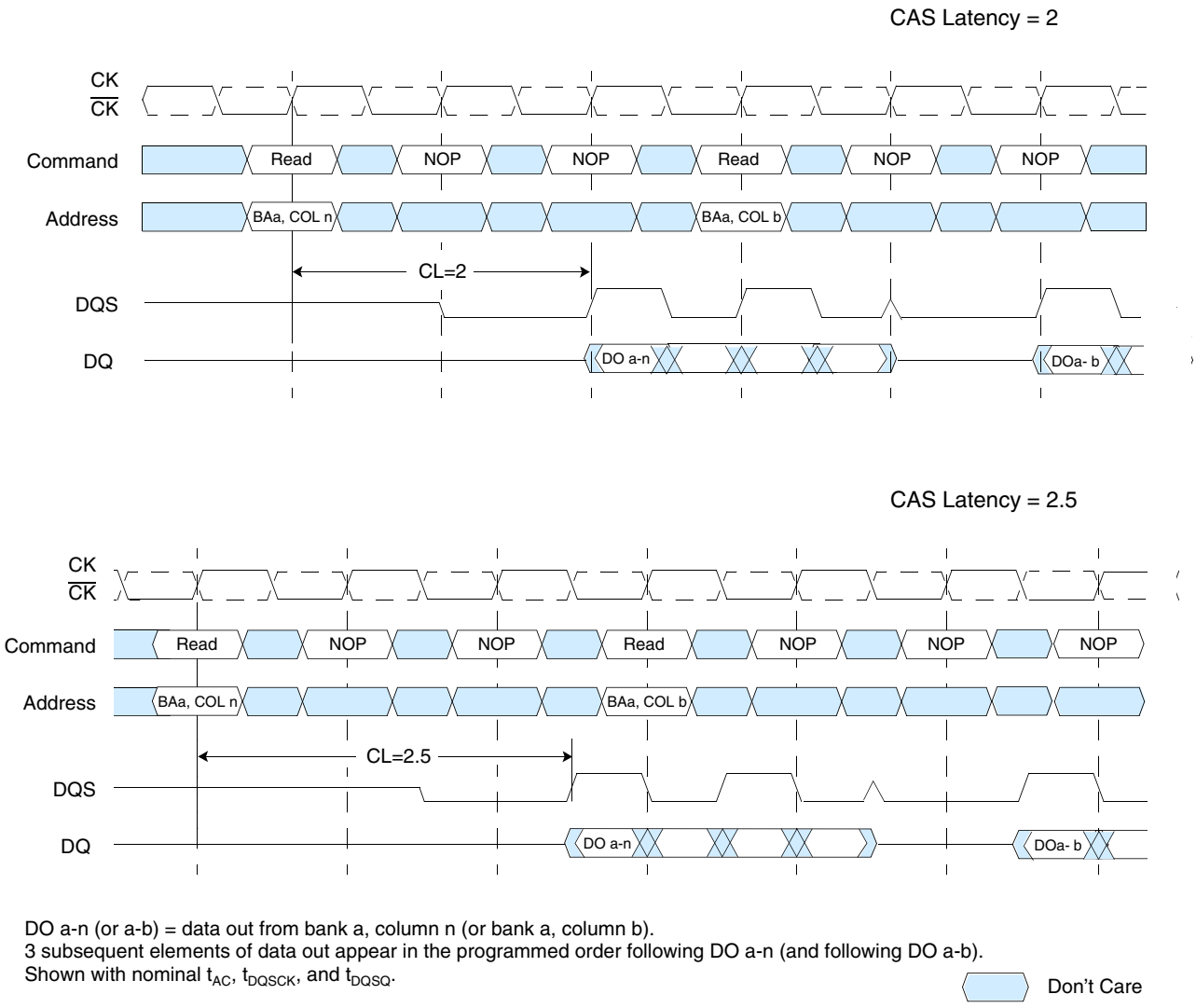


Figure 12 Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)

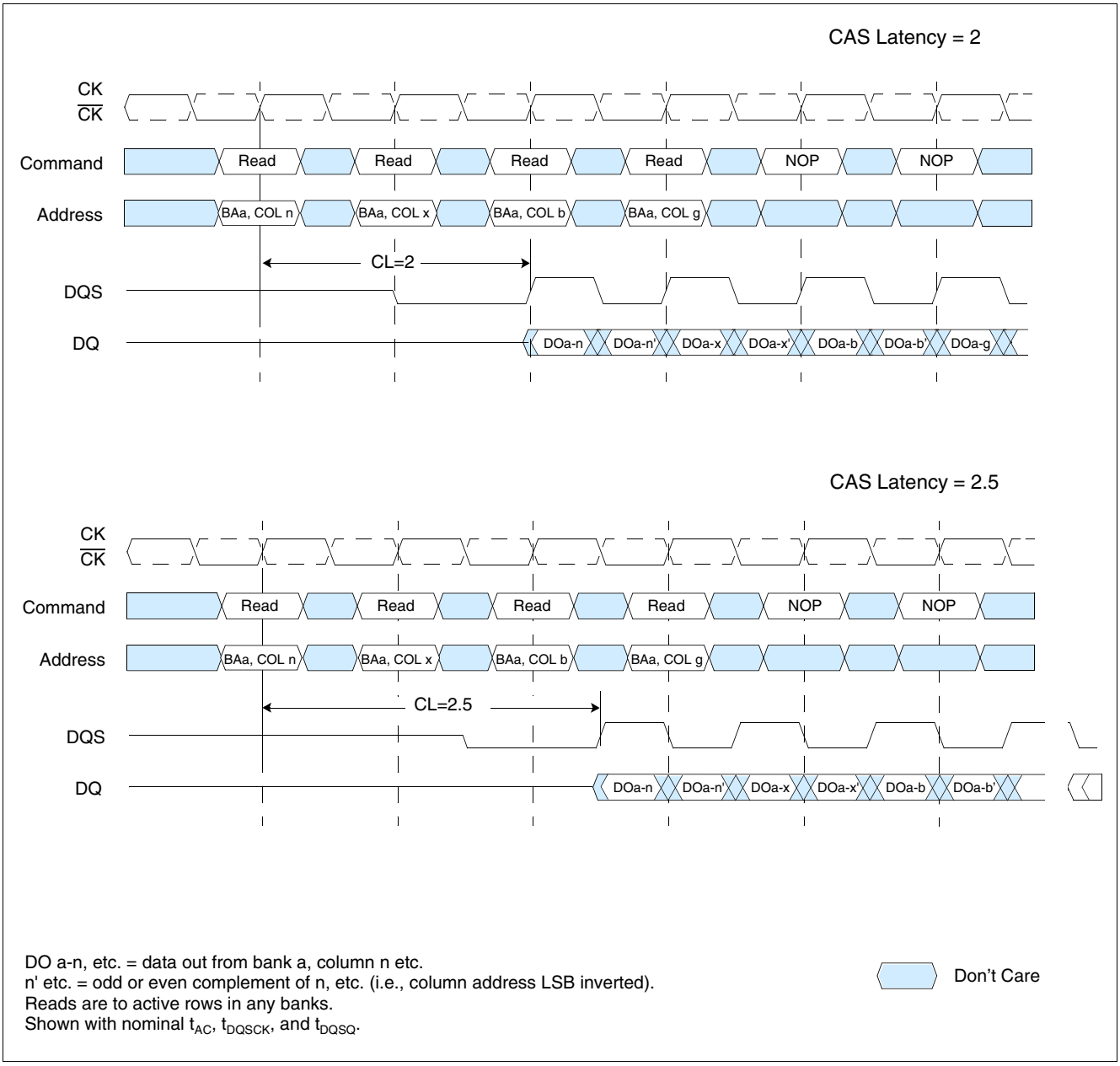


Figure 13 Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)

Data from any Read burst may be truncated with a Burst Terminate command, as shown on **Figure 14 "Terminating a Read Burst: CAS Latencies (Burst Length = 8)" on Page 30**. The Burst Terminate latency is equal to the read (CAS) latency, i.e. the Burst Terminate command should be issued x cycles after the Read command, where x equals the number of desired data element pairs.

Data from any Read burst must be completed or truncated before a subsequent Write command can be issued. If truncation is necessary, the Burst Terminate command must be used, as shown on **Figure 15 "Read to Write: CAS Latencies (Burst Length = 4 or 8)" on Page 31**. The example is shown for t_{DQSS} (min). The t_{DQSS} (max) case, not shown here, has a longer bus idle time. t_{DQSS} (min) and t_{DQSS} (max) are defined in the section on Writes.

A Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that Auto Precharge was not activated). The Precharge command should be issued x cycles after the Read command, where x equals the number of desired data element pairs (pairs are required by the *2n* prefetch architecture). This is shown on **Figure 16 "Read to Precharge: CAS Latencies (Burst Length = 4 or 8)" on Page 32** for Read latencies of 2 and 2.5. Following the Precharge command, a subsequent command to the same bank cannot be

issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a Read being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same Read burst with Auto Precharge enabled. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

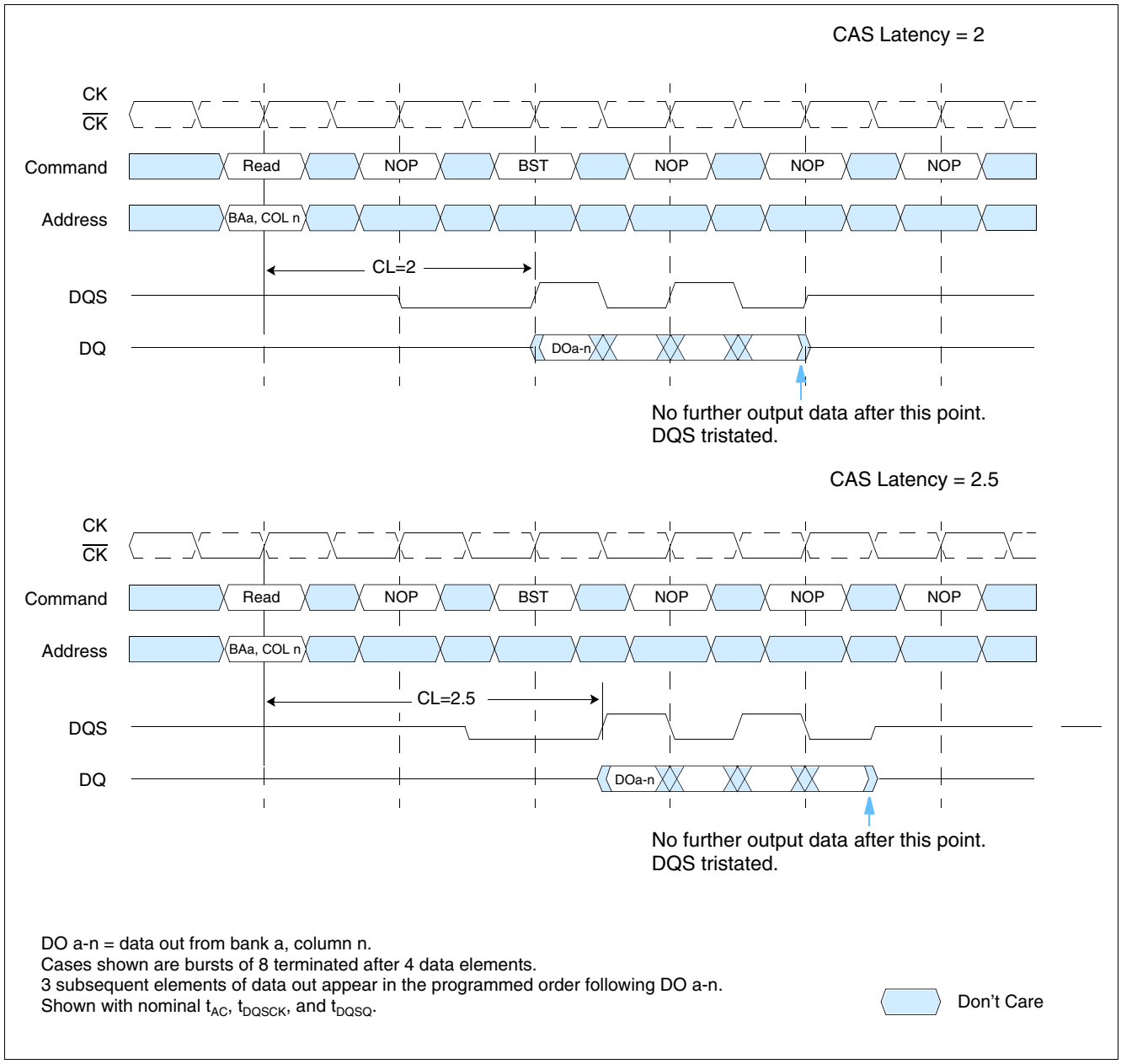


Figure 14 Terminating a Read Burst: CAS Latencies (Burst Length = 8)

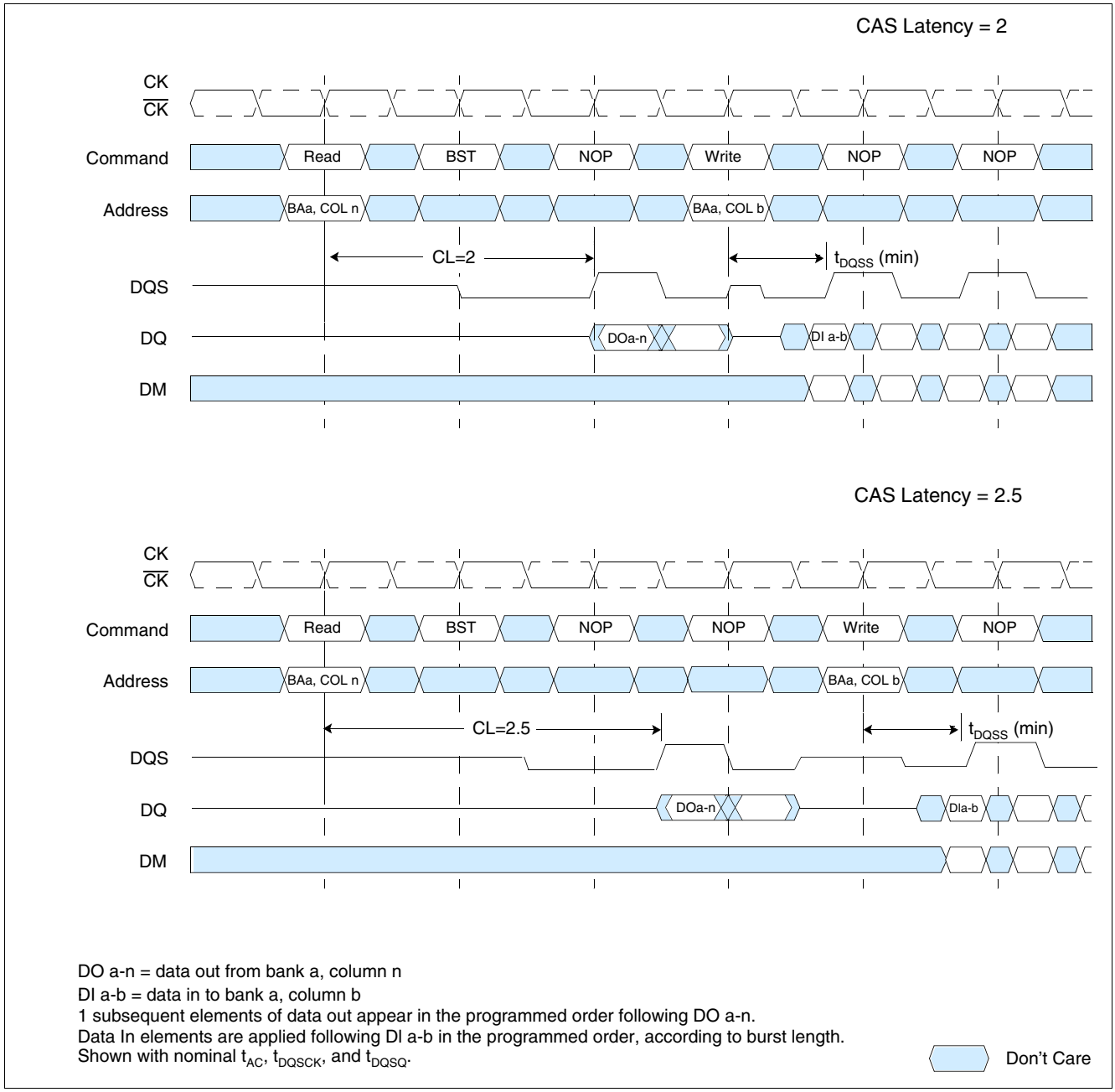


Figure 15 Read to Write: CAS Latencies (Burst Length = 4 or 8)

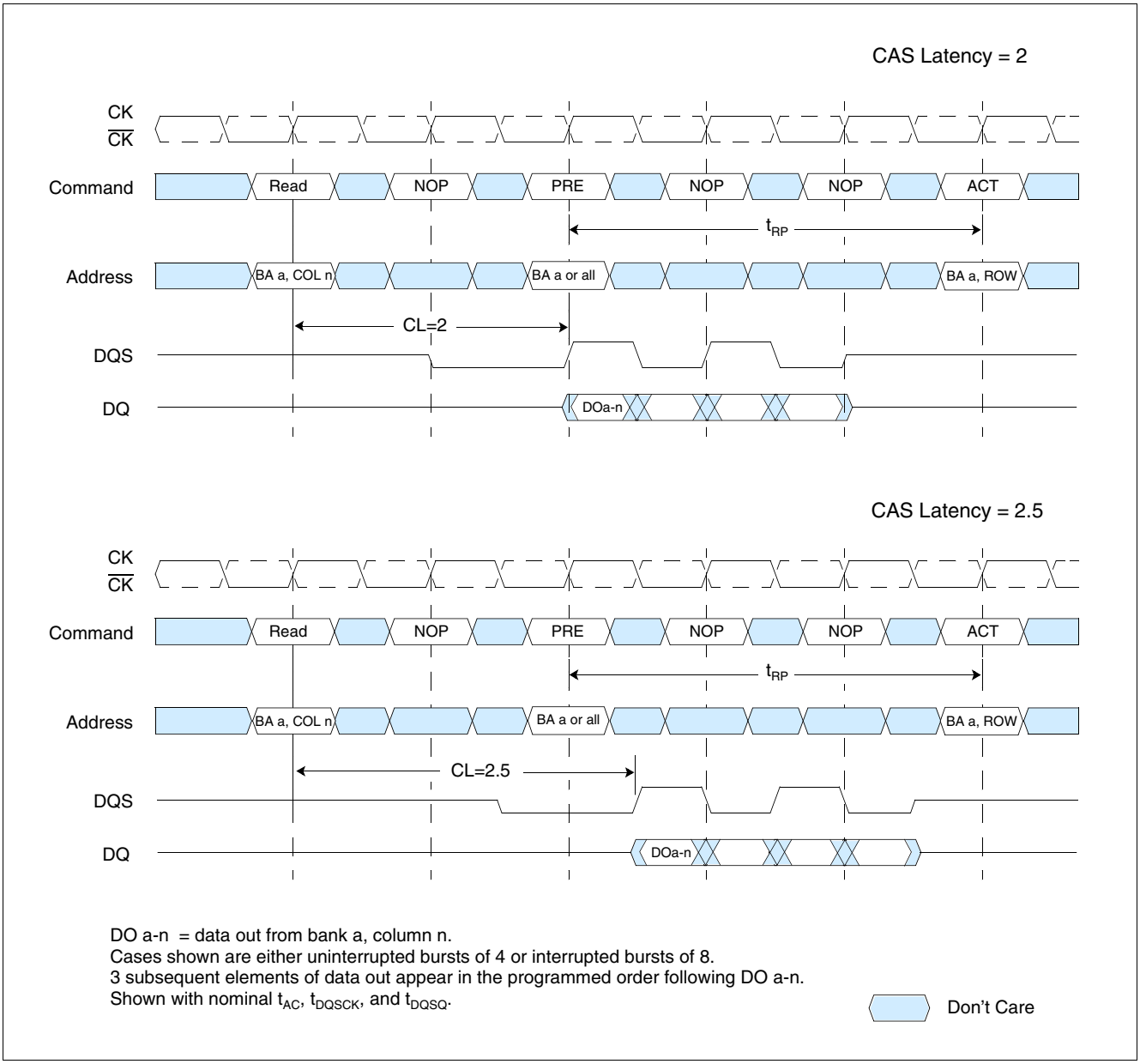


Figure 16 Read to Precharge: CAS Latencies (Burst Length = 4 or 8)

3.5.3 Writes

Write bursts are initiated with a Write command, as shown on **Figure 17 "Write Command" on Page 34**.

The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. t_{DQSS} (min) and t_{DQSS} (max)). **Figure 18 "Write Burst (Burst Length = 4)" on Page 35** shows the two extremes of t_{DQSS} for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). **Figure 19 "Write to Write (Burst Length = 4)" on Page 36** shows concatenated bursts of 4. An example of non-consecutive Writes is shown on **Figure 20 "Write to Write: Max. DQSS, Non-Consecutive (Burst Length = 4)" on Page 37**. Full-speed random write accesses within a page or pages can be performed as shown on **Figure 21 "Random Write Cycles (Burst Length = 2, 4 or 8)" on Page 38**. Data for any Write burst may be followed by a subsequent Read command. To follow a Write without truncating the write burst, t_{WTR} (Write to Read) should be met as shown on **Figure 22 "Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)" on Page 39**.

Data for any Write burst may be truncated by a subsequent Read command, as shown in the figures on **Figure 23 "Write to Read: Interrupting (CAS Latency = 2; Burst Length = 8)" on Page 40** to **Figure 25 "Write to Read: Nominal DQSS, Interrupting (CAS Latency = 2; Burst Length = 8)" on Page 42**. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in the diagrams noted previously.

Data for any Write burst may be followed by a subsequent Precharge command. To follow a Write without truncating the write burst, t_{WR} should be met as shown on **Figure 26 "Write to Precharge: Non-Interrupting (Burst Length = 4)" on Page 43**.

Data for any Write burst may be truncated by a subsequent Precharge command, as shown in the figures on **Figure 27 "Write to Precharge: Interrupting (Burst Length = 4 or 8)" on Page 44** to **Figure 29 "Write to Precharge: Nominal DQSS (2-bit Write), Interrupting (Burst Length = 4 or 8)" on Page 46**. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data in should be masked with DM. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

In the case of a Write burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

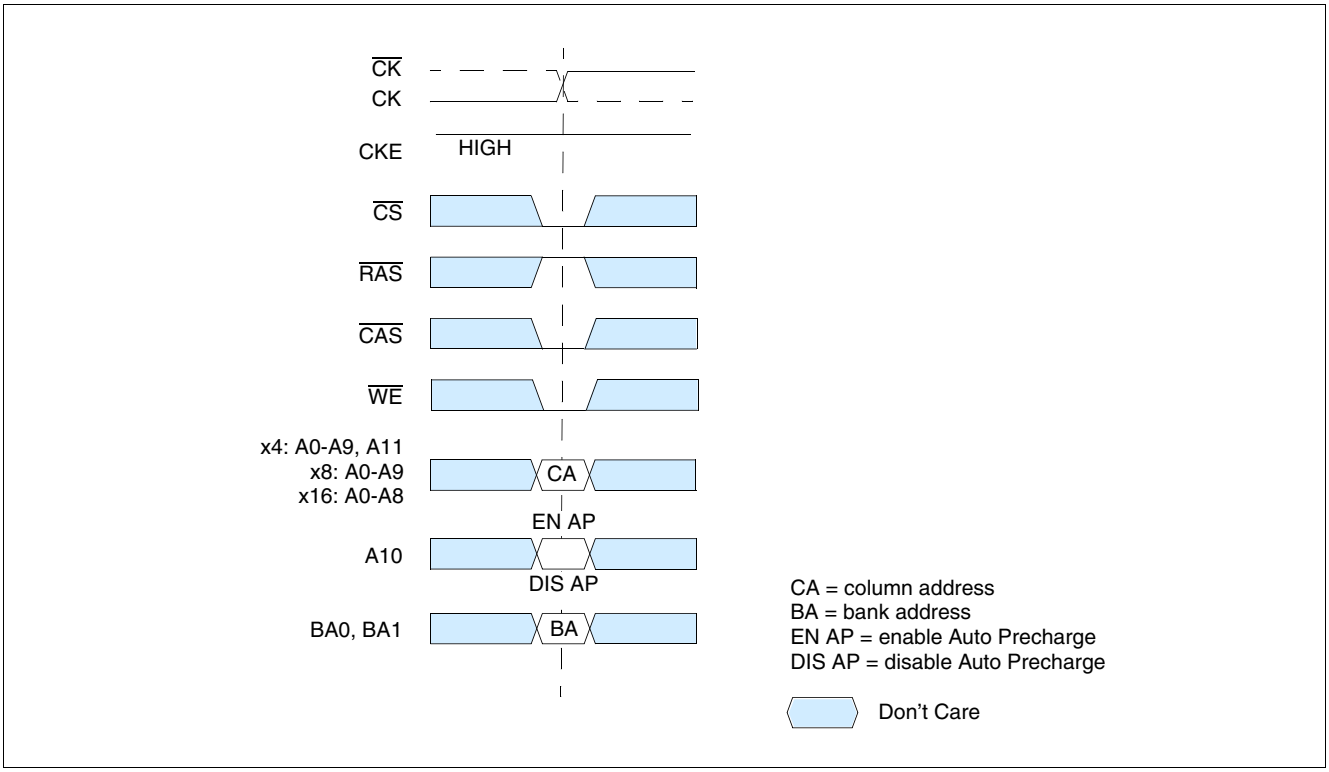
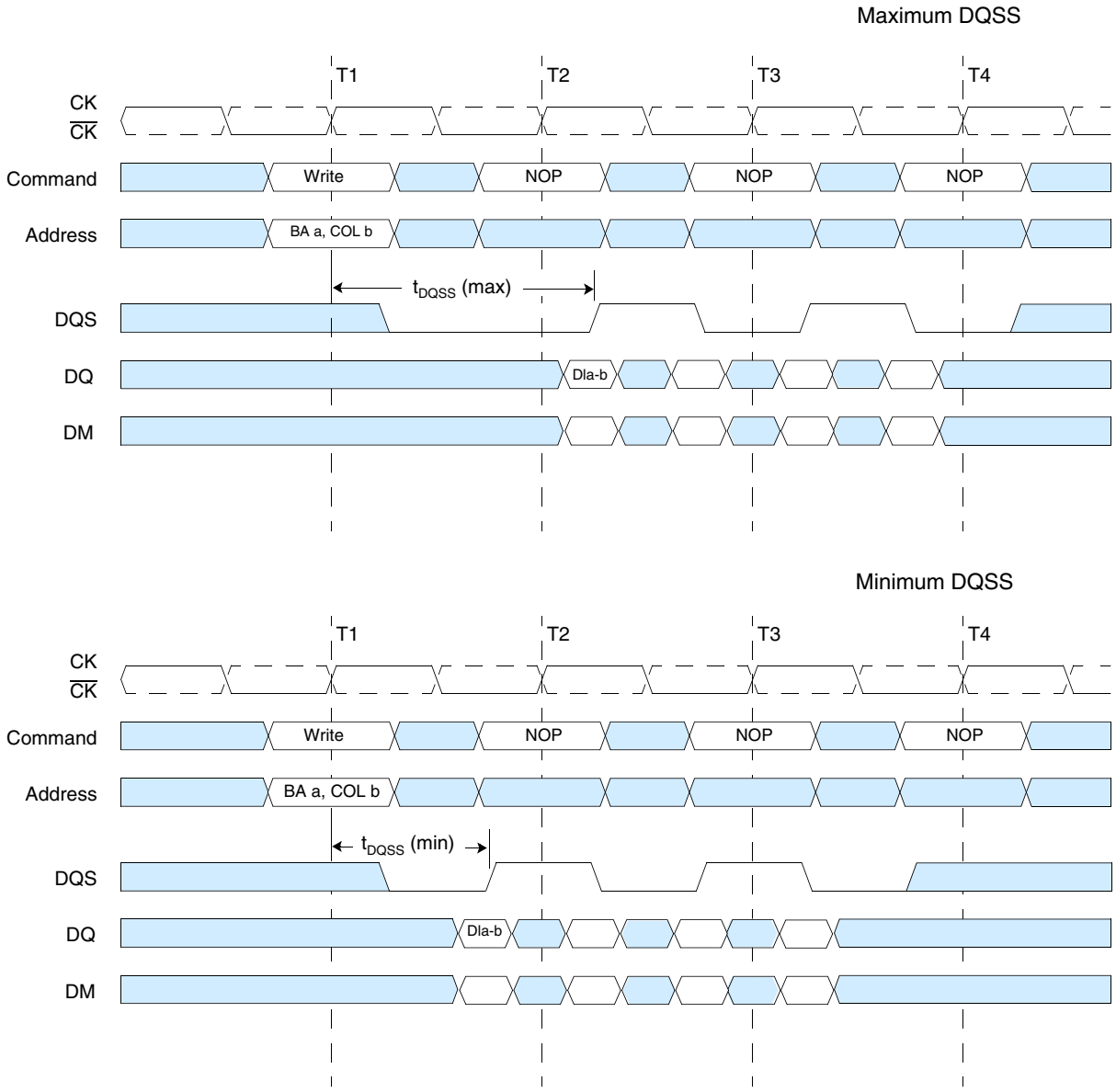
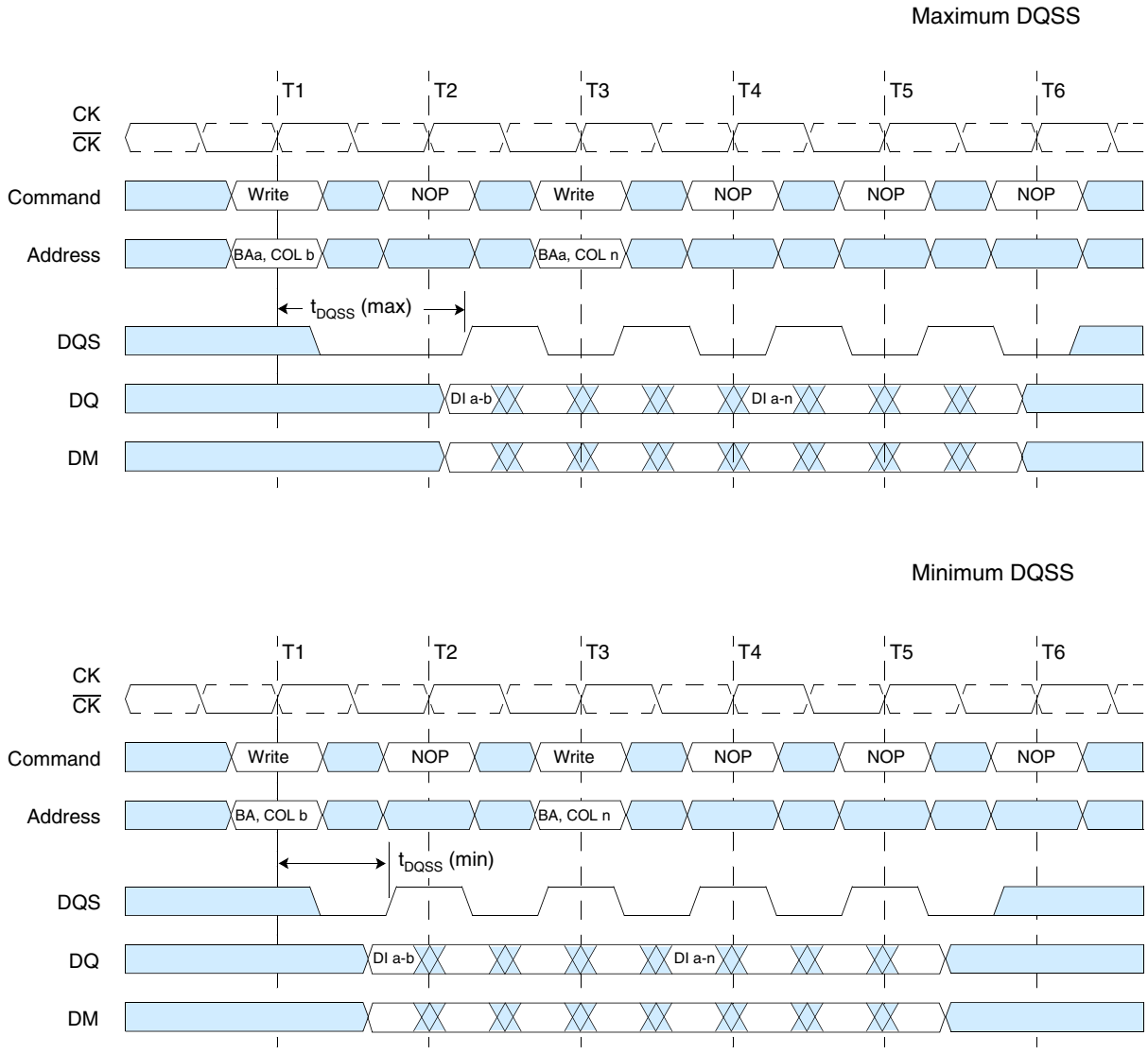


Figure 17 Write Command



DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
A10 is Low with the Write command (Auto Precharge is disabled).

Figure 18 Write Burst (Burst Length = 4)



DI a-b = data in for bank a, column b, etc.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
3 subsequent elements of data in are applied in the programmed order following DI a-n.
A non-interrupted burst is shown.
Each Write command may be to any bank.

Don't Care

Figure 19 Write to Write (Burst Length = 4)

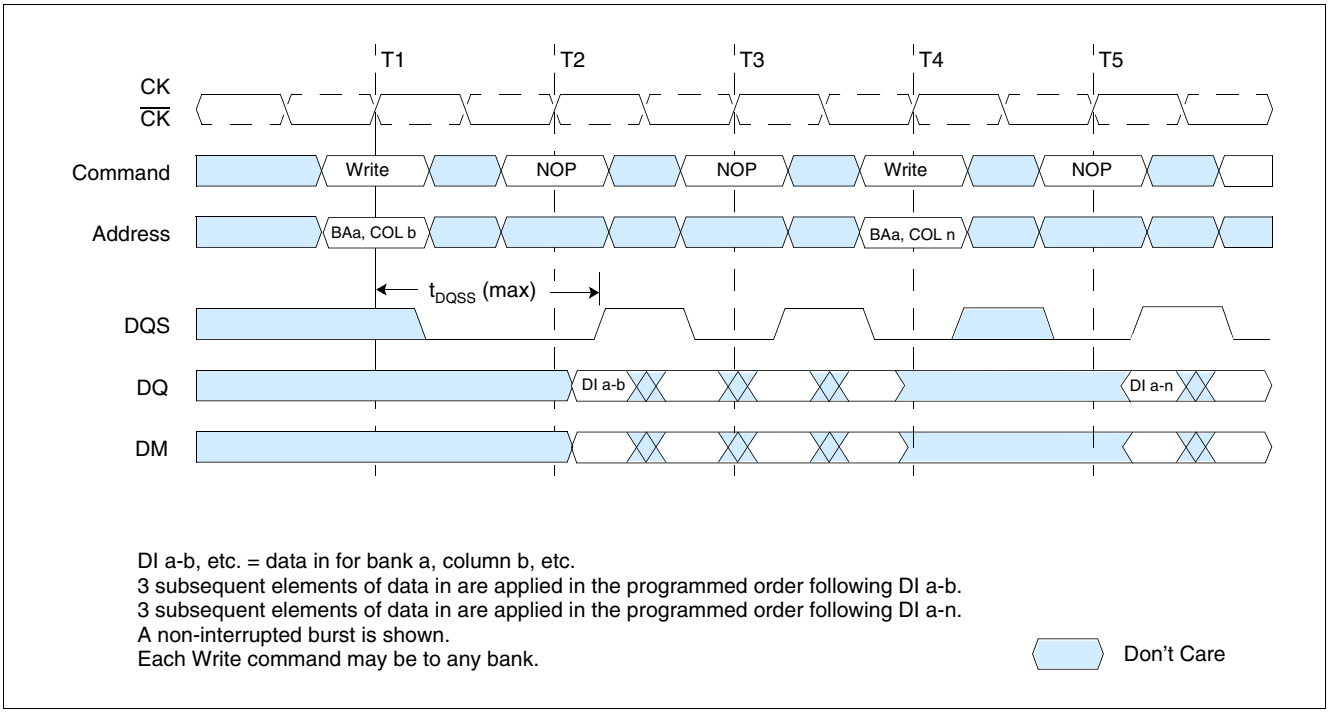


Figure 20 Write to Write: Max. DQSS, Non-Consecutive (Burst Length = 4)

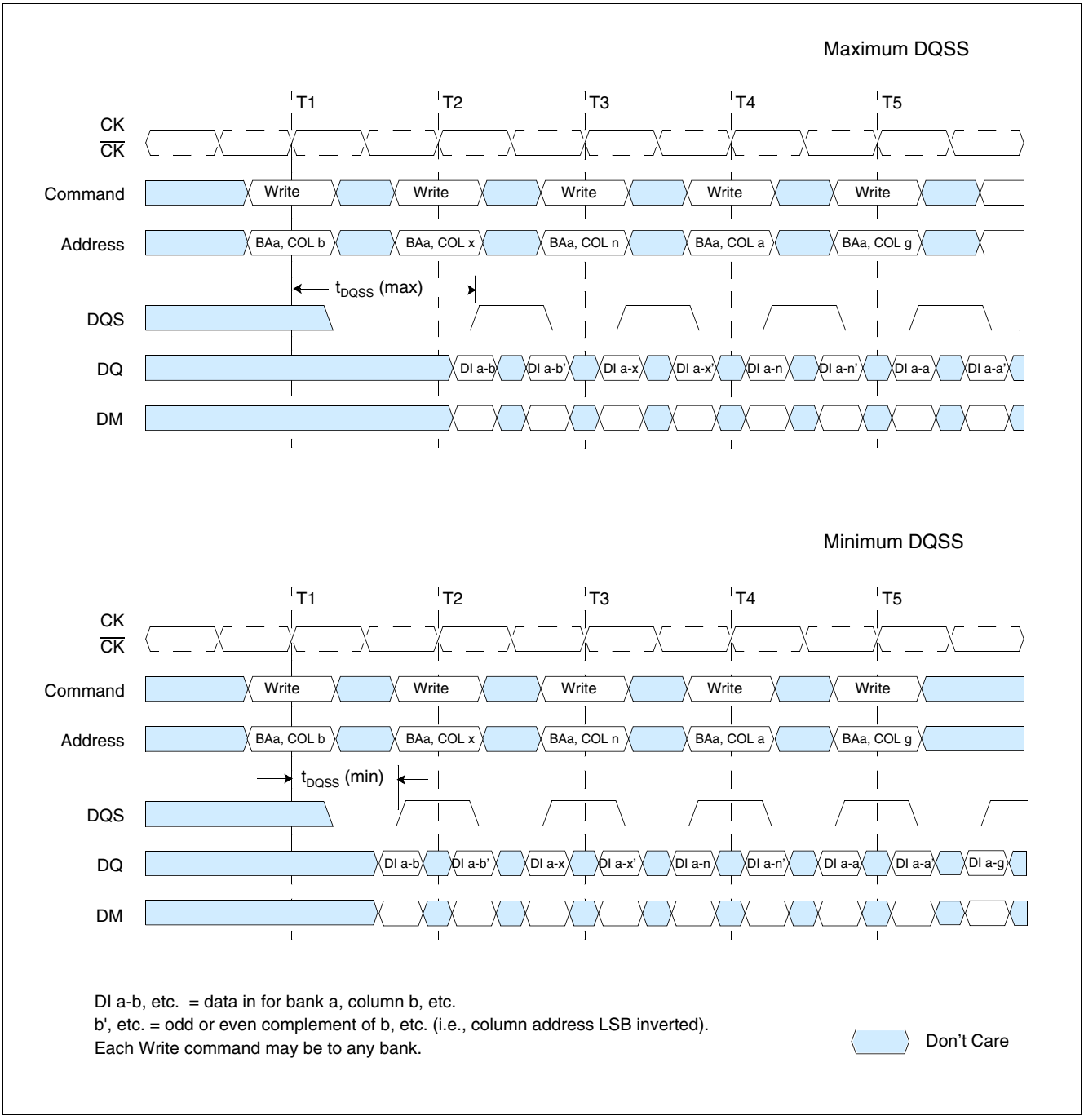


Figure 21 Random Write Cycles (Burst Length = 2, 4 or 8)

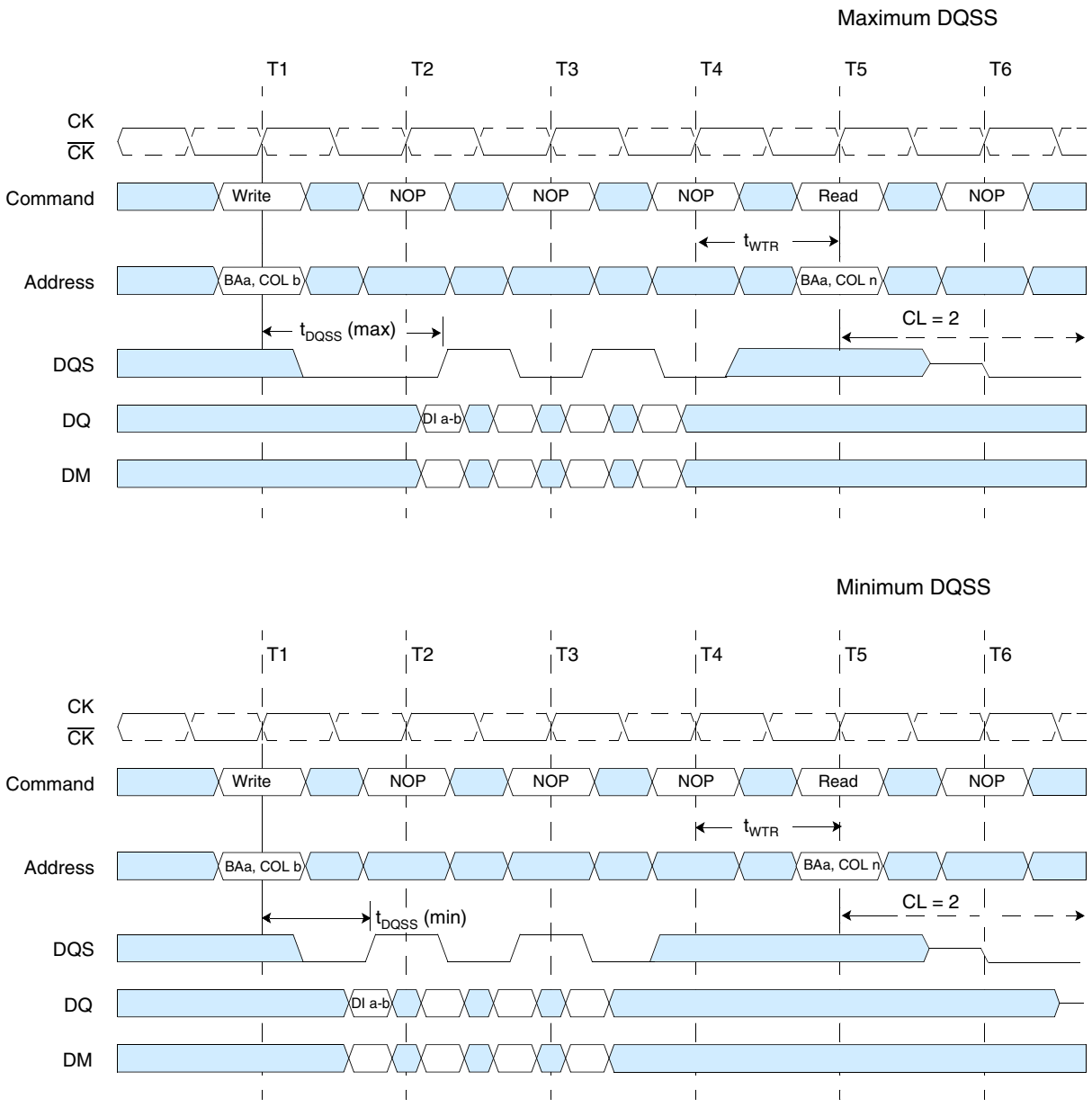


Figure 22 Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)

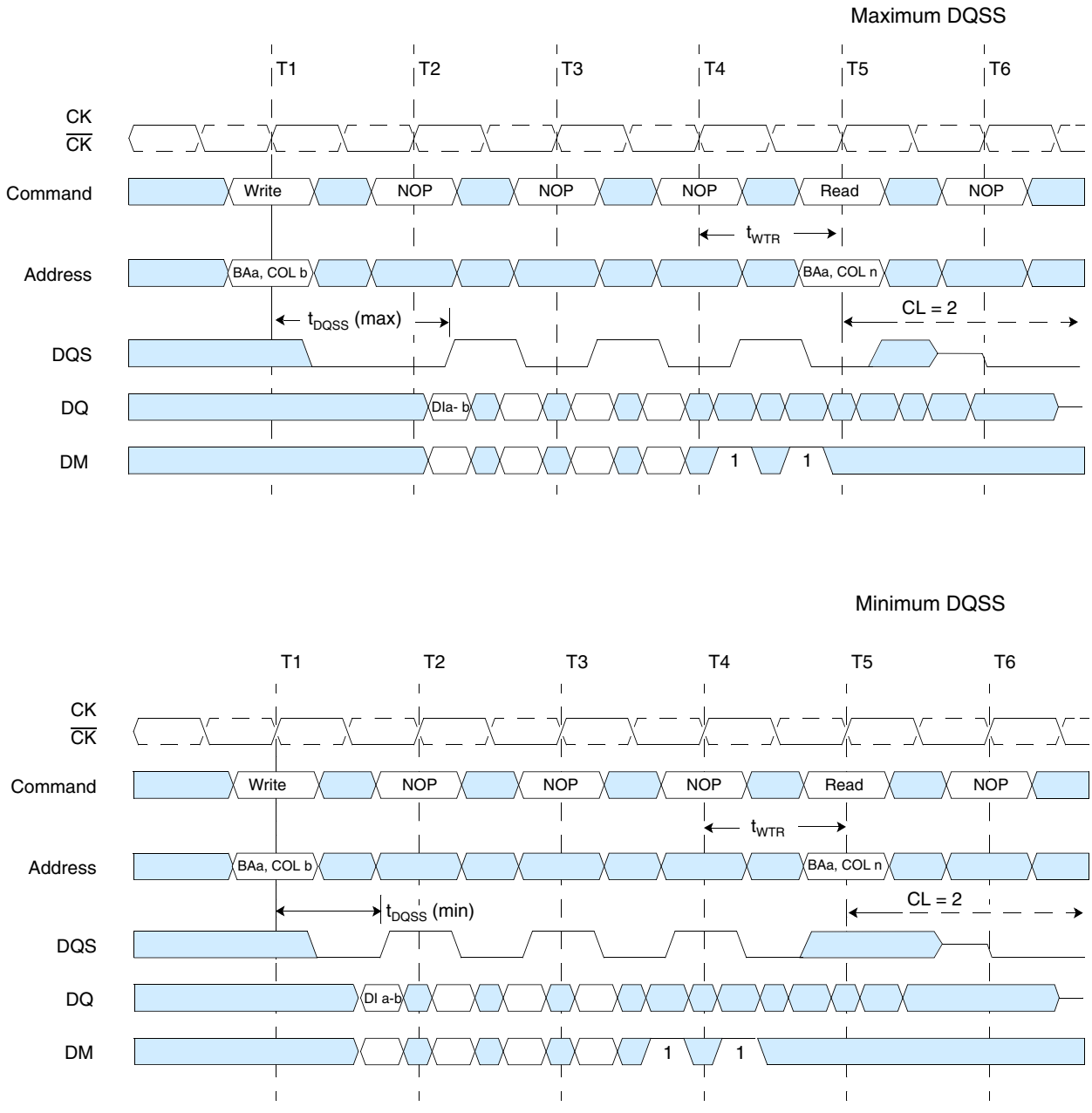
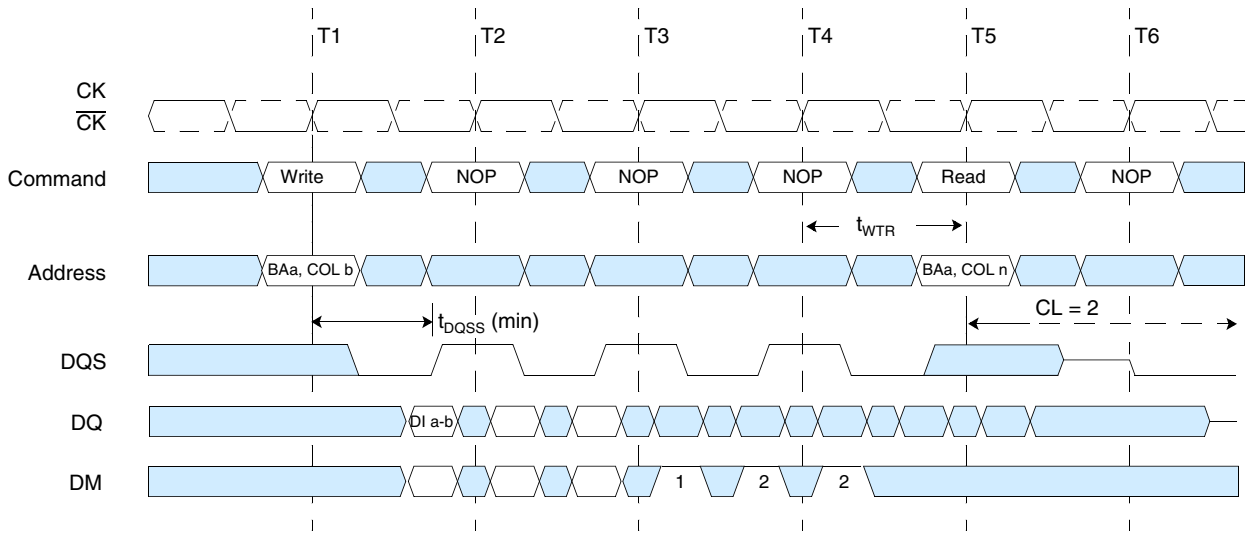


Figure 23 Write to Read: Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 3 data elements are written.
2 subsequent elements of data in are applied in the programmed order following DI a-b.
t_{WTR} is referenced from the first positive CK edge after the last desired data in pair (not the last desired data in element)
The Read command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands are not necessarily to the same bank.
1 = This bit is correctly written into the memory array if DM is low.
2 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Figure 24 Write to Read: Minimum DQSS, Odd Number of Data (3-bit Write), Interrupting (CAS Latency = 2; Burst Length = 8)

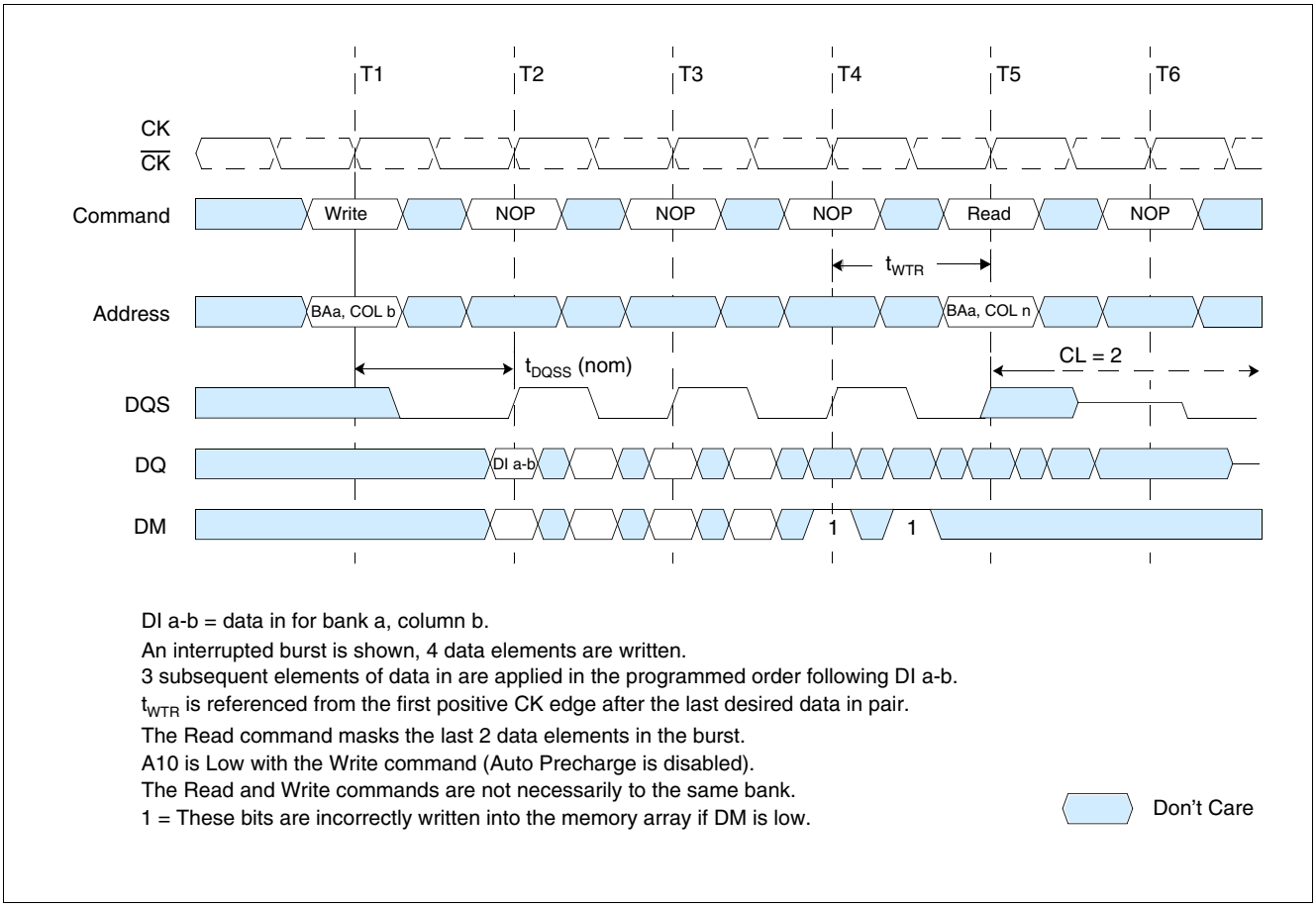


Figure 25 Write to Read: Nominal DQSS, Interrupting (CAS Latency = 2; Burst Length = 8)

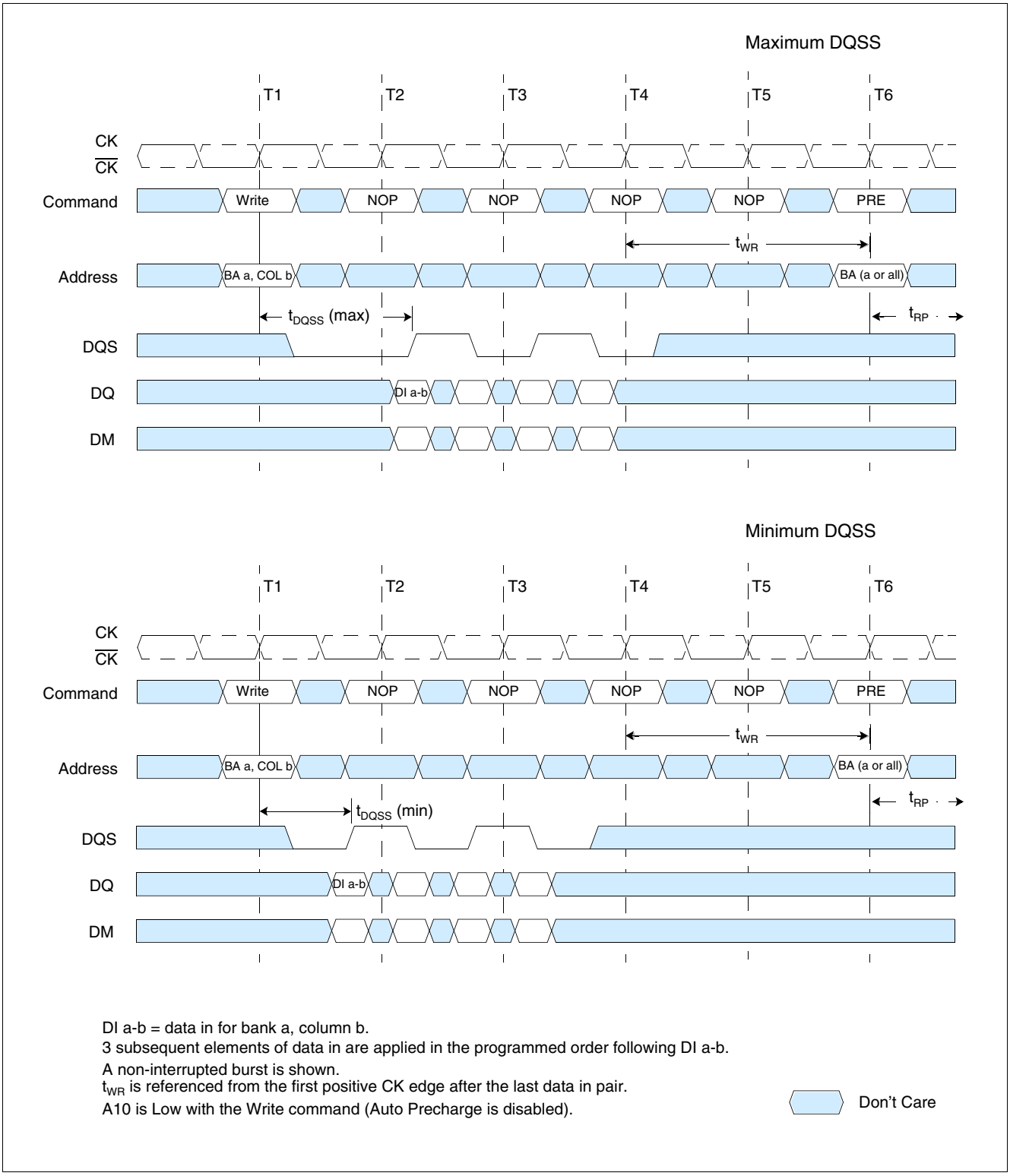
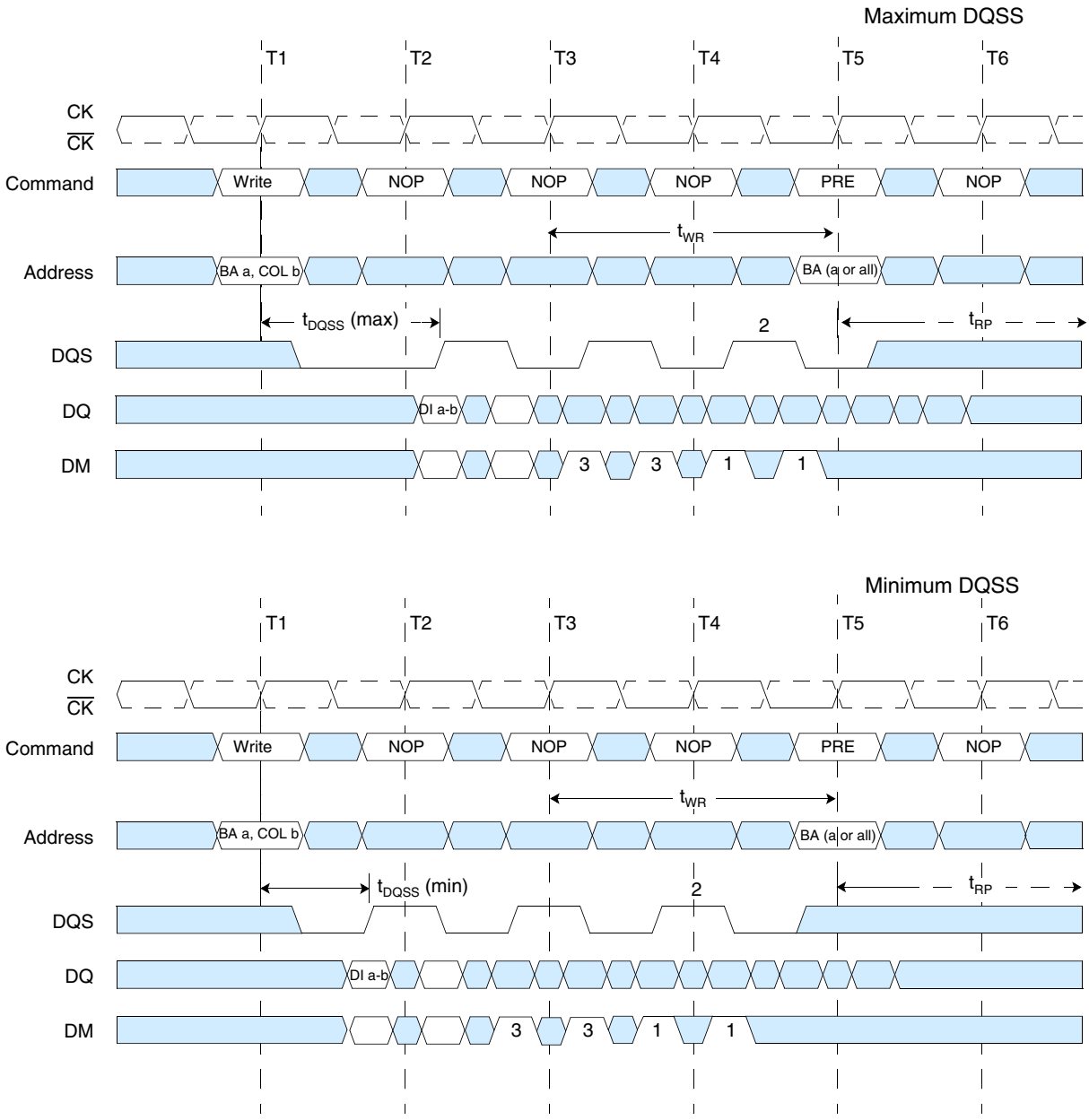


Figure 26 Write to Precharge: Non-Interrupting (Burst Length = 4)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst, for burst length = 8.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Figure 27 Write to Precharge: Interrupting (Burst Length = 4 or 8)

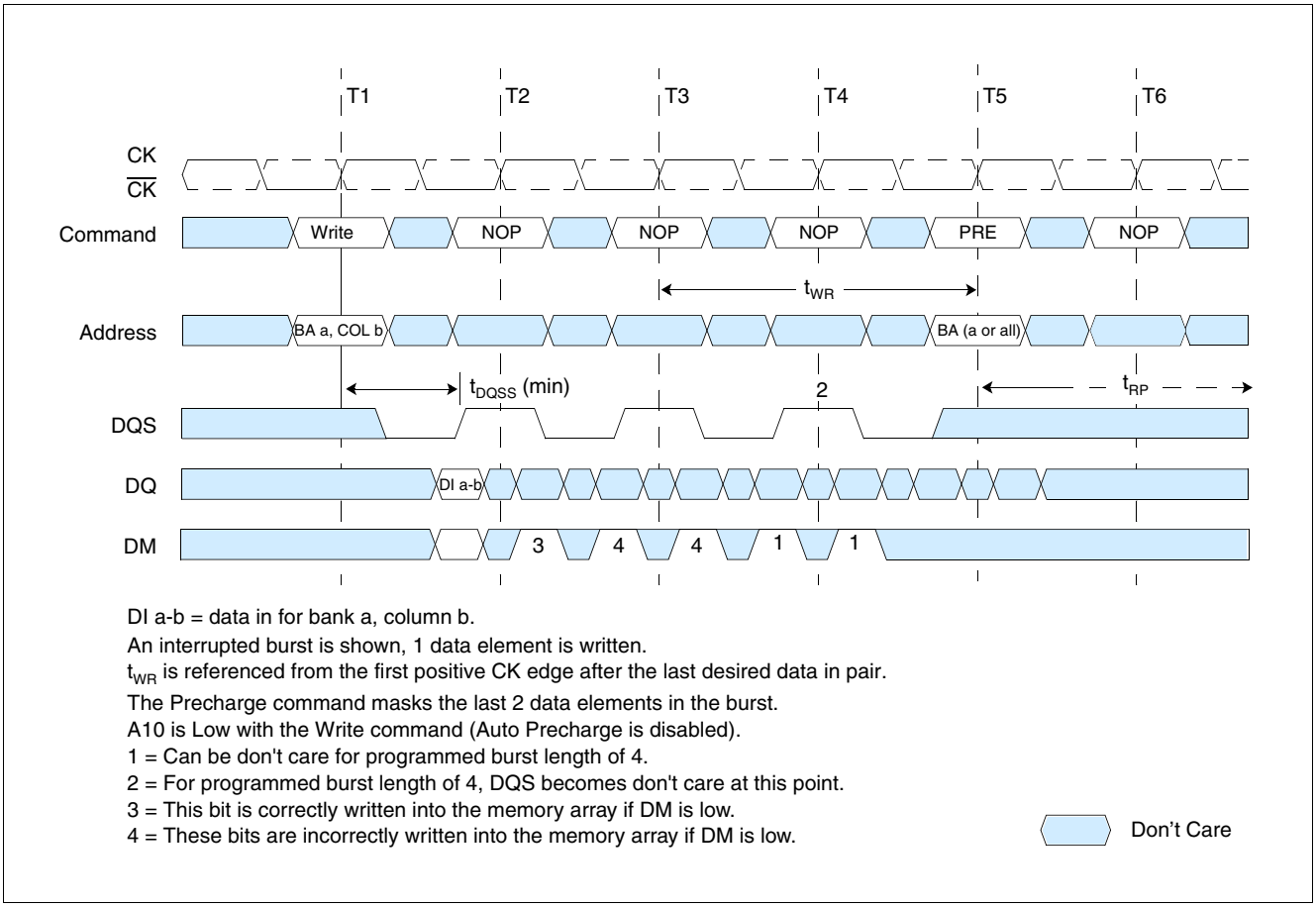


Figure 28 Write to Precharge: Minimum DQSS, Odd Number of Data (1-bit Write), Interrupting (Burst Length = 4 or 8)

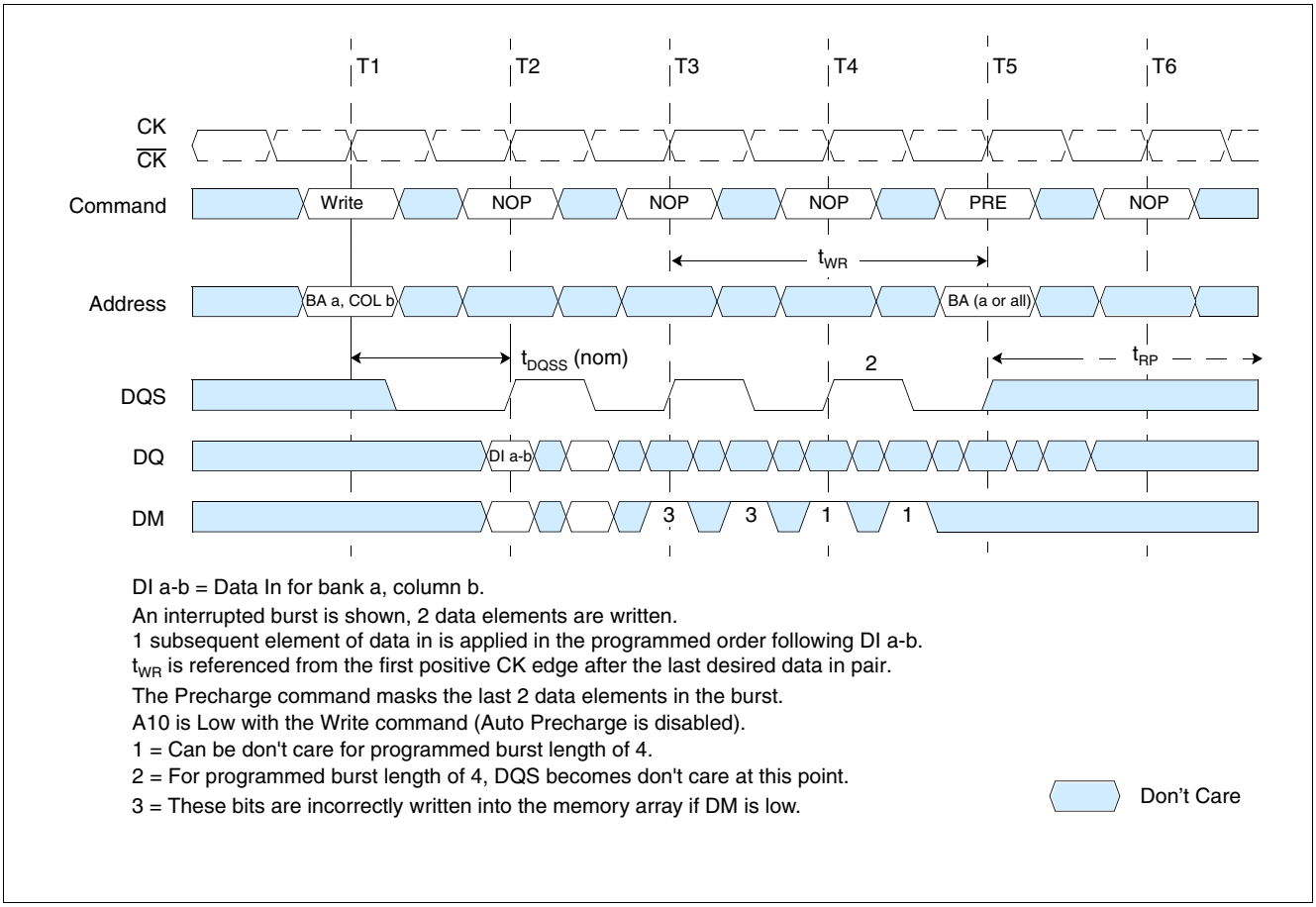


Figure 29 Write to Precharge: Nominal DQSS (2-bit Write), Interrupting (Burst Length = 4 or 8)

3.5.4 Precharge

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

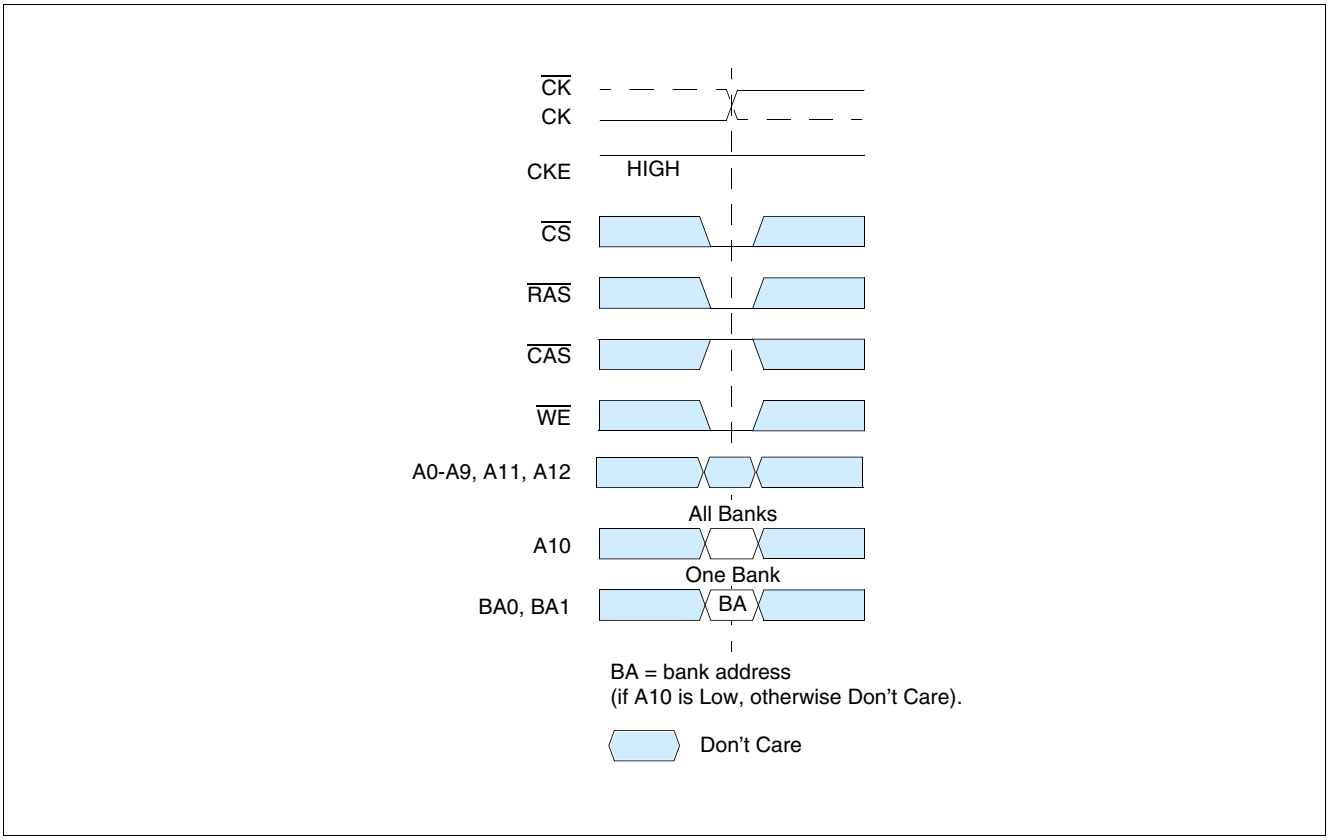


Figure 30 Precharge Command

3.5.5 Power-Down

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. The DLL is still running in Power Down mode, so for maximum power savings, the user has the option of disabling the DLL prior to entering Power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a Read command can be issued. In power-down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are “Don’t Care”. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled power-down mode.

The power-down state is synchronously exited when CKE is registered HIGH (along with a Nop or Deselect command). A valid, executable command may be applied one clock cycle later.

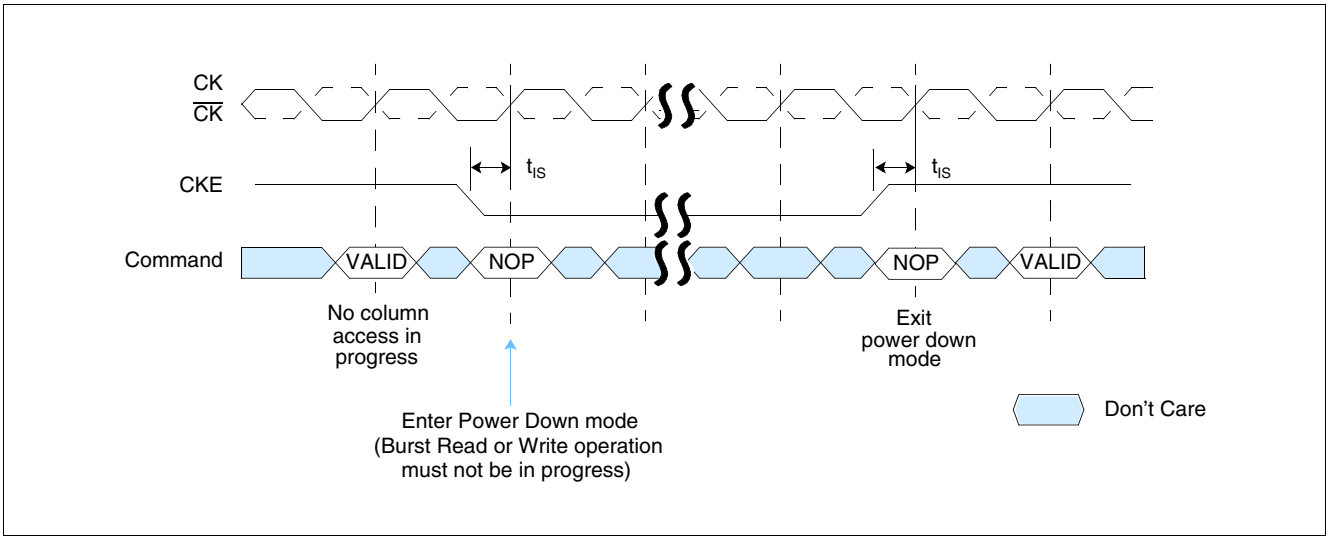


Figure 31 Power Down

Table 8 Truth Table 2: Clock Enable (CKE)

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	–
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	1)
Power Down	L	L	X	Maintain Power-Down	–
Power Down	L	H	Deselect or NOP	Exit Power-Down	–
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	–
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	–
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	–
	H	H	See **"Truth Table 3: Current State Bank n - Command to Bank n (same bank)" on Page 49**	–	–

1) Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

1. CKEn is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMAND n is the command registered at clock edge n, and ACTION n is a result of COMMAND n.
4. All states and sequences not shown are illegal or reserved.

Table 9 Truth Table 3: Current State Bank n - Command to Bank n (same bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	1) to 6)
	L	H	H	H	No Operation	NOP. Continue previous operation	1) to 6)
Idle	L	L	H	H	Active	Select and activate row	1) to 6)
	L	L	L	H	AUTO REFRESH	–	1) to 7)
	L	L	L	L	MODE REGISTER SET	–	1) to 7)
Row Active	L	H	L	H	Read	Select column and start Read burst	1) to 6), 10)
	L	H	L	L	Write	Select column and start Write burst	1) to 6), 10)
	L	L	H	L	Precharge	Deactivate row in bank(s)	1) to 6), 8)
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1) to 6), 10)
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1) to 6), 8)
	L	H	H	L	BURST TERMINATE	BURST TERMINATE	1) to 6), 9)
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1) to 6), 10), 11)
	L	H	L	L	Write	Select column and start Write burst	1) to 6), 10)
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1) to 6), 8), 11)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).

2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.

3) Current state definitions: Idle:The bank has been precharged, and t_{RP} has been met. Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress. Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated. Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank. Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state. Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state. Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state. Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state. Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state& according to Truth Table 4.

5) The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states. Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the “all banks idle” state. Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when tMRD has been met. Once t_{MRD} is met, the DDR SDRAM is in the “all banks idle” state. Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.

6) All states and sequences not shown are illegal or reserved.

7) Not bank-specific; requires that all banks are idle.

8) May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.

9) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.

10) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.

11) Requires appropriate DM masking.

Table 10 Truth Table 4: Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	1) to 6)
	L	H	H	H	No Operation	NOP. Continue previous operation.	1) to 6)
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	–	1) to 6)
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 7)
	L	H	L	L	Write	Select column and start Write burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start new Read burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 8)
	L	H	L	L	Write	Select column and start new Write burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start new Read burst	1) to 7), 10)
	L	H	L	L	Write	Select column and start Write burst	1) to 7), 9), 10)
	L	L	H	L	Precharge	–	1) to 6)
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 7), 9)
	L	H	L	L	Write	Select column and start new Write burst	1) to 7), 9)
	L	L	H	L	Precharge	–	1) to 6)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 8**: Clock Enable (CKE) and after t_{XSNR}/t_{XSRD} has been met (if the previous state was self refresh).

2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3) Current state definitions:
Idle: The bank has been precharged, and t_{RP} has been met.
Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Read with Auto Precharge Enabled: See [10].
Write with Auto Precharge Enabled: See [10].

4) AUTO REFRESH and Mode Register Set commands may only be issued when all banks are idle.

5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

6) All states and sequences not shown are illegal or reserved.

7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.

8) Requires appropriate DM masking.

9) **Concurrent Auto Precharge:**
This device supports “Concurrent Auto Precharge”. When a read with auto precharge or a write with auto precharge is enabled any command may follow to the other banks as long as that command does not interrupt the read or write data transfer and all other limitations apply (e.g. contention between READ data and WRITE data must be avoided). The minimum delay from a read or write command with auto precharge enable, to a command to a different banks is summarized in **Table 11**.

10) A Write command may be applied after the completion of data output.

Table 11 Truth Table 5: Concurrent Auto Precharge

From Command	To Command (different bank)	Minimum Delay with Concurrent Auto Precharge Support	Unit
WRITE w/AP	Read or Read w/AP	1 + (BL/2) + t_{WTR}	t_{CK}
	Write to Write w/AP	BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}
Read w/AP	Read or Read w/AP	BL/2	t_{CK}
	Write or Write w/AP	CL (rounded up) + BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}

3.6 Simplified State Diagram

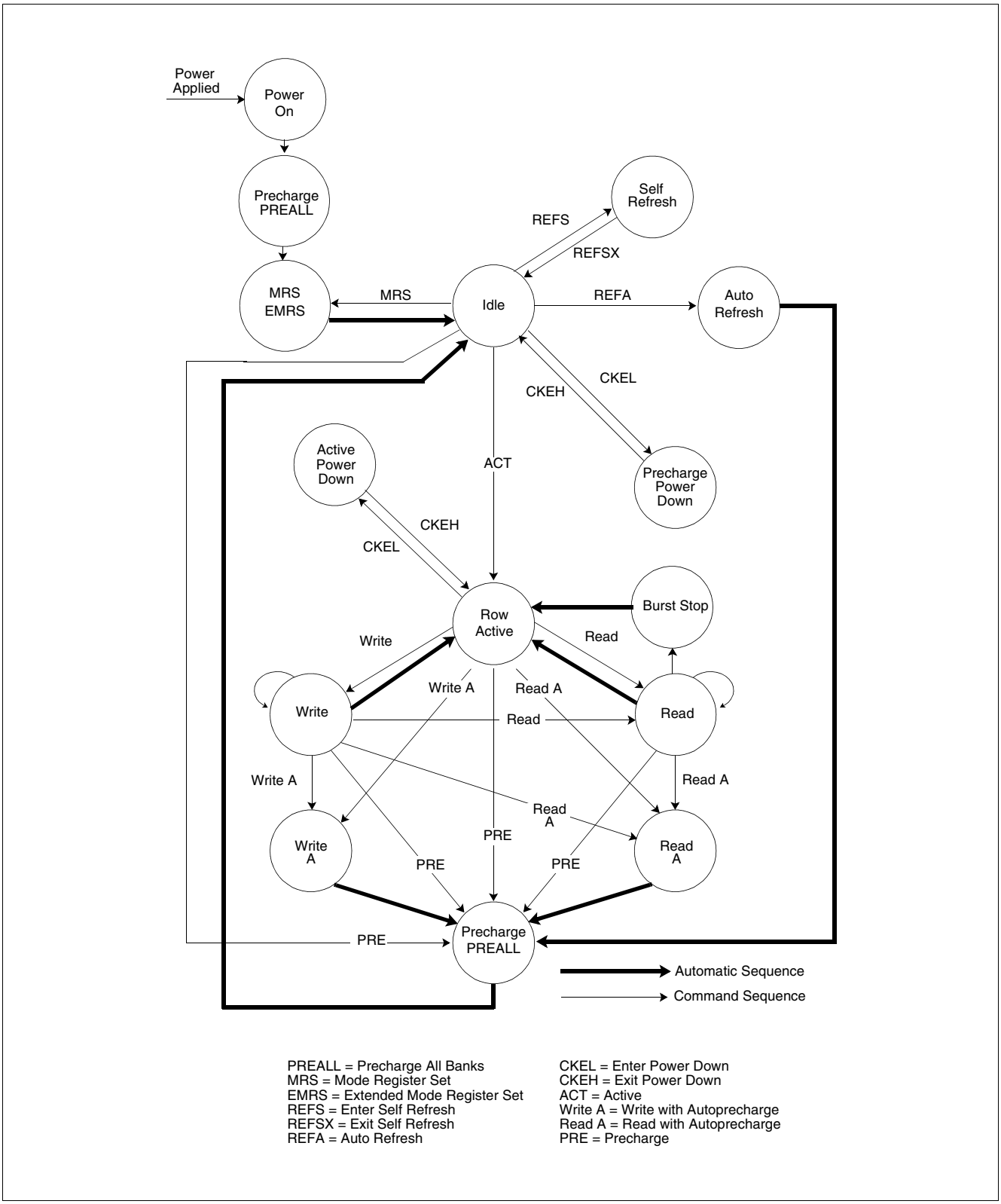


Figure 32 Simplified State Diagram

4 Electrical Characteristics

4.1 Operating Conditions

Table 12 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	—	V_{DDQ}+0.5	V	—
Voltage on inputs relative to V_{SS}	V_{IN}	–1.0	—	+3.6	V	—
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1.0	—	+3.6	V	—
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1.0	—	+3.6	V	—
Operating temperature (ambient)	T_A	0	—	+70	°C	—
Storage temperature (plastic)	T_{STG}	-55	—	+150	°C	—
Power dissipation (per SDRAM component)	P_D	—	1.5	—	W	—
Short circuit output current	I_{OUT}	—	50	—	mA	—

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 13 Input and Output Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input Capacitance: CK, $\overline{CK}$	C_{I1}	1.5	—	2.5	pF	TSOPII [1]
		2.0	—	3.0	pF	TFBGA [1]
Delta Input Capacitance	C_{dI1}	—	—	0.25	pF	[1]
Input Capacitance: All other input-only pins	C_{I2}	1.5	—	2.5	pF	TFBGA [1]
		2.0	—	3.0	pF	TSOPII [1]
Delta Input Capacitance: All other input-only pins	C_{dIO}	—	—	0.5	pF	[1]
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	3.5	—	4.5	pF	TFBGA [1)2)]
		4.0	—	5.0	pF	TSOPII [1)2)]
Delta Input/Output Capacitance: DQ, DQS, DM	C_{dIO}	—	—	0.5	pF	[1]

1) These values are guaranteed by design and are tested on a sample base only. V_{DDQ} = V_{DD} = 2.5 V ± 0.2 V, f = 100 MHz, T_A = 25 °C, $V_{OUT(DC)}$ = V_{DDQ}/2, V_{OUT} (Peak to Peak) 0.2 V. Unused pins are tied to ground.

2) DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

Table 14 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2)3)]
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[8]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	[8]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	[8]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	[8)6)]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[7]
Input Leakage Current	I_I	–2		2	µA	Any input 0 V ≤ $V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [8)9)]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V ≤ $V_{OUT} \leq V_{DDQ}$
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V

1) 0 °C ≤ $T_A \leq$ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400);

2) DDR400 conditions apply for all clock frequencies above 166 MHz

3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

7) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

8) Inputs are not recognized as valid until V_{REF} stabilizes.

9) Values are shown per component

4.2 Normal Strength Pull-down and Pull-up Characteristics

1. The nominal pulldown V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
2. The full variation in driver pulldown current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.
3. The nominal pullup V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
4. The full variation in driver pullup current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.
5. The full variation in the ratio of the maximum to minimum pullup and pulldown current does not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
6. The full variation in the ratio of the nominal pullup to pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0 V.

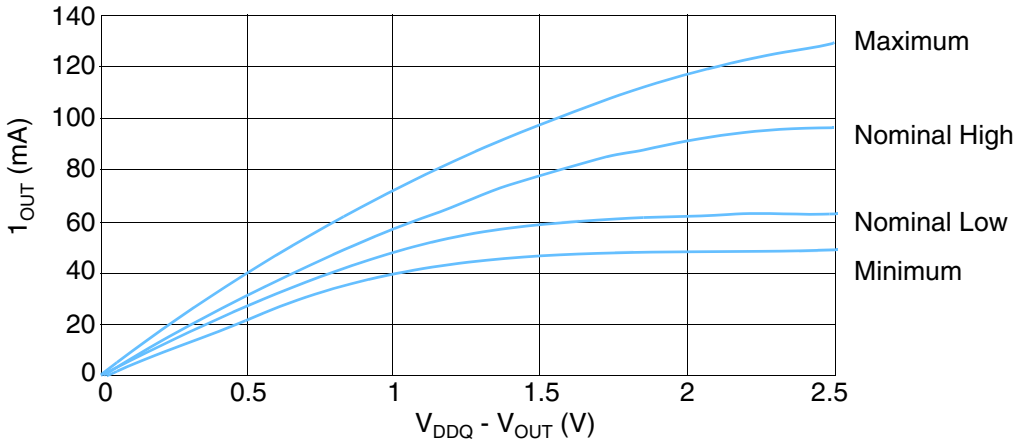


Figure 33 Normal Strength Pull-down Characteristics

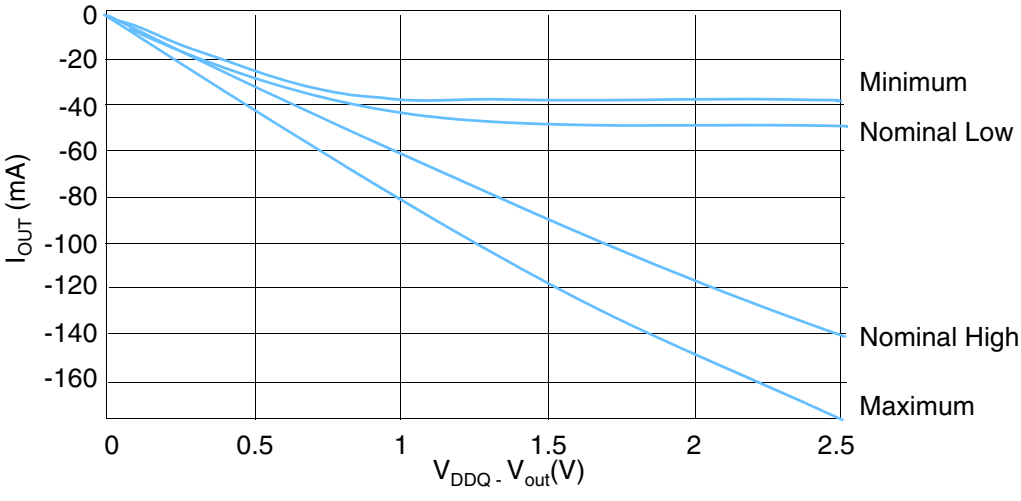


Figure 34 Normal Strength Pull-up Characteristics

Table 15 Normal Strength Pull-down and Pull-up Currents

Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Nominal Low	Nominal High	min.	max.	Nominal Low	Nominal High	min.	max.
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.9	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	–155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	–160.1	–41.2	–198.2

Table 16 Pull-down and Pull-up Process Variations and Conditions

Parameter	Nominal	Minimum	Maximum
Operating Temperature	25 °C	0 °C	70 °C
V_{DD}/V_{DDQ}	2.5 V	2.3 V	2.7 V
Process Corner	typical	slow-slow	fast-fast

4.3 Weak Strength Pull-down and Pull-up Characteristics

1. The weak pulldown V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve
2. The weak pullup V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
3. The full variation in driver pullup current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.
4. The full variation in the ratio of the maximum to minimum pullup and pulldown current does not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
5. The full variation in the ratio of the nominal pullup to pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0V.

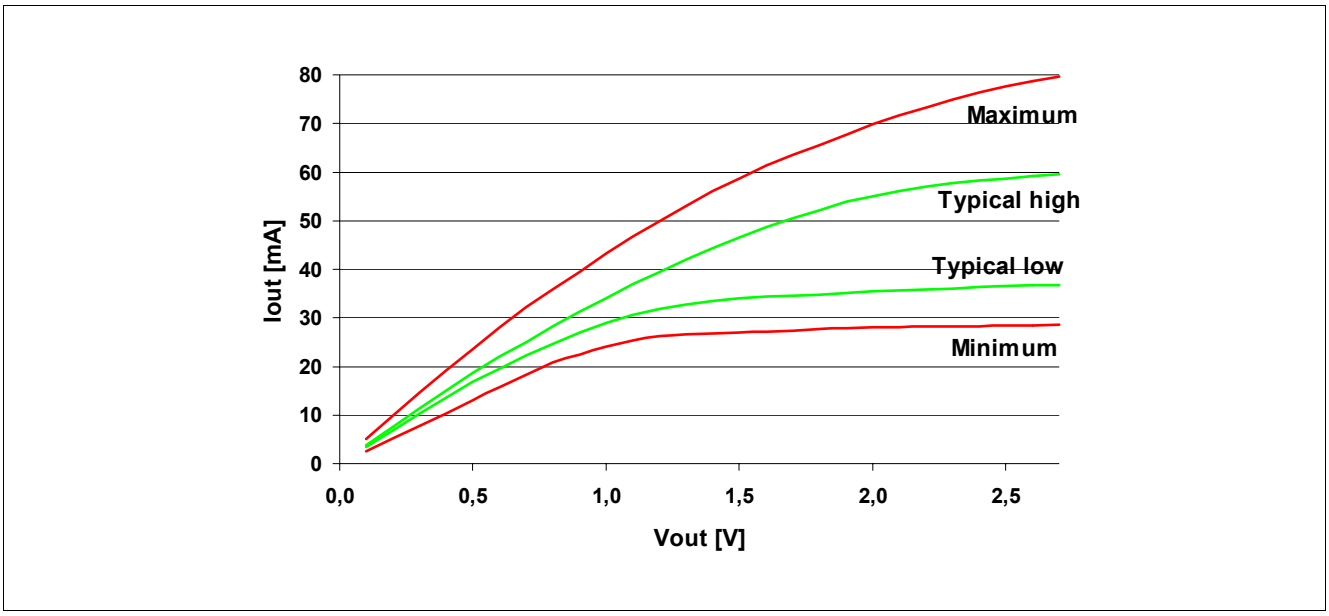


Figure 35 Weak Strength Pull-down Characteristics

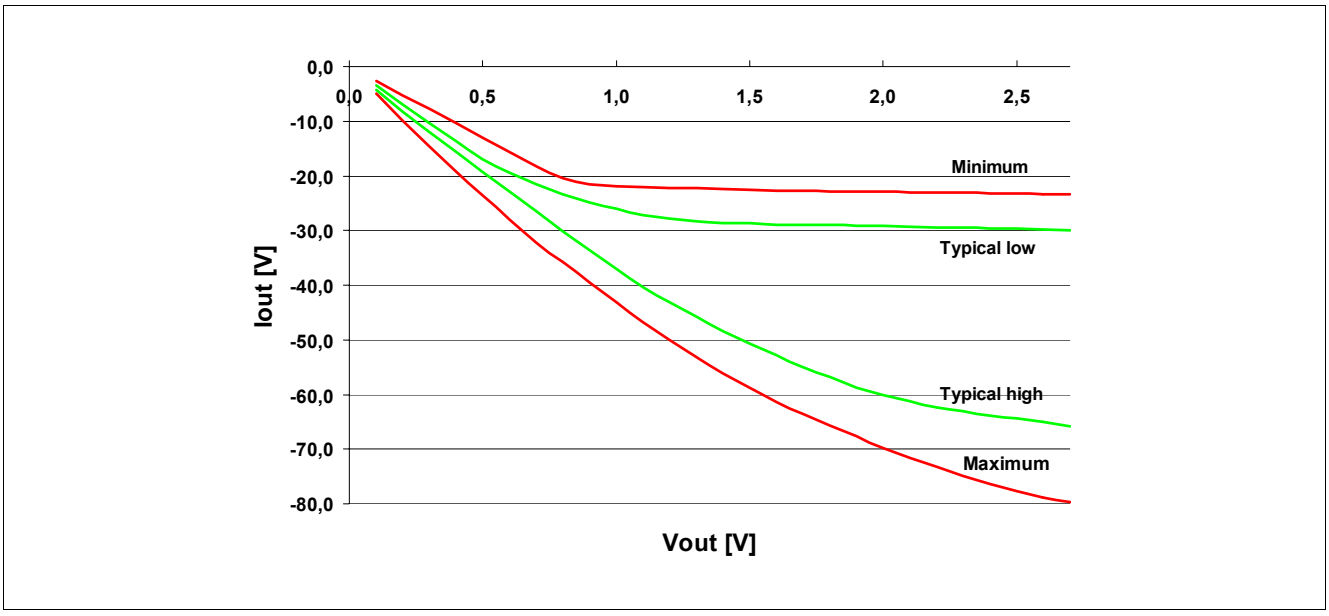


Figure 36 Weak Strength Pull-up Characteristics

Table 17 Weak Strength Driver Pull-down and Pull-up Characteristics

Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Nominal Low	Nominal High	min.	max.	Nominal Low	Nominal High	min.	max.
0.1	3.4	3.8	2.6	5.0	–3.5	–4.3	–2.6	–5.0
0.2	6.9	7.6	5.2	9.9	–6.9	–8.2	–5.2	–9.9
0.3	10.3	11.4	7.8	14.6	–10.3	–12.0	–7.8	–14.6
0.4	13.6	15.1	10.4	19.2	–13.6	–15.7	–10.4	–19.2
0.5	16.9	18.7	13.0	23.6	–16.9	–19.3	–13.0	–23.6
0.6	19.6	22.1	15.7	28.0	–19.4	–22.9	–15.7	–28.0
0.7	22.3	25.0	18.2	32.2	–21.5	–26.5	–18.2	–32.2
0.8	24.7	28.2	20.8	35.8	–23.3	–30.1	–20.4	–35.8
0.9	26.9	31.3	22.4	39.5	–24.8	–33.6	–21.6	–39.5
1.0	29.0	34.1	24.1	43.2	–26.0	–37.1	–21.9	–43.2
1.1	30.6	36.9	25.4	46.7	–27.1	–40.3	–22.1	–46.7
1.2	31.8	39.5	26.2	50.0	–27.8	–43.1	–22.2	–50.0
1.3	32.8	42.0	26.6	53.1	–28.3	–45.8	–22.3	–53.1
1.4	33.5	44.4	26.8	56.1	–28.6	–48.4	–22.4	–56.1
1.5	34.0	46.6	27.0	58.7	–28.7	–50.7	–22.6	–58.7
1.6	34.3	48.6	27.2	61.4	–28.9	–52.9	–22.7	–61.4
1.7	34.5	50.5	27.4	63.5	–28.9	–55.0	–22.7	–63.5
1.8	34.8	52.2	27.7	65.6	–29.0	–56.8	–22.8	–65.6
1.9	35.1	53.9	27.8	67.7	–29.2	–58.7	–22.9	–67.7
2.0	35.4	55.0	28.0	69.8	–29.2	–60.0	–22.9	–69.8
2.1	35.6	56.1	28.1	71.6	–29.3	–61.2	–23.0	–71.6
2.2	35.8	57.1	28.2	73.3	–29.5	–62.4	–23.0	–73.3
2.3	36.1	57.7	28.3	74.9	–29.5	–63.1	–23.1	–74.9
2.4	36.3	58.2	28.3	76.4	–29.6	–63.8	–23.2	–76.4
2.5	36.5	58.7	28.4	77.7	–29.7	–64.4	–23.2	–77.7
2.6	36.7	59.2	28.5	78.8	–29.8	–65.1	–23.3	–78.8
2.7	36.8	59.6	28.6	79.7	–29.9	–65.8	–23.3	–79.7

Table 18 Evaluation Conditions for I/O Driver Characteristics

Parameter	Nominal	Minimum	Maximum
Operating Temperature	25	70	0
V_{DD}/V_{DDQ}	2.5	2.3	2.7
Process Corner	typ.	slow-slow	fast-fast

4.4 AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

Notes:

1. *All voltages referenced to V_{SS}.*
2. *Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.*
3. ***Figure 37** represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).*
4. *AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.*
5. *The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level).*
6. *For System Characteristics like Setup & Holdtime Derating for Slew Rate, I/O Delta Rise/Fall Derating, DDR SDRAM Slew Rate Standards, Overshoot & Undershoot specification and Clamp V-I characteristics see the latest JEDEC specification for DDR components.*

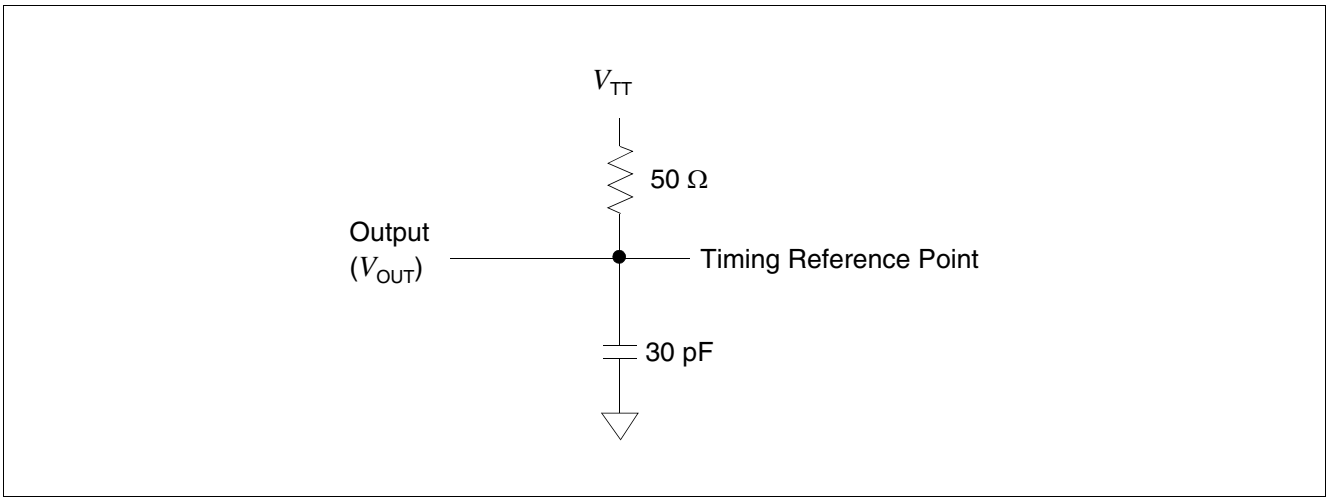


Figure 37 AC Output Load Circuit Diagram / Timing Reference Load

Table 19 AC Operating Conditions[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Input High (Logic 1) Voltage, DQ, DQS and DM Signals	$V_{IH(AC)}$	V_{REF} + 0.31	—	V	2)3)
Input Low (Logic 0) Voltage, DQ, DQS and DM Signals	$V_{IL(AC)}$	—	V_{REF} – 0.31	V	2)3)
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	2)3)4)
Input Closing Point Voltage, CK and $\overline{CK}$ Inputs	$V_{IX(AC)}$	0.5 × V_{DDQ} – 0.2	0.5 × V_{DDQ} + 0.2	V	2)3)5)

1) V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR200 - DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400); 0 °C ≤ T_A ≤ 70 °C

2) Input slew rate = 1 V/ns.

3) Inputs are not recognized as valid until V_{REF} stabilizes.

4) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

5) The value of V_{IX} is expected to equal 0.5 × V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Table 20 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1)]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock cycle time	t_{CK}	5	8	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	(t_{WR}/t_{CK})+(t_{RP}/t_{CK})				t_{CK}	2)3)4)5)6)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
		—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)

Table 20 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})	—	min. (t_{CL}, t_{CH})	—	ns	2)3)4)5)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)9)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.70	–0.70	+0.70	ns	2)3)4)5)7)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
DQ/DQS output hold time	t_{QH}	t_{HP} –t_{QHS}	—	t_{HP} –t_{QHS}	—	ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA 2)3)4)5)
		—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	t_{RCD} or t_{RASmin}	—	t_{RCD} or t_{RASmin}	—	ns	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)8)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	70	—	72	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)

Table 20 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)10)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)11)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

9) These parameters guarantee device timing, but they are not necessarily tested on each device.

10) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specificationsof the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on t_{DQSS}.

11) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

Table 21 AC Timing - Absolute Specifications PC2100A and PC2100

Parameter	Symbol	–7		–7F		Unit	Note/ Test Condition [1]
		DDR266A		DDR266			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock cycle time	t_{CK2}	7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
Clock cycle time	$t_{CK2.5}$	7.5	12	7.5	12	ns	CL = 2.5 2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)

Table 21 AC Timing - Absolute Specifications PC2100A and PC2100

Parameter	Symbol	–7		–7F		Unit	Note/ Test Condition 1)
		DDR266A		DDR266			
		Min.	Max.	Min.	Max.		
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$				t_{CK}	2)3)4)5)6)
DQ and DM input hold time	t_{DH}	0.5	—	0.5	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.5	—	+0.5	ns	FBGA 2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.5	—	+0.5	ns	TSOP 2)3)4)5)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.5	—	0.5	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Address and control input hold time	t_{IH}	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)8)
Address and control input hold time	t_{IH}	1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)8)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)9)
Address and control input setup time	t_{IS}	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
Address and control input setup time	t_{IS}	1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.75	—	+0.75	ns	FBGA 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.75	—	+0.75	ns	TSOP 2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	t_{RCD} or t_{RASmin}		t_{RCD} or t_{RASmin}		ns	2)3)4)5)
Active to Precharge command	t_{RAS}	45	120E+3	45	120E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	65	—	65	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	20	—	ns	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)

Table 21 AC Timing - Absolute Specifications PC2100A and PC2100

Parameter	Symbol	–7		–7F		Unit	Note/ Test Condition 1)
		DDR266A		DDR266			
		Min.	Max.	Min.	Max.		
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	75	—	75	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	20	—	ns	2)3)4)5)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	15	—	ns	2)3)4)5)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)11)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)12)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V

2) Input slew rate ≥ 1 V/ns for DDR266, DDR266A

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

9) These parameters guarantee device timing, but they are not necessarily tested on each device.

10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

11) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

Table 22 I_{DD} Conditions

Parameter	Symbol
Operating Current: one bank; active/ precharge; $t_{RC} = t_{RCMIN}$; $t_{CK} = t_{CKMIN}$; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	I_{DD1}
Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{ILMAX}; $t_{CK} = t_{CKMIN}$	I_{DD2P}
Precharge Floating Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE ≥ V_{IHMIN}; $t_{CK} = t_{CKMIN}$, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE ≥ V_{IHMIN}; $t_{CK} = t_{CKMIN}$, address and other control inputs stable at ≥ V_{IHMIN} or ≤ V_{ILMAX}; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2Q}
Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{ILMAX}; $t_{CK} = t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD3P}
Active Standby Current: one bank active; $\overline{CS} \geq V_{IHMIN}$; CKE ≥ V_{IHMIN}; $t_{RC} = t_{RASMAX}$; $t_{CK} = t_{CKMIN}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$; I_{OUT} = 0 mA	I_{DD4R}
Operating Current: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$	I_{DD4W}
Auto-Refresh Current: $t_{RC} = t_{RFCMIN}$, burst refresh	I_{DD5}
Self-Refresh Current: CKE ≤ 0.2 V; external clock on; $t_{CK} = t_{CKMIN}$	I_{DD6}
Operating Current: four bank; four bank interleaving with BL = 4; Refer to the following page for detailed test conditions.	I_{DD7}

Table 23 I_{DD} Specifications

Symbol	DDR200 -8		DDR266A -7		DDR266 -7F		DDR333 -6		DDR400B -5		Unit	Note/Test Condition[1]
	typ.	max.	typ.	max.	typ.	max.	typ.	max.	typ.	max.		
I_{DD0}	70	90	75	100	83	110	85	110	70	90	mA	x4/x8 [3]
	72	95	77	105	86	115	88	115	75	90	mA	x16 [3]
I_{DD1}	80	100	90	110	98	120	100	120	80	100	mA	x4/x8 [3]
	83	105	94	115	102	125	104	125	95	110	mA	x16 [3]
I_{DD2P}	5	7	6	8	6	8	6	9	4	5	mA	[3]
I_{DD2F}	30	35	35	40	35	40	45	55	30	36	mA	[3]
I_{DD2Q}	18	22	20	25	20	25	25	28	20	28	mA	[3]
I_{DD3P}	13	16	15	18	15	18	18	21	13	18	mA	[3]
I_{DD3N}	40	45	50	55	50	55	60	65	38	45	mA	[3]
	42	50	52	60	52	60	63	70	43	54	mA	x16 [3]
I_{DD4R}	79	95	95	115	95	115	110	140	85	100	mA	x4/x8 [3]
	89	110	107	130	107	130	124	160	100	120	mA	x16 [3]
I_{DD4W}	85	105	105	125	105	125	125	145	90	105	mA	x4/x8 [3]
	96	120	119	140	119	140	141	165	100	130	mA	x16 [3]
I_{DD5}	126	170	135	180	135	180	144	190	140	190	mA	[3]
I_{DD6}	1.5	2.5	1.5	2.5	1.5	2.5	1.5	2.5	1.4	2.8	mA	standard power[3][4]
	1.20	1.25	1.20	1.25	1.20	1.25	1.20	1.25	—	—	mA	low power
I_{DD7}	150	210	171	225	171	225	208	270	210	250	mA	x4/x8 [3]
	158	220	180	235	180	235	218	285	210	250	mA	x16 [3]

1) Test conditions for typical values: V_{DD} = 2.5 V (DDR333), V_{DD} = 2.6 V (DDR400), T_A = 25 °C, test conditions for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

2) I_{DD} specifications are tested after the device is properly initialized and measured at 100 MHz for DDR200, 133 MHz for DDR266, 166 MHz for DDR333, and 200 MHz for DDR400.

3) Input slew rate = 1 V/ns.

4) Enables on-chip refresh and address counters.

4.4.1 I_{DD} Current Measurement Conditions

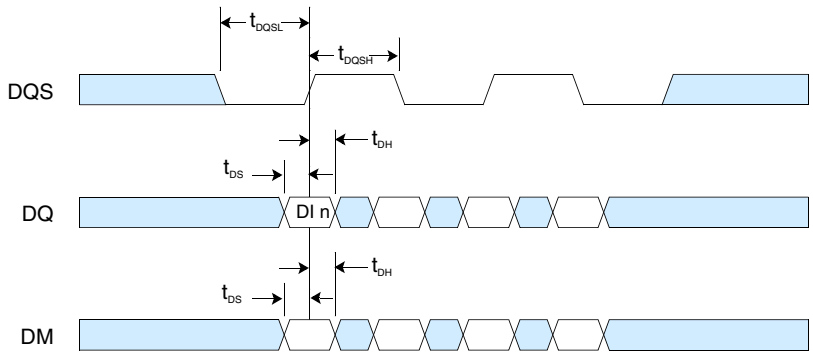
I_{DD1}: Operating Current: One Bank Operation

1. Only one bank is accessed with tRC(min) , Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0 mA.
2. Timing patterns
   a) **DDR200** (100MHz, CL=2) : t_{CK} = 10 ns, CL=2, BL=4, $t_{RCD} = 2 \times t_{CK}$, $t_{RAS} = 5 \times t_{CK}$
   Setup: A0 N R0 N N P0 N
   Read : A0 N R0 N N P0 N - repeat the same timing with random address changing
   50% of data changing at every burst changing at every burst
   b) **DDR266** (133MHz, CL=2) : t_{CK} = 7.5 ns, CL=2, BL=4, $t_{RCD} = 3 \times t_{CK}$, $t_{RC} = 9 \times t_{CK}$, $t_{RAS} = 5 \times t_{CK}$
   Setup: A0 N N R0 N P0 N N N
   Read : A0 N N R0 N P0 N NN - repeat the same timing with random address changing
   50% of data changing at every burst
   c) **DDR333** (166MHz, CL=2.5) : tCK = 6 ns, CL=2.5, BL=4, $t_{RCD} = 3 \times t_{CK}$, $t_{RC} = 9 \times t_{CK}$, $t_{RAS} = 5 \times t_{CK}$
   Setup: A0 N N R0 N P0 N N N
   Read : A0 N N R0 N P0 N N N - repeat the same timing with random address changing
   50% of data changing at every burst
   d) **DDR400B** (200 MHz, CL = 3): t_{CK} = 5 ns, BL = 4, $t_{RCD} = 3 \times t_{CK}$, $t_{RC} = 11 \times t_{CK}$, $t_{RAS} = 8 \times t_{CK}$
   Setup:A0 N N R0 N N N N P0 N N
   Read: A0 N N R0 N N N N P0 N N -repeat the same timing with random address changing
3. Legend: A = Activate, R = Read, W = Write, P = Precharge, N = NOP

I_{DD7}: Operating Current: Four Bank Operation

1. Four banks are being interleaved with t_{RCMIN}. Burst Mode, Address and Control inputs on NOP edge are not changing. I_{OUT} = 0 mA.
2. Timing patterns
   a) **DDR200** (100 MHz, CL = 2): t_{CK} = 10 ns, CL = 2, BL = 4, $t_{RRD} = 2 \times t_{CK}$, $t_{RCD} = 3 \times t_{CK}$, Read with autoprecharge
   Setup: A0 N A1 R0 A2 R1 A3 R2
   Read: A0 R3 A1 R0 A2 R1 A3 R2 - repeat the same timing with random address changing
   50% of data changing at every burst
   b) **DDR266A** (133 MHz, CL = 2): t_{CK} = 7.5 ns, CL = 2, BL = 4, $t_{RRD} = 2 \times t_{CK}$, $t_{RCD} = 3 \times t_{CK}$
   Setup: A0 N A1 R0 A2 R1 A3 R2 N R3
   Read: A0 N A1 R0 A2 R1 A3 R2 N R3 - repeat the same timing with random address changing
   50% of data changing at every burst
   c) **DDR333** (166 MHz, CL = 2.5): t_{CK} = 6 ns, CL = 2.5, BL = 4, $t_{RRD} = 2 \times t_{CK}$, $t_{RCD} = 3 \times t_{CK}$
   Setup: A0 N A1 R0 A2 R1 A3 R2 N R3
   Read: A0 N A1 R0 A2 R1 A3 R2 N R3 - repeat the same timing with random address changing
   50% of data changing at every burst
   d) **DDR400B** (200 MHz, CL = 3): t_{CK} = 5 ns, BL = 4, $t_{RRD} = 2 \times t_{CK}$, $t_{RCD} = 3 * \times t_{CK}$, $t_{RAS} = 8 \times t_{CK}$
   Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N
   Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N - repeat the same timing with random address
3. Legend: A = Activate, R = Read, W = Write, P = Precharge, N = NOP

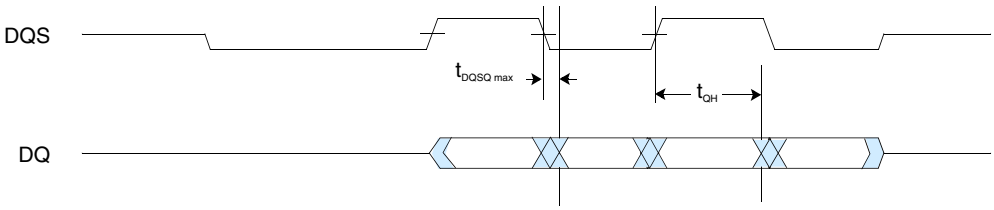
5 Timing Diagrams



DI n = Data In for column n.
3 subsequent elements of data in are applied in programmed order following DI n.

Don't Care

Figure 38 Data Input (Write), Timing Burst Length = 4



t_{QH} (Data output hold time from DQS)

t_{DQSQ} and t_{QH} are only shown once and are shown referenced to different edges of DQS, only for clarify of illustration.
t_{DQSQ} and t_{QH} both apply to each of the four relevant edges of DQS.

$t_{DQSQ\ max.}$ is used to determine the worst case setup time for controller data capture.
t_{QH} is used to determine the worst case hold time for controller data capture.

Figure 39 Data Output (Read), Timing Burst Length = 4

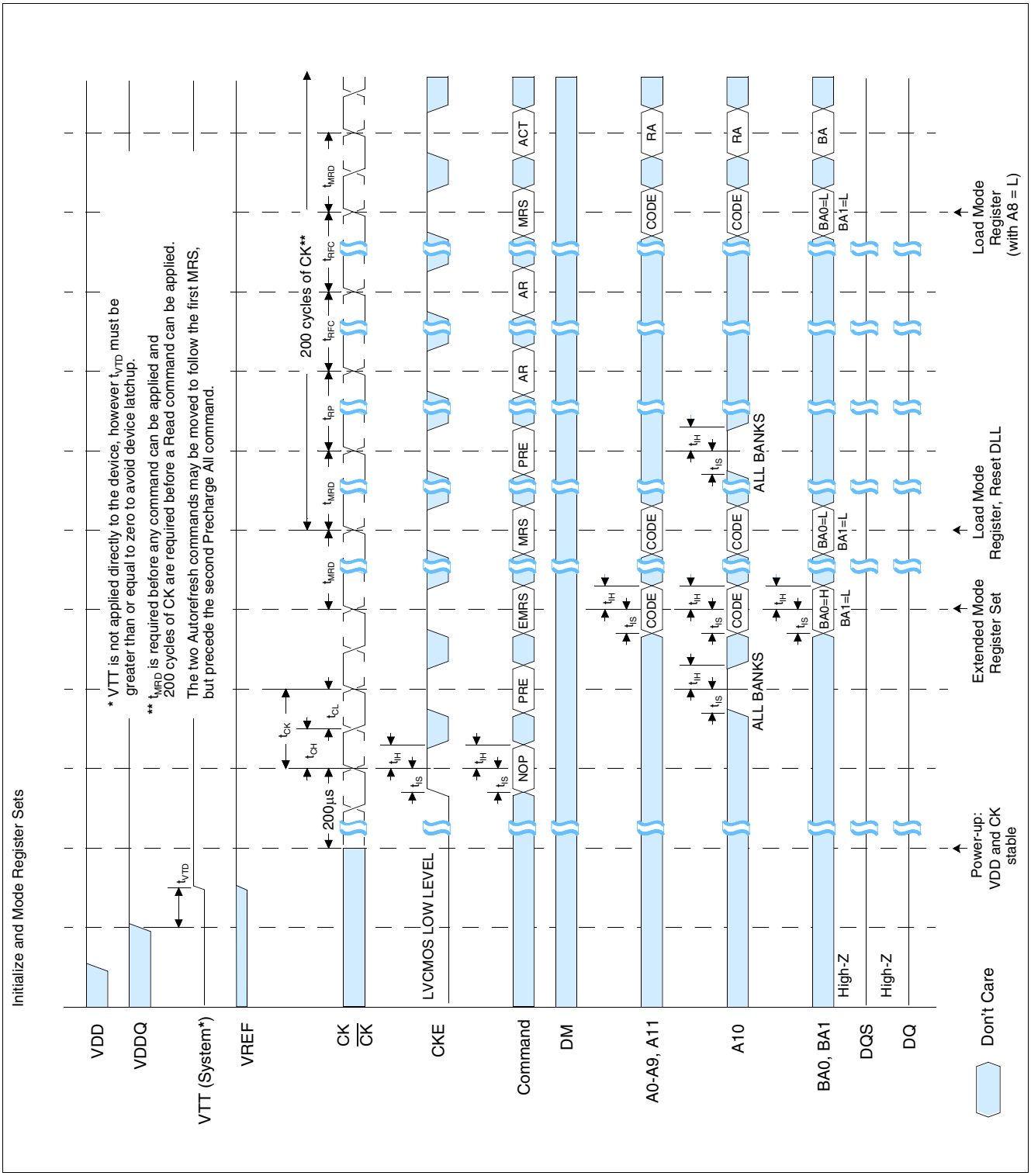


Figure 40 Initialize and Mode Register Sets

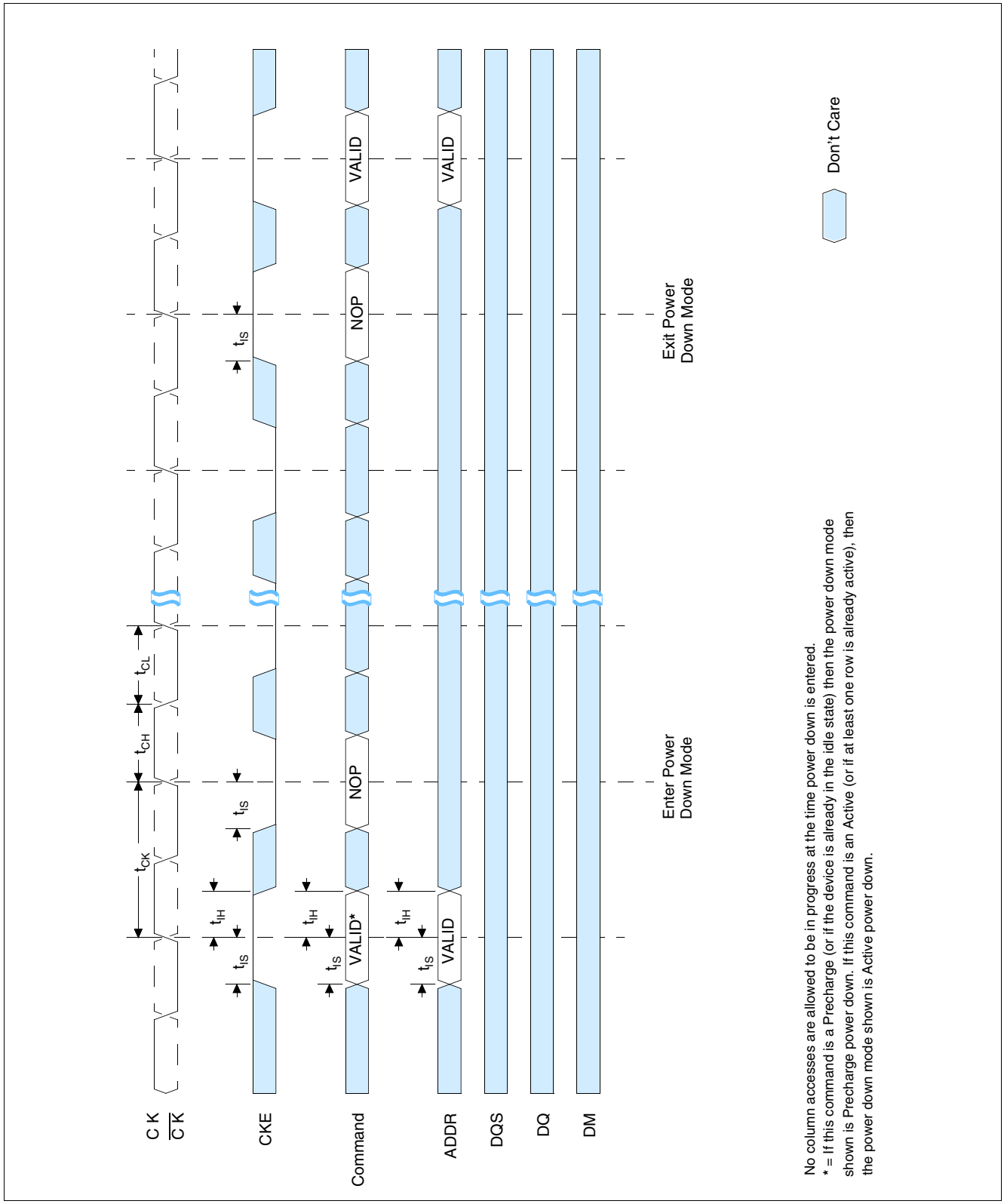


Figure 41 Power Down Mode

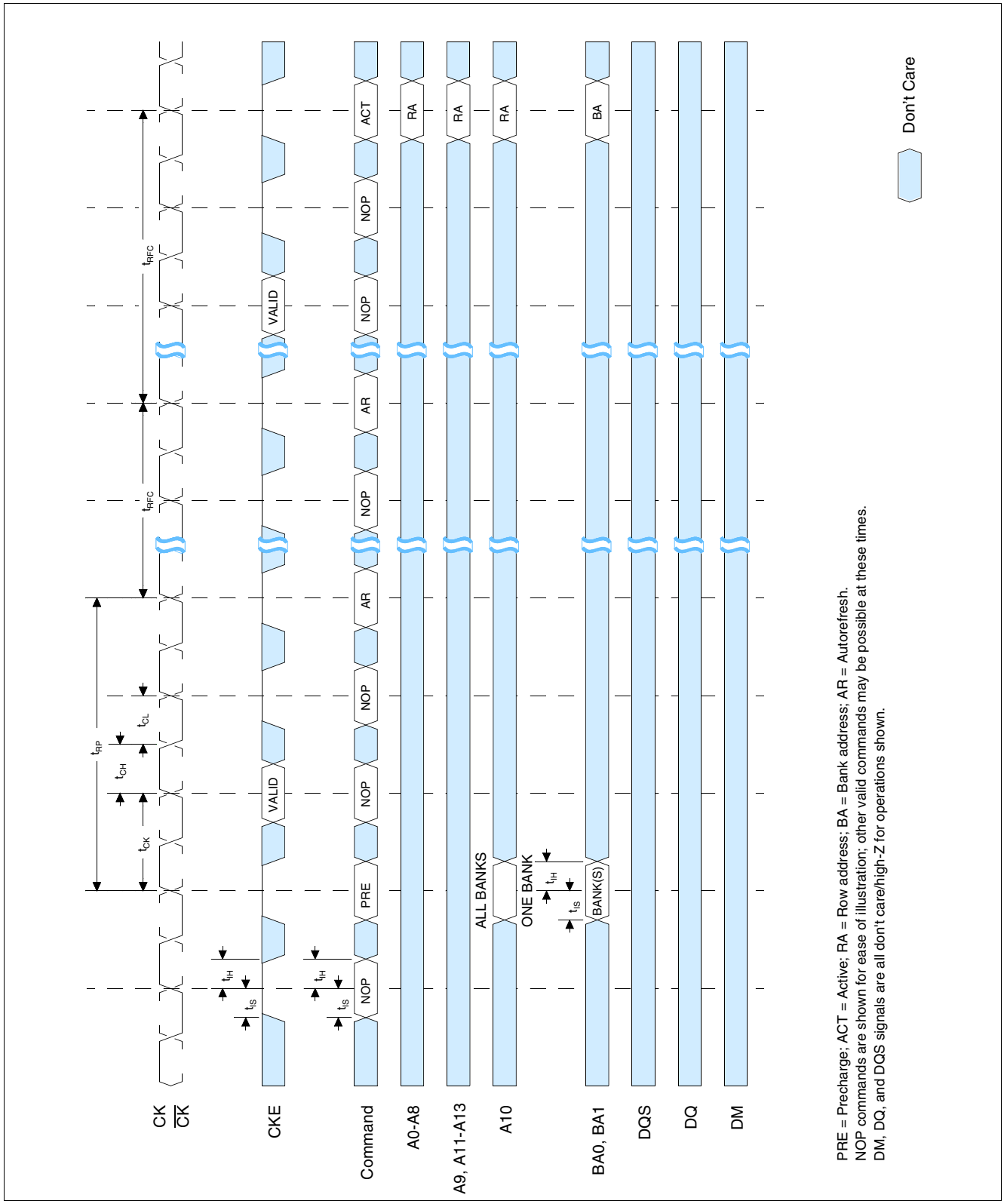


Figure 42 Auto Refresh Mode

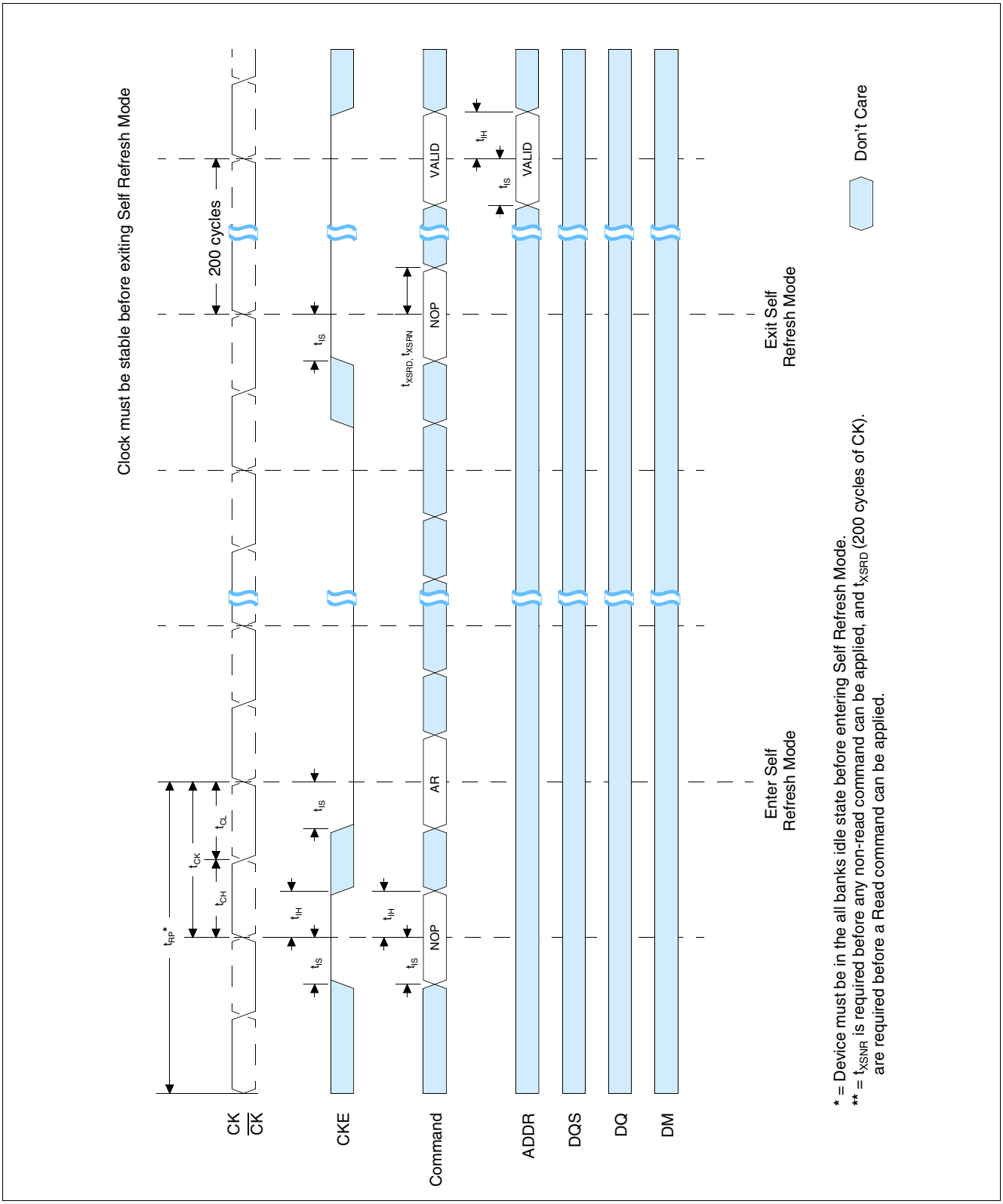


Figure 43 Self Refresh Mode

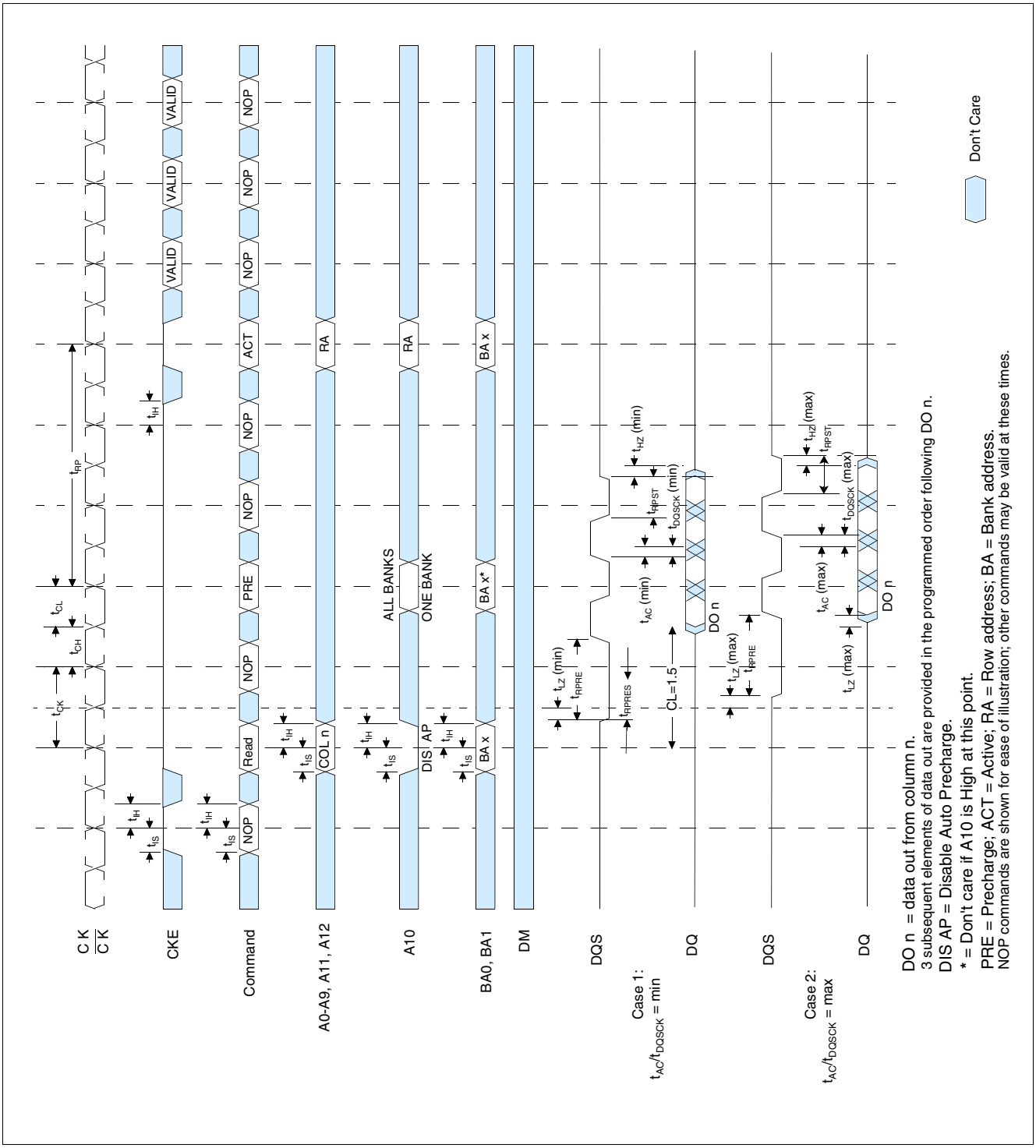


Figure 44 Read without Auto Precharge (Burst Length = 4)

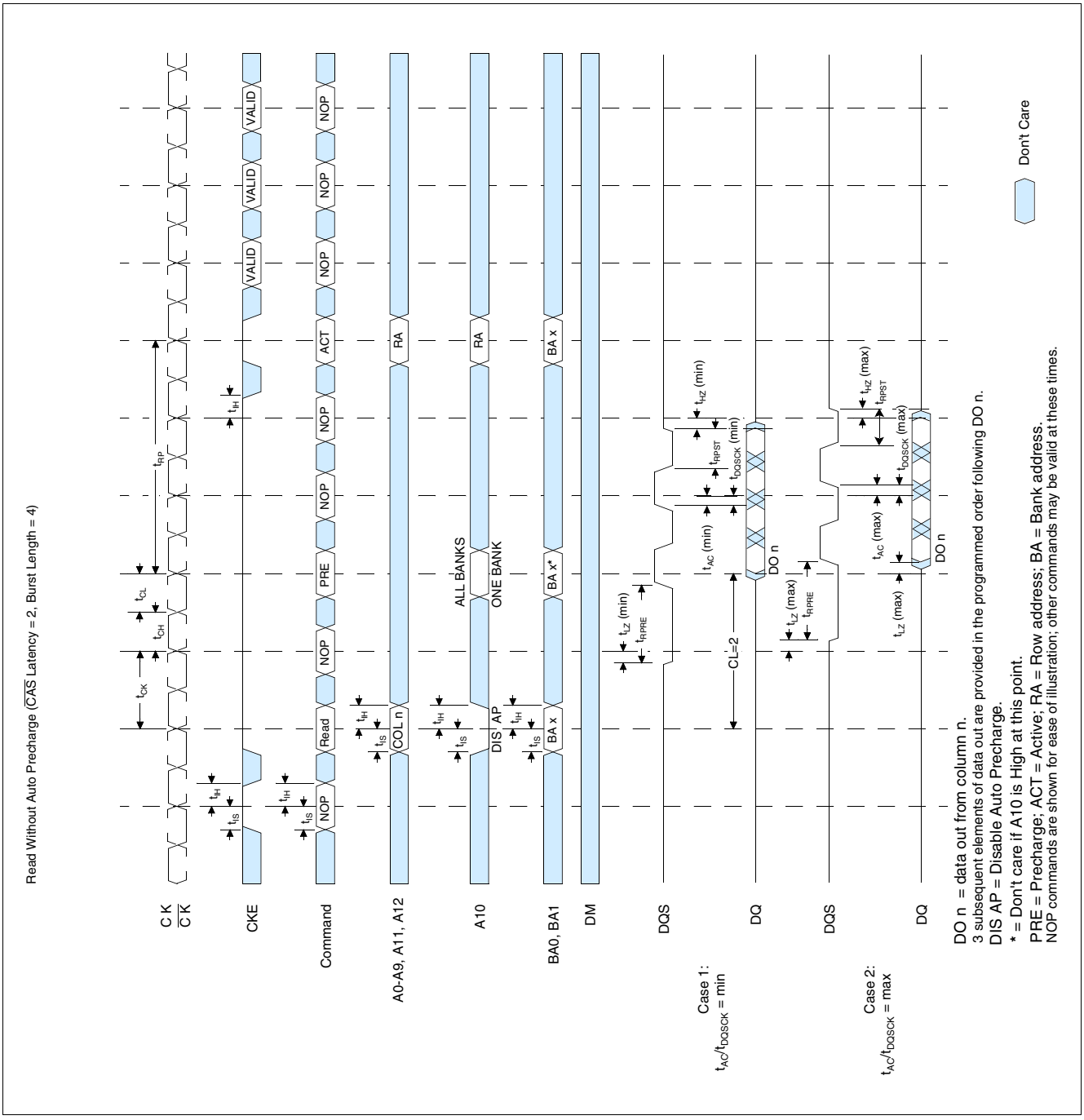


Figure 45 Read with Auto Precharge (Burst Length = 4)

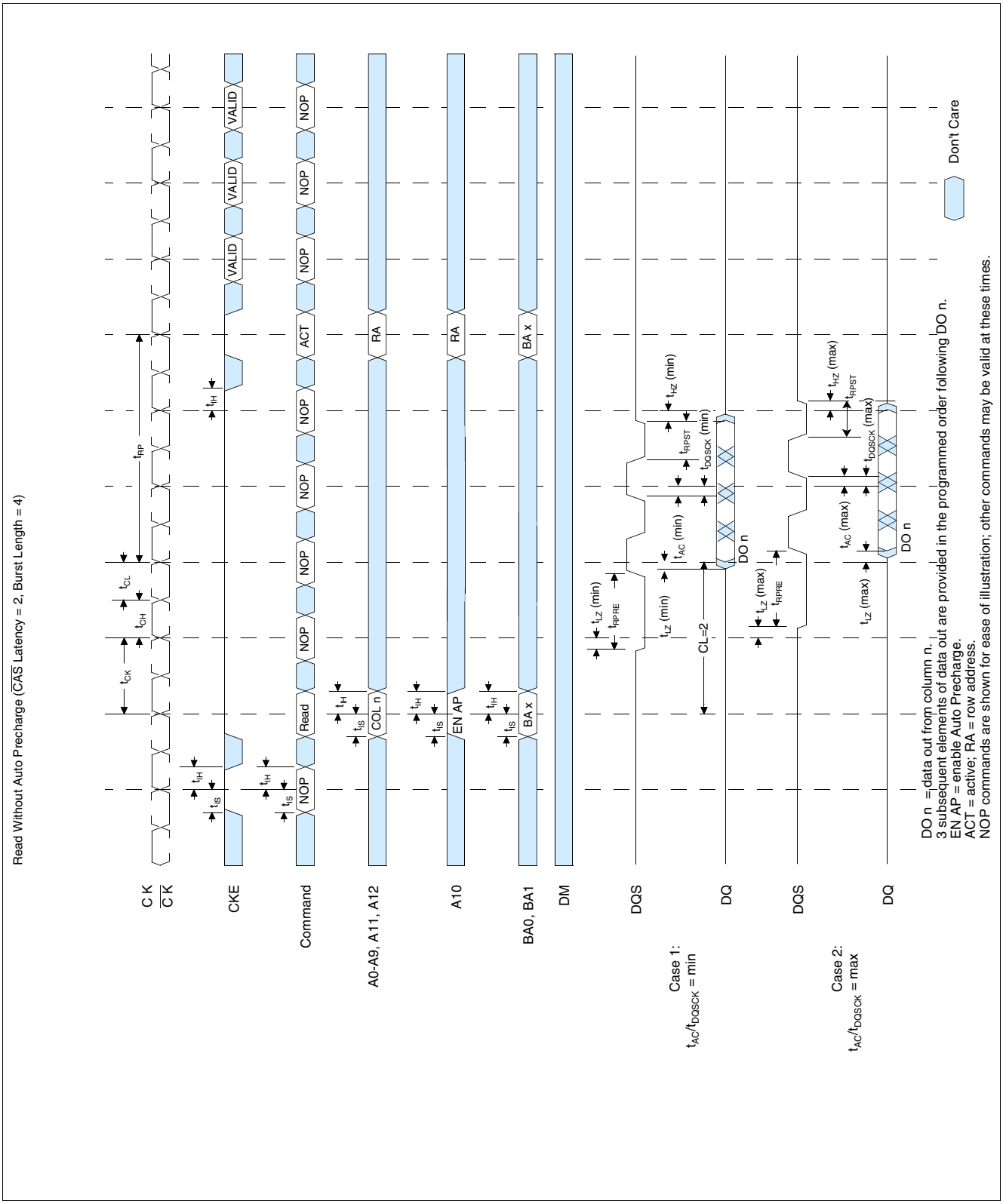


Figure 46 Bank Read Access (Burst Length = 4)

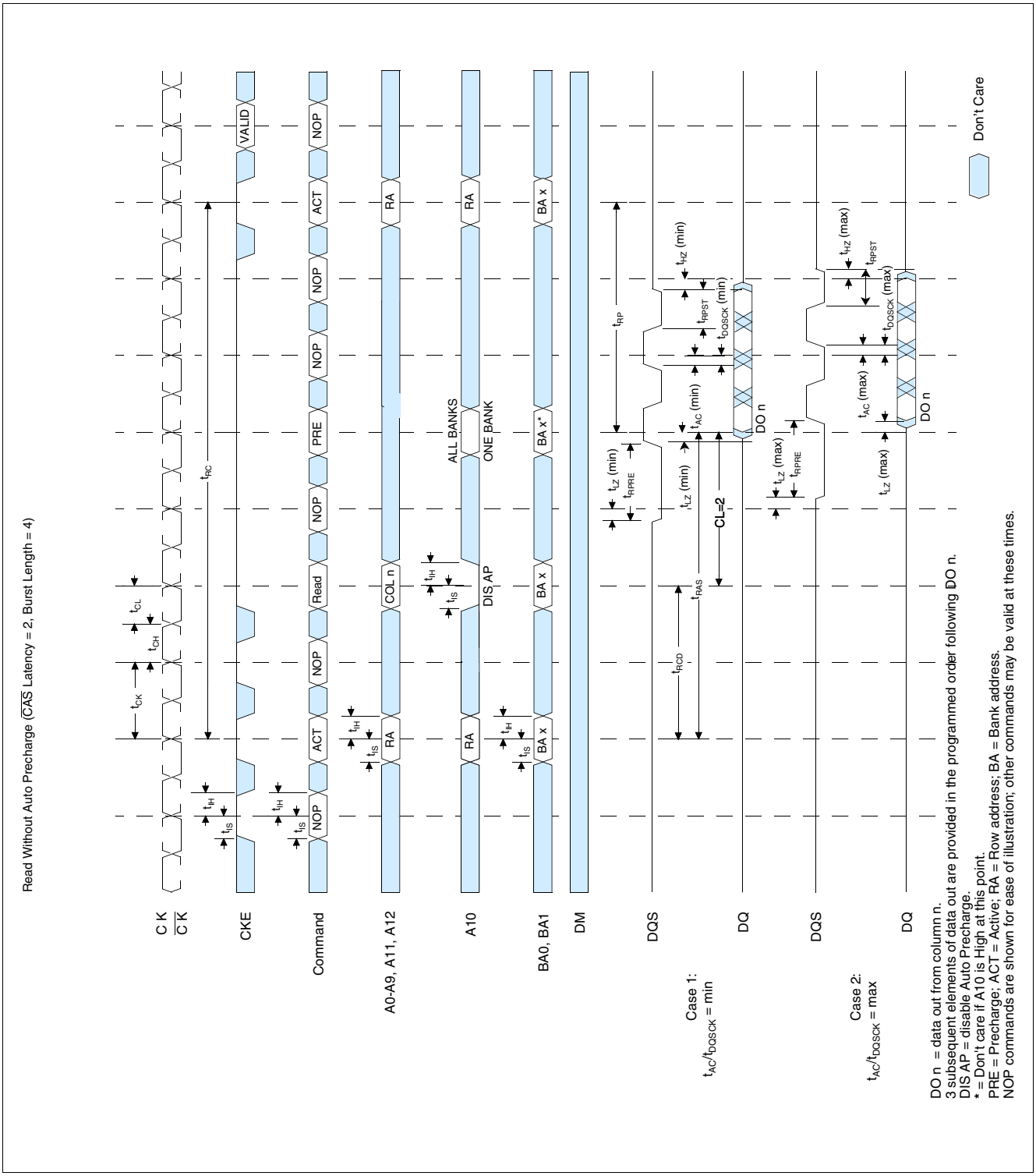


Figure 47 Write without Auto Precharge (Burst Length = 4)

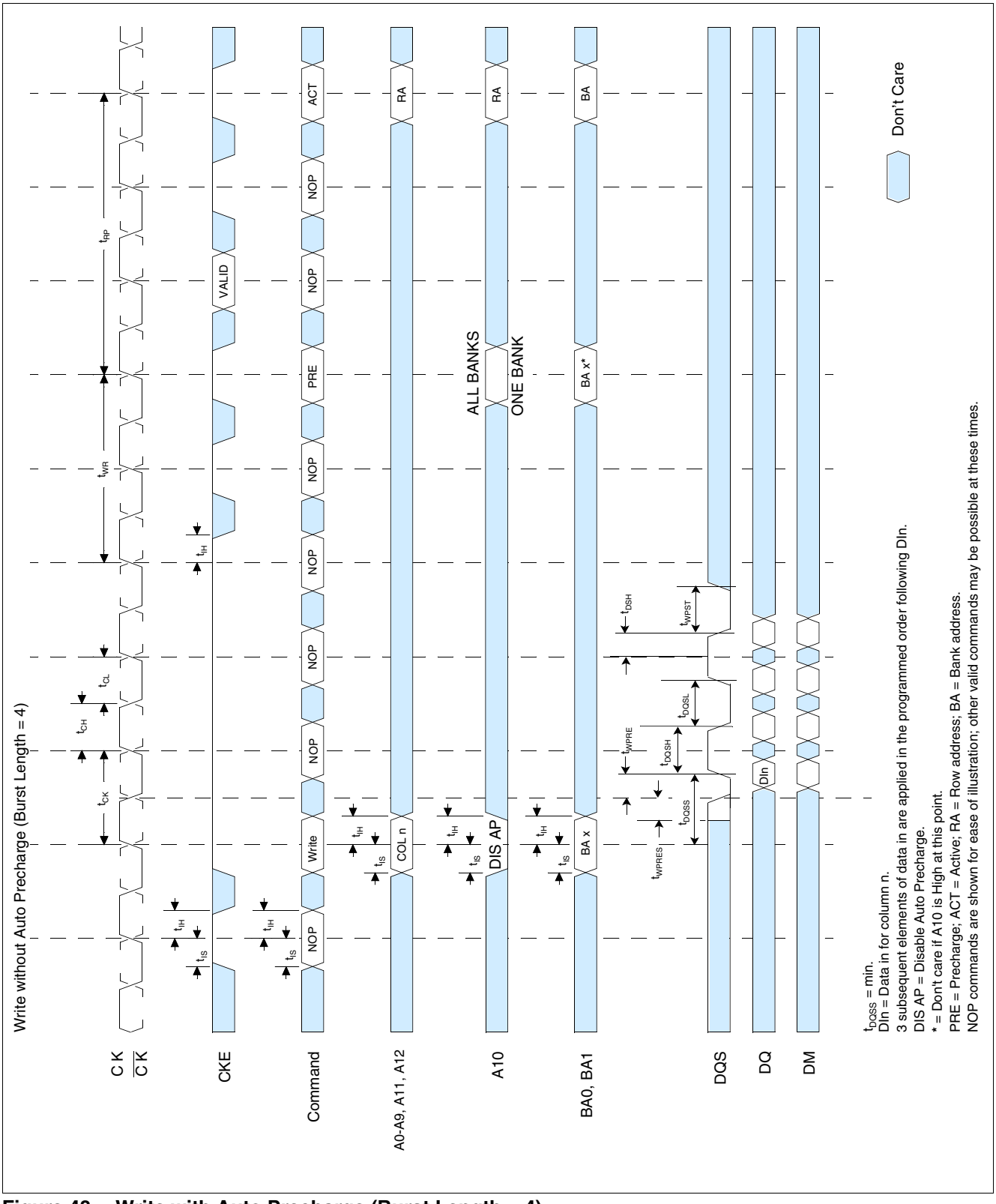


Figure 48 Write with Auto Precharge (Burst Length = 4)

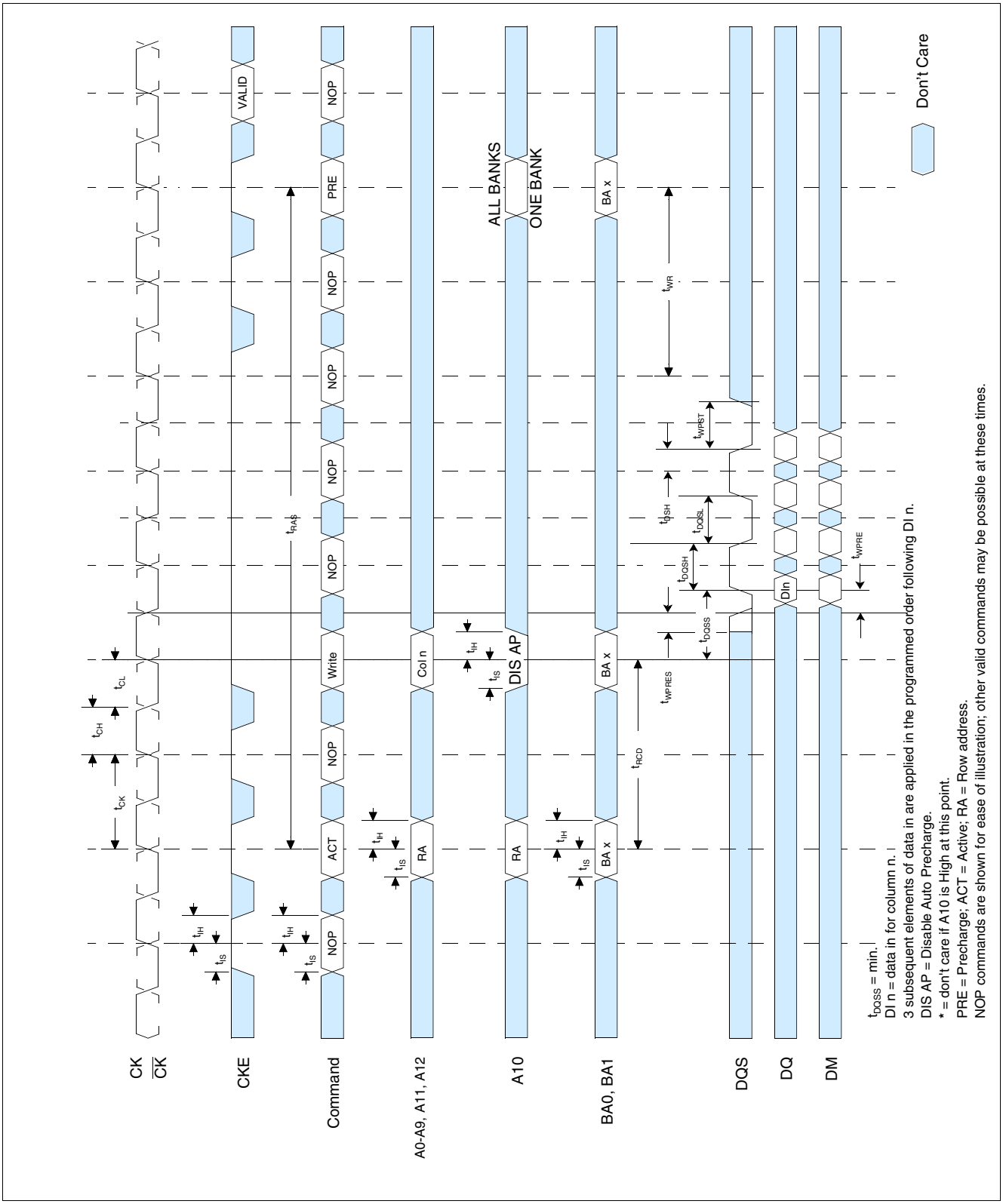


Figure 49 Bank Write Access (Burst Length = 4)

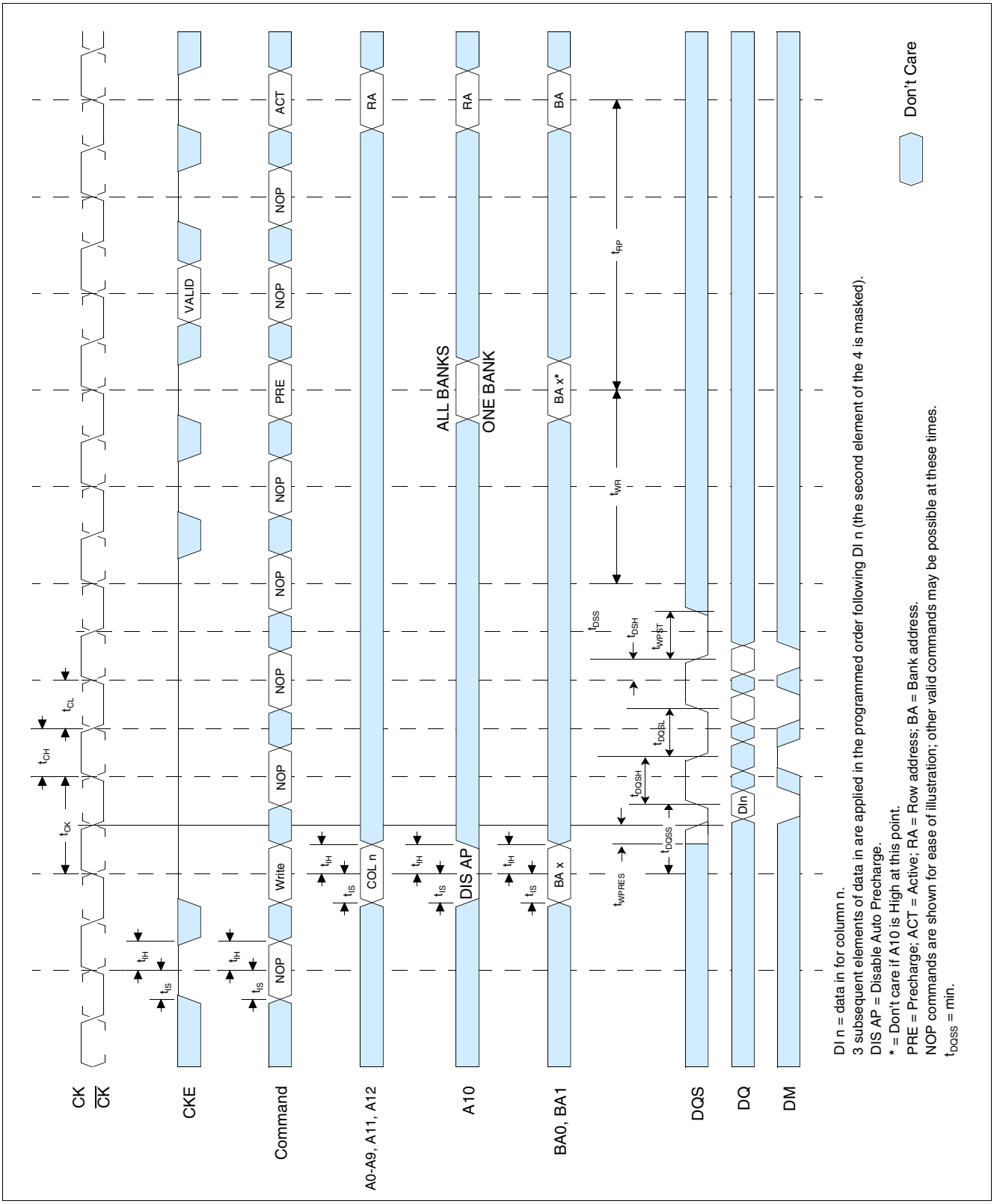
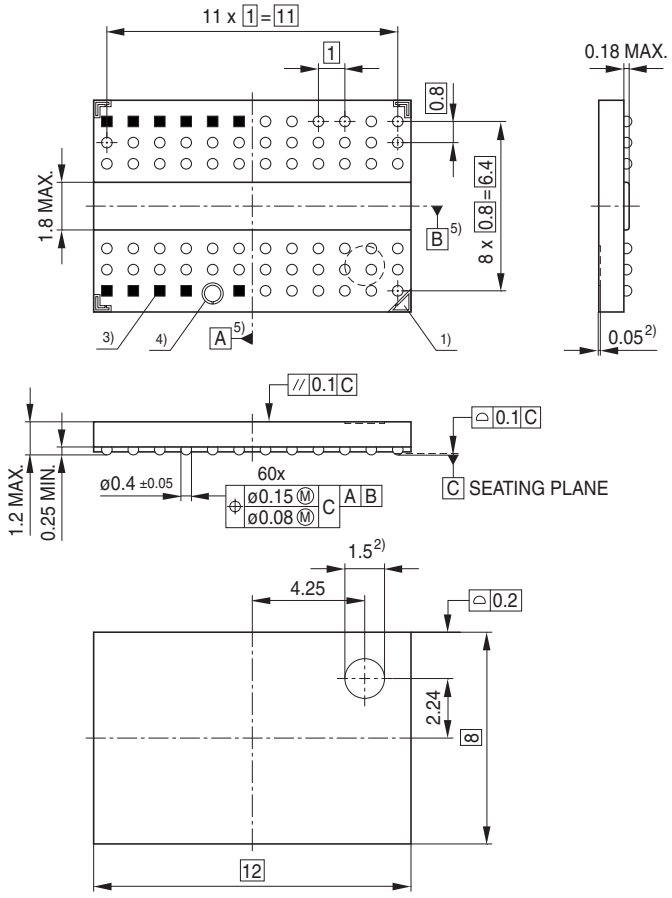


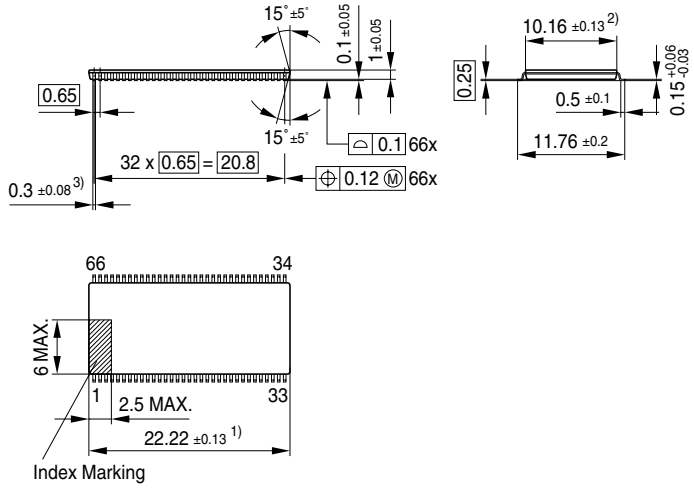
Figure 50 Write DM Operation (Burst Length = 4)

6 Package Outlines



1) A1 Marking Ballside
2) A1 Marking Chipside
3) Dummy Pads without Ball ■
4) Bad Unit Marking (BUM)
5) Middle of Packages Edges

Figure 51 **P-TFBGA-60-2** (Plastic Thin Fine-Pitch Ball Grid Array Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include plastic protrusion of 0.25 max. per side
3) Does not include dambar protrusion of 0.13 max.

Figure 52 P-TSOPII-66-1 (Plastic Thin Small Outline Package Type II)

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