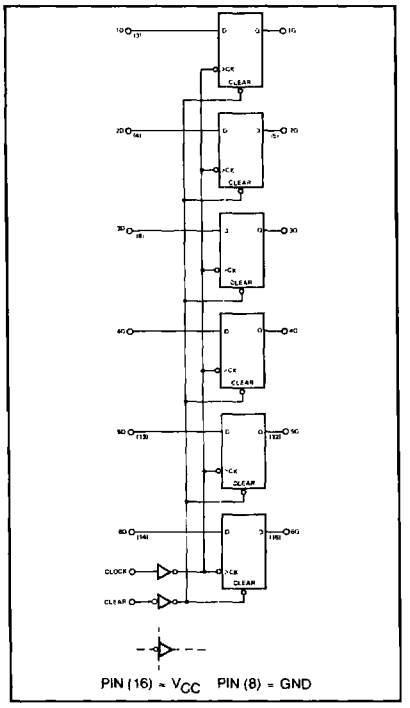
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

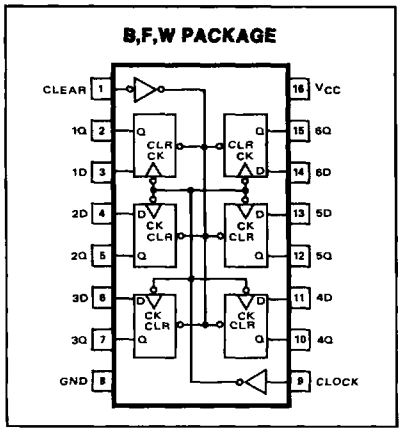
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE (Each Flip-Flop)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_w	Width of pulse Clock			20			20			12			ns
	Clear												
t_{Setup}	Input setup time												ns
	Data			20			20↑			8			
	Clear inactive			25			25↑			15			
t_{Hold}	Input hold time			0			5↑			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	ns
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PHL}	High-to-low	Clear	Q		23	35		23	35		13	22	

Load circuit and typical waveforms are shown at the front of section.