



High Speed SRAM

128K-Word By 8 Bit

CS18HS10243

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
1.2	Add green code in part no.	Jul.22,2005	
1.3	Remove 32PIN STSOP	Jun.12,2006	



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■ DESCRIPTION

The CS18HS10243 series products are 131,072-words by 8-bits static RAM fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the CS18HS10243 series products exhibit very high-speed performance with single +3.3-volt power supply while requiring very low power and no clock or refreshing to operate. The CS18HS10243 is packed in a standard 32L SOJ-300mil, 32L SOP-450mil, 32L TSOP(I)-8x20mm and 32L PDIP-300mil.

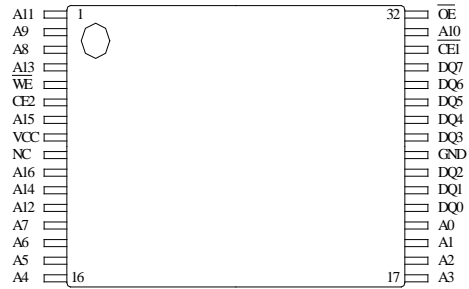
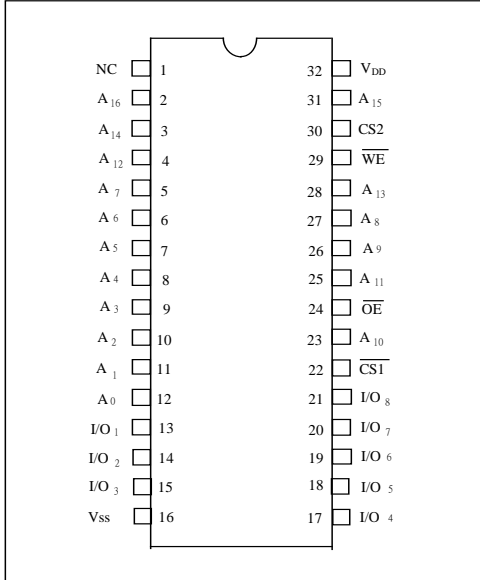
■ FEATURES

1. 131,072-word x 8-bit organization
2. Low operation voltage: 3.0 ~ 3.6V
3. Fully static operation - no clock or refreshing required
4. LVTTTL-compatible inputs and outputs
5. Common I/O capability
6. Low power consumption
 - Active: 120/110 mA (Max.)
 - Standby: 2 mA
7. Very high speed access: 12/15 ns (Max.)
8. Output Enable (\overline{OE}) available for very fast access

■ Product Family

Part No.	Operating Temp	Vcc. Range	Speed (ns)	Supply Current mA (Max.)		Package Type
				Operating	Standby	
CS18HS10243CC	0~70°C	3.0~3.6V	12	120	2	32 SOP-450mil
CS18HS10243SC						32 SOJ-300mil
CS18HS10243EC			110	32TSOP-8x20mm		
CS18HS10243TC			15	32PDIP-300mil		

■ PIN CONFIGURATIONS



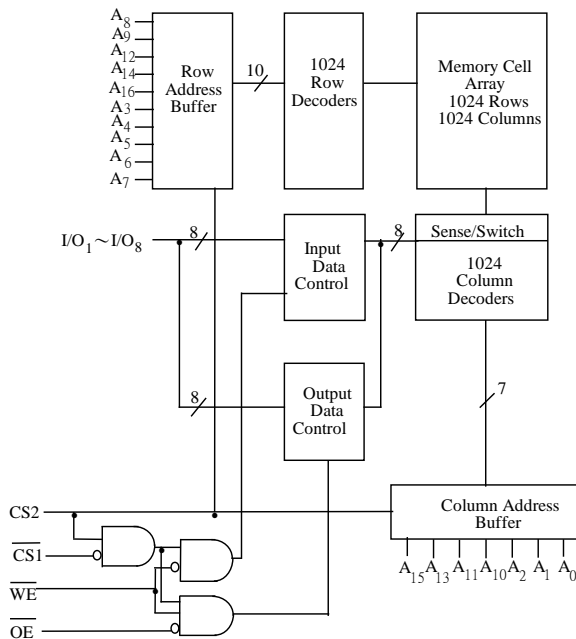
32L TSOP(I)-8x20mm

32L PDIP- 300 mil

32L SOP - 450 mil

32L SOJ - 300 mil

■ BLOCK DIAGRAM





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■ PIN DESCRIPTIONS

Symbols	Functions
A0~A16	Address Inputs
I/O1~I/O8	Data Inputs / Outputs
$\overline{CS}1, CS2$	Chip Select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
VDD	Power Supply
VSS	Ground

■ TRUTH TABLE

\overline{CS}	CS2	\overline{OE}	\overline{WE}	Mode	I/O1~I/O8	VDD Current
H	X	X	X	Not Selected	High Z	I _{sb} , I _{sb1}
X	L	X	X	Not Selected	High Z	I _{sb} , I _{sb1}
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

■ ABSOLUTE MAXIMUM RATINGS

Parameters	Rating	Unit
Supply Voltage to Vss	-0.5 to +5.5	V
Input/Output to Vss	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

■ OPERATING RANGE

Range	Ambient Temperature	V _{cc}
Commercial	0~70°C	3.3V±10%



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■ DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{SS} = 0V, T_a = 0 to 70°C)

Parameters	Symbols	Test Conditions	Min.	Typ.	Max	Unit	
Input Low Voltage	V _{IL}	-	-0.3	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.3	-	V _{DD} +0.3	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , \overline{CS} = V _{IH} or \overline{OE} = V _{IH} or \overline{WE} = V _{IL}	-10	-	+10	μA	
Output Low Voltage	V _{OL}	I _{OL} = +8.0mA	-	-	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	-	-	V	
Operating Power Supply Current	I _{DD}	\overline{CS} = V _{IL} , I/O = 0 mA	12	-	-	120	mA
		Cycle = MIN	15	-	-	110	mA
		Duty = 100%					mA
Standby Power Supply Current	I _{SB}	\overline{CS} = V _{IH} , Cycle = MIN Duty = 100%	-	-	10	mA	
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	2	mA	

Note: Typical characteristics are measured at V_{DD} = 3.3V, T_a = 25°C

■ AC Characteristics: Capacitances

(V_{DD} = 3.3V, T_a = 25°C, f = 1 MHz)

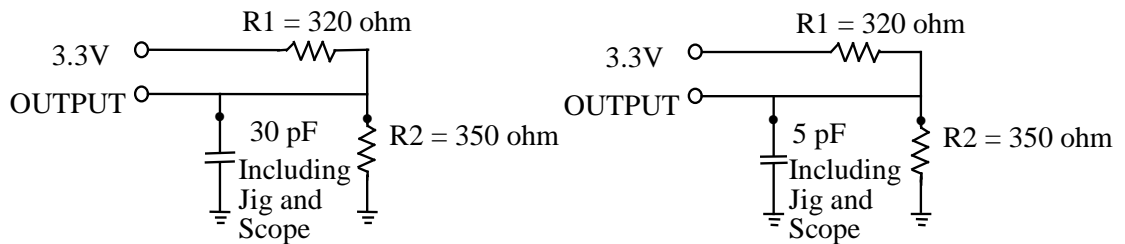
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

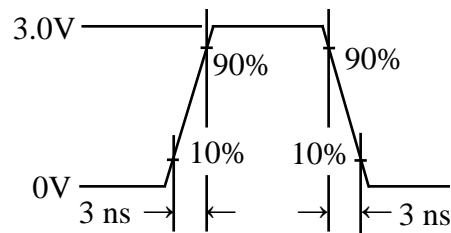
AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 30 \text{ pF}$, $I_{OH}/I_{OL} = -4 \text{ mA} / 8 \text{ mA}$

■ AC Test Loads and Waveforms



(For T_{CLZ} , T_{OLZ} , T_{CHZ} , T_{OHZ} , T_{WHZ} , T_{OW})





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■ AC Performances:

(V_{DD} = 3.3V, V_{SS} = 0V, Ta = 0 to 70°C)

(1) Read Cycle

Parameters	Symbols	CS18HS10243-12		CS18HS10243-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	TRC	12	-	15	-	ns
Address Access Time	TAA	-	12	-	15	ns
Chip Select Access Time	TACS	-	12	-	15	ns
Output Enable to Output Valid	TAOE	-	7	-	8	ns
Chip Selection to Output in Low Z	TCLZ*	3	-	3	-	ns
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	ns
Chip Deselection to Output in High Z	TCHZ*	-	6	-	7	ns
Output Disable to Output in High Z	TOHZ*	-	6	-	7	ns
Output Hold from Address Change	TOH	3	-	3	-	ns

*These parameters are sampled but not 100% tested

(2) Write Cycle

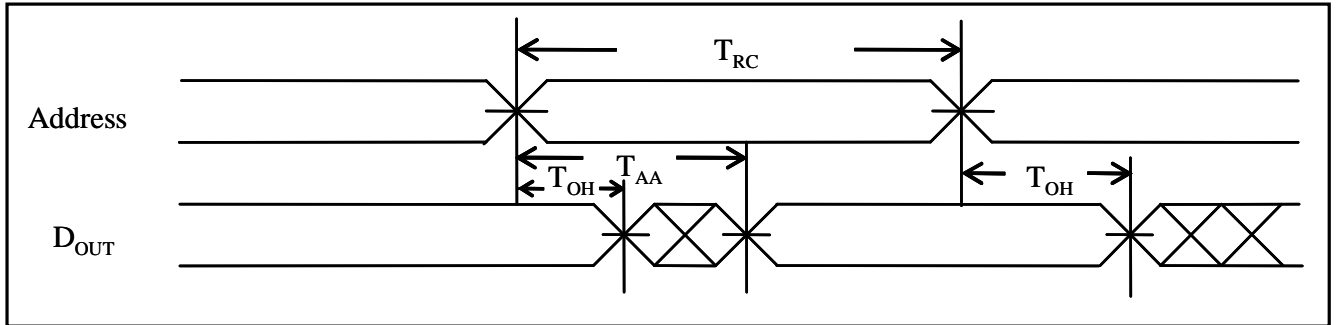
Parameters	Symbols	CS18HS10243-12		CS18HS10243-15		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	TWC	12	-	15	-	ns
Chip Selection to End of Write	TCW	10	-	12	-	ns
Address Valid to End of Write	TAW	10	-	12	-	ns
Address Setup Time	TAS	0	-	0	-	ns
Write Pulse Width	TWP	10	-	12	-	ns
Write Recovery Time	TWR	0	-	0	-	ns
Data Valid to End of Write	TDW	8	-	10	-	ns
Data Hold from End of Write	TDH	0	-	0	-	ns
Write to Output in High Z	TWHZ*	-	6	-	7	ns
Output Disable to Output in High Z	TOHZ*	-	6	-	7	ns
Output Active from End of Write	TOW	0	-	0	-	ns

These parameters are sampled but not 100% tested

■ Timing Waveforms

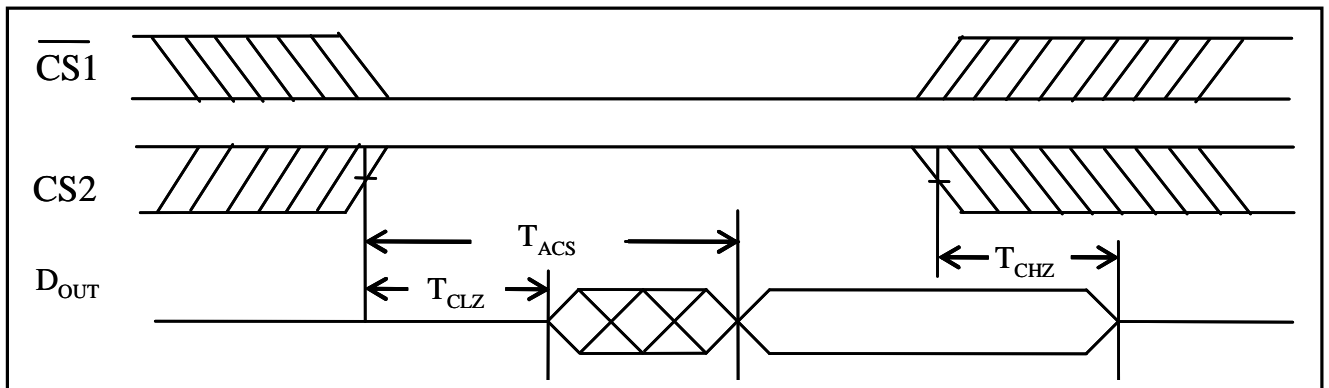
Read Cycle 1

(Address Controlled)



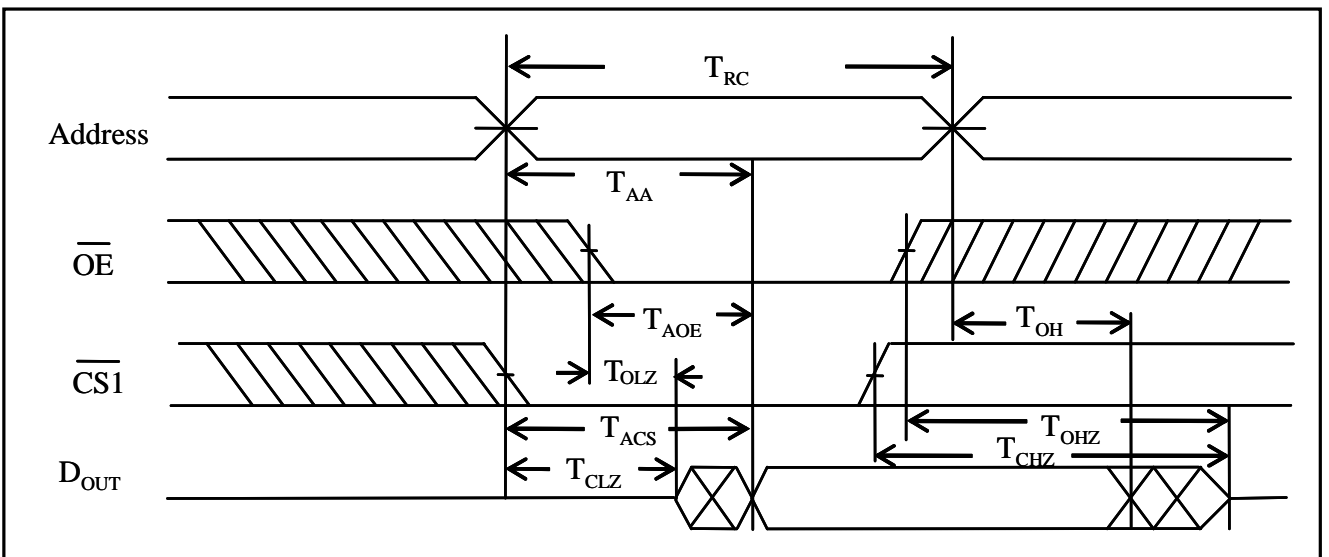
Read Cycle 2

(Chip Select Controlled)



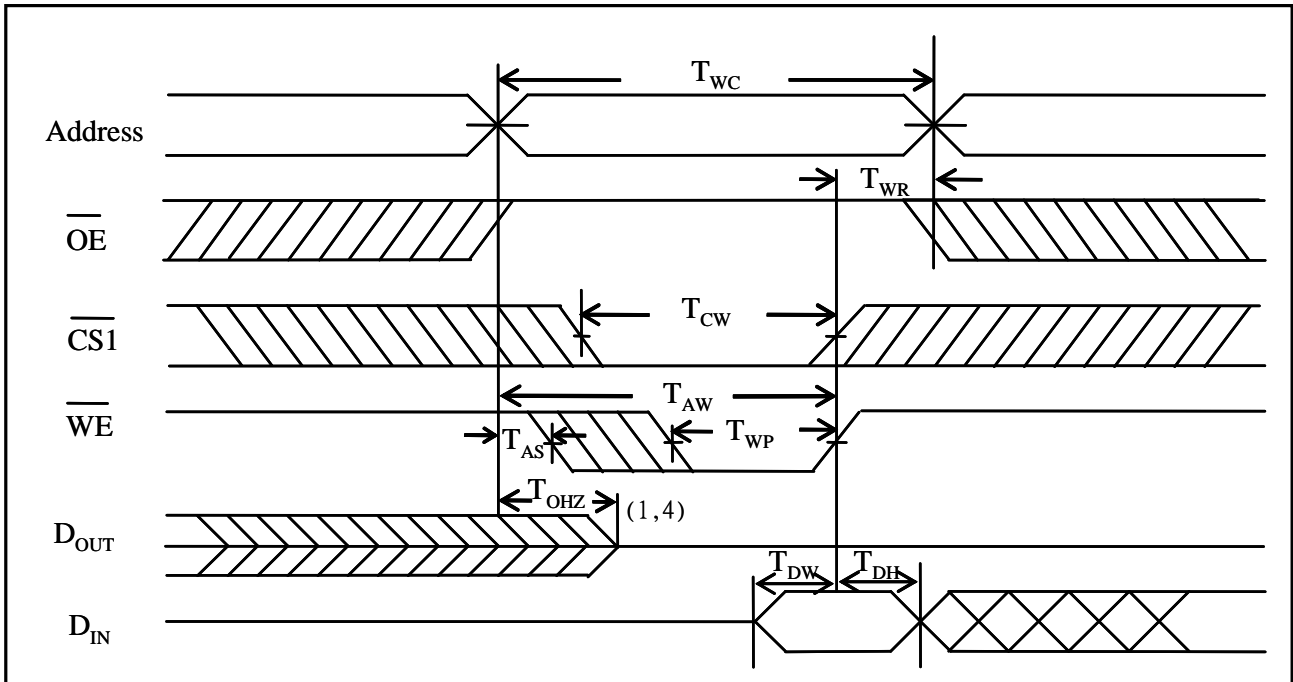
Read Cycle 3

(Output Enable Controlled)



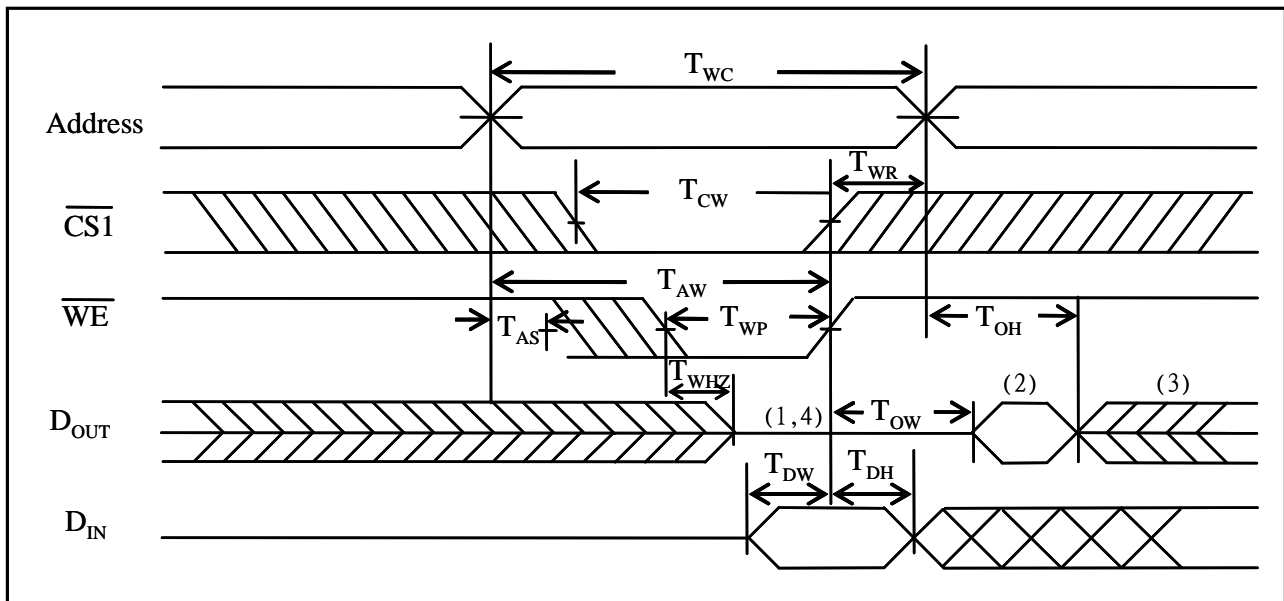
Write Cycle 1

($\overline{\text{OE}}$ Clock)



Write Cycle 2

($\overline{\text{OE}} = \text{VIL Fixed}$)

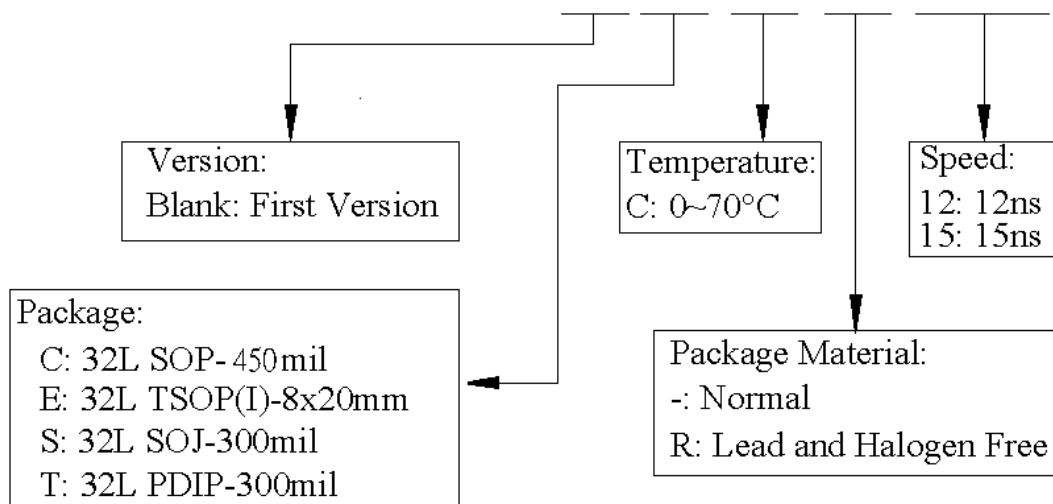


Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured $\pm 500\text{mV}$ from steady state with $\text{CL} = 5\text{pF}$. This parameter is guaranteed but not 100% tested.

■ ORDER INFORMATION

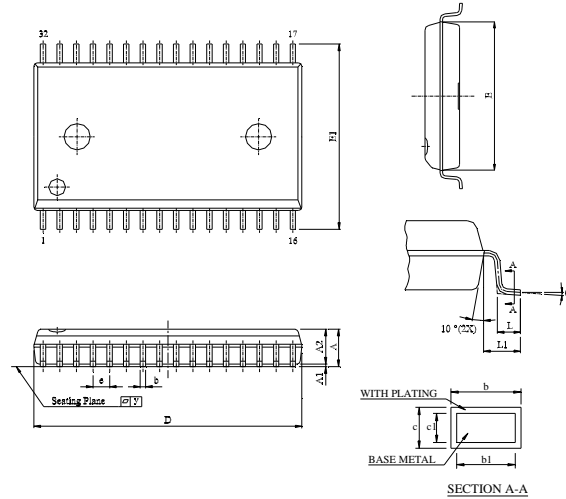
CS18HS10243 X X X X XX



Note: Package material code "R" meets ROHS

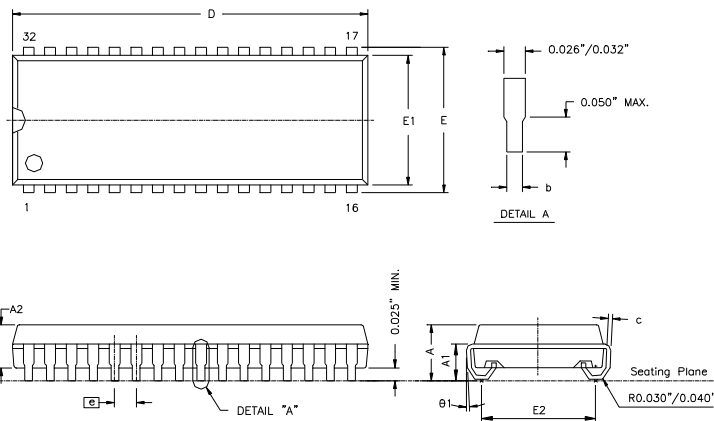
■ PACKAGE DIMENSIONS

- 32 SOP - 450 mil



SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	-	0°
	Nom.	2.821	0.229	2.680	-	-	-	-	20.447	11.303	14.097	1.270	0.834	1.397	-	-
	Max.	2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	-	0°
	Nom.	0.111	0.009	0.1055	-	-	-	-	0.805	0.445	0.555	0.050	0.033	0.055	-	-
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

- 32 SOJ - 300 mil



SYMBOL		A	A1	A2	b	c	D	E	E1	E2	e	θ
mm	Min.	3.10	2.08	2.41	0.41	0.18	20.83	8.53	7.49	6.78	1.27	0°
	Nom.	3.35	-	2.54	0.46	0.20	20.96	bsc	7.62	bsc	bsc	-
	Max.	3.61	-	2.67	0.51	0.33	21.08	-	7.75	-	-	10°
inch	Min.	0.122	0.082	0.095	0.016	0.007	0.820	0.336	0.295	0.267	0.050	0°
	Nom.	0.132	-	0.100	0.018	0.008	0.825	bsc	0.300	bsc	bsc	-
	Max.	0.142	-	0.105	0.020	0.013	0.830	-	0.305	-	-	10°

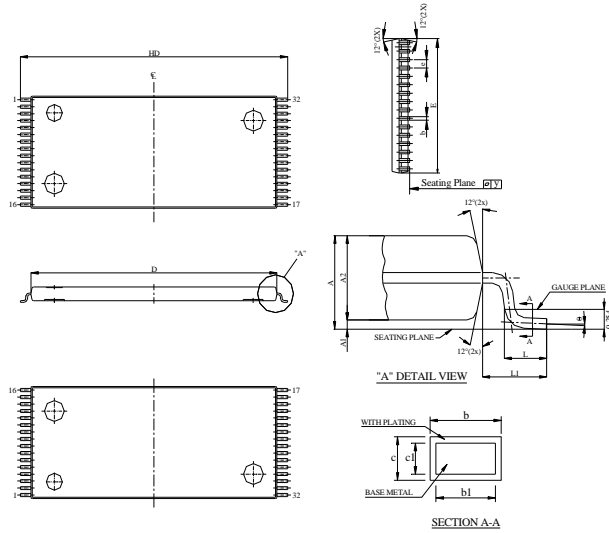


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- 32TSOP – 8x20mm



SYMBOL	A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	18.30	7.90	0.40	19.80	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	18.40	8.00	0.50	20.00	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	0.724	0.315	0.020	0.787	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004

- 32PDIP – 300mil

