

December 1992

Radiation Hardened Dual-D Flip-Flop with Set and Reset

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(SI)
- Dose Rate Upset $>10^{10}$ RAD(SI)/s 20ns Pulse
- Cosmic Ray Upset Rate 2×10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
 - VIL = 0.8V Max
 - VIH = VCC/2 Min
- Input Current Levels II $\leq 5\mu A$ at VOL, VOH

Description

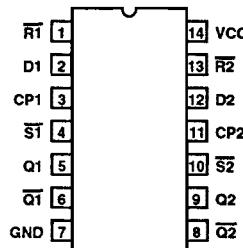
The Harris HCTS74MS is a Radiation Hardened positive edge triggered flip-flop with set and reset.

The HCTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

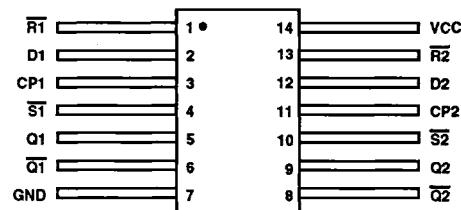
The HCTS74MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

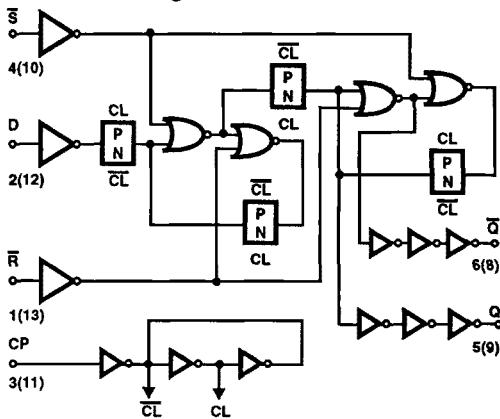
INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	/	H	H	L
H	H	/	L	L	H
H	H	L	X	Q0	$\bar{Q}0$

NOTE: L = Logic Level Low, H = Logic Level High, X = Don't Care
 / = Transition from Low to High Level

Q0 = The level of Q before the indicated input conditions were established.

* This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

Functional Diagram



Specifications HCTS74MS

Absolute Maximum Ratings

Supply Voltage (VCC)	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output	±25mA
(All Voltage Reference to the VSS Terminal)	
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W
Power Dissipation per Package (PD)		
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	1W	
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$		Derate Linearly at 13mW/ $^\circ\text{C}$

Operating Conditions

Supply Voltage (VCC)	+4.5V to +5.5V	Input Low Voltage (VIL)	0.0V to 0.8V
Operating Temperature Range (T_A)	-55°C to +125°C	Input High Voltage (VIH)	VCC/2 to VCC
Input Rise and Fall Times at VCC = 4.5V (TR, TF)	100ns/V Max.		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests $VO \geq 4.0\text{V}$ is recognized as a logic "1", and $VO \leq 0.5\text{V}$ is recognized as a logic "0".
3. Force/Measure functions may be interchanged.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CP to Q, \bar{Q}	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
\bar{S} to Q	TPLH	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	24	ns
\bar{S} to \bar{Q}	TPHL	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	38	ns
\bar{R} to Q	TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	40	ns
\bar{R} to \bar{Q}	TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 35		pF
			1	+125°C	Typical 35		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	25	MHz
			1	+125°C	-	16	MHz
Data to CP Set-up Time	TSU	VCC = 4.5V	1	+25°C	11	-	ns
			1	+125°C	12	-	ns
Hold Time	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time \bar{R}, \bar{S} to CP	TREM	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C	6	-	ns
Pulse Width \bar{R}, \bar{S}	TW	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns
Pulse Width CP	TW	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

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TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP. ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	0.4	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, \bar{Q}	TPHL	VCC = 4.5V	+25°C	2	37	2	46	ns
	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
\bar{S} to Q	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
\bar{S} to \bar{Q}	TPHL	VCC = 4.5V	+25°C	2	38	2	48	ns
\bar{R} to Q	TPHL	VCC = 4.5V	+25°C	2	40	2	50	ns
\bar{R} to \bar{Q}	TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	6µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H

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TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS					
5, 6, 8, 9	1, 2, 3, 4, 7, 10, 11, 12, 13			14	
STATIC BURN-IN II TEST CONNECTIONS					
5, 6, 8, 9	7		1, 2, 3, 4, 10, 11, 12, 13, 14		
DYNAMIC BURN-IN TEST CONNECTIONS					
-	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

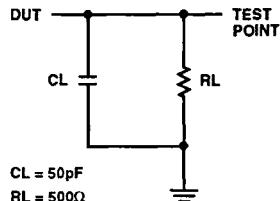
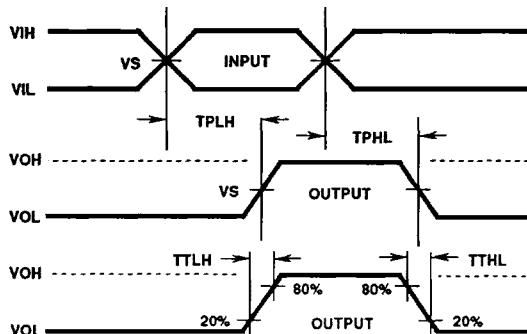
NOTES:

1. Each pin except VCC and GND will have a resistor of $10\text{ k}\Omega \pm 5\%$ for static burn-in.
2. Each pin except VCC and GND will have a resistor of $1\text{ k}\Omega \pm 5\%$ for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

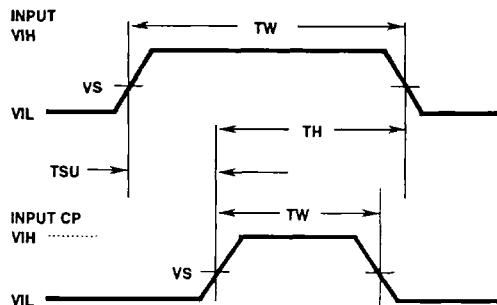
OPEN	GROUND	VCC = 5V ± 0.5V
5, 6, 8, 9	7	1, 2, 3, 4, 10, 11, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of $47\text{ k}\Omega \pm 5\%$ for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger

VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

TH = HOLD TIME
 TSU = SETUP TIME
 TW = PULSE WIDTH

Die Characteristics**DIE DIMENSIONS:**

89 x 88 mils
2.25 x 2.24mm

METALLIZATION:

Type: SiAl
Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2
Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

DIE ATTACH:

Material: Silver Epoxy

WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5 \text{A/cm}^2$

BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$
4 mils x 4 mils

Metalization Mask Layout

HCTS74MS

