

128K x 8 SRAM

MSM8128-45/55

Issue 4.1 : JUNE 1996

Description

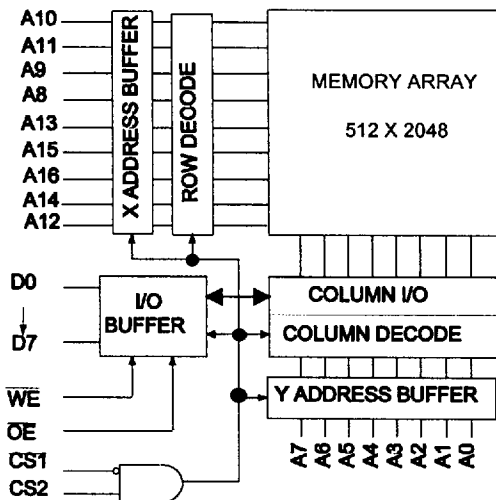
The MSM8128 is a 1Mbit monolithic SRAM organised as 128Kx8 available with access times of 45 / 55 ns. The device is available in three ceramic package options including a high density VIL™ package. It has a low power standby and 3.0V battery backup capability, completely static operation and is directly TTL compatible. May be screened in accordance with MIL-STD-883.

131,072 x 8 CMOS High Speed Static RAM

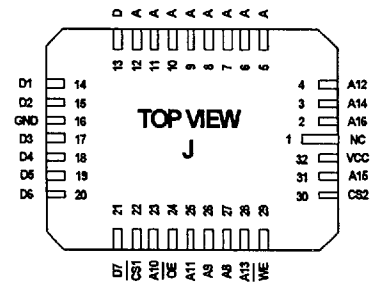
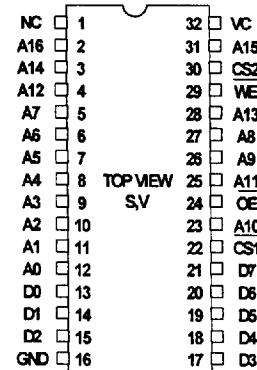
Features

- Very Fast Access Times of 45/55 ns
- Low Power Operation 440 mW (Max.)
- Low Power Standby 11 mW (Max.) - L Version
- Completely Static Operation
- Low Voltage Data Retention
- Directly TTL compatible
- JEDEC Standard 32 pin DIL footprint
- May be processed in accordance with MIL-STD-883C

Block Diagram



Pin Definition



Package Details

Pin Count	Description	Package
32	0.6" Dual-in-Line (DIP)	S
32	0.1" Vertical-in-Line (VIL™)	V
32	J-Leaded Chip Carrier (JLCC)	J

Pin Functions

- A0-A16** Address Inputs
- D0-7** Data Input/Output
- CS1** Chip Select 1
- CS2** Chip Select 2
- OE** Output Enable
- WE** Write Enable
- NC** No Connect
- V_{cc}** Power (+5V)
- GND** Ground

DC OPERATING CONDITIONS**Absolute Maximum Ratings**

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

- Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- (2) V_T can be -3.0V pulse of less than 20ns.

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I suffix)
	T_{AM}	-55	-	125	°C (M, MB suffix)

- Notes : (1) V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IH} = \text{Gnd to } V_{CC}$	-2	-	2	μA
Output Leakage Current	I_{LO}	$\overline{\text{CS1}} = V_{IH}$, $\text{CS2} = V_{IL}$, $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$	-2	-	2	μA
Operating Supply Current	I_{CC}	$\overline{\text{CS1}} = V_{IL}$, $\text{CS2} = V_{IH}$, $I_{OUT} = 0\text{mA}$	-	-	80	mA
Average Supply Current	I_{CC1}	Min. Cycle, duty=100%, $I_{OUT} = 0\text{mA}$	-	-	120	mA
Standby Supply Current	I_{SB}	$\overline{\text{CS1}} = V_{IH}$, $\text{CS2} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} , Min. Cycle	-	-	15	mA
- L Version	I_{SB1}	$\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$, $\text{CS2} \leq 0.2\text{V}$, $0.2\text{V} \geq V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-1	2	mA
Output Voltage	V_{OL}	$I_{OL} = 8.0\text{ mA}$	-	-	0.4	V
	V_{OH}	$I_{OH} = -4.0\text{ mA}$	2.4	-	-	V

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Test Condition	typ	max	Unit
I/P Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	-	7	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	-	7	pF

Note: This parameter is sampled and not 100% tested.

Operating Modes

The table below shows the logic inputs required to control the MSM8128 SRAM.

Mode	$\overline{CS1}$	CS2	\overline{OE}	\overline{WE}	V_{CC} Current	I/O Pin	Reference Cycle
Not Selected	1	X	X	X	I_{SB}, I_{SB1}	High Z	Power Down
Not Selected	X	0	X	X	I_{SB}, I_{SB1}	High Z	Power Down
Output Disable	0	1	1	1	I_{CC}	High Z	
Read	0	1	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	1	X	0	I_{CC}	D_{IN}	Write Cycle

1 = V_{IH}

0 = V_{IL}

X = Don't Care

Low V_{CC} Data Retention Characteristics - L Version Only ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

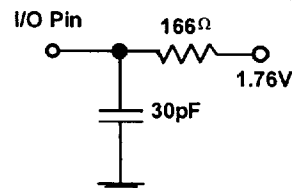
Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC} - 0.2\text{V}$, $CS2 \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq CS2 \leq 0.2\text{V}$, $V_{IN} \geq 0\text{V}$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0\text{V}$, $V_{IN} \geq 0\text{V}$, $\overline{CS1} \geq V_{CC} - 0.2\text{V}$, $CS2 \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq CS2 \leq 0.2\text{V}$.	-	-	750	μA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ns

Notes (1) CS2 controls address buffer, WE buffer, $\overline{CS1}$ buffer and \overline{OE} buffer. If CS2 controls data retention mode, V_{in} levels (\overline{WE} , \overline{OE} , $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls Data Retention mode, CS2 must be $\geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq CS2 \leq 0.2\text{V}$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

AC Test Conditions

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: See Load Diagram
- * $V_{CC} = 5\text{V} \pm 10\%$

Output Load



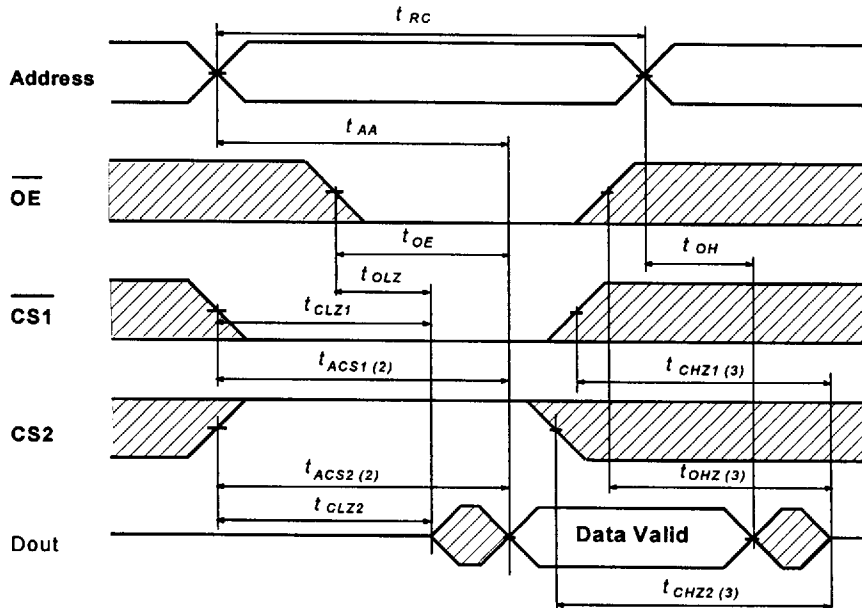
AC OPERATING CONDITIONS

Parameter	Symbol	45		55		Units
		min	max	min	max	
Read Cycle Time	t_{RC}	45	-	55	-	ns
Address Access Time	t_{AA}	-	45	-	55	ns
Chip Selection ($\overline{CS1}$) Access Time	t_{ACS1}	-	45	-	55	ns
Chip Selection (CS2) Access Time	t_{ACS2}	-	45	-	55	ns
Output Enable to Output Valid	t_{OE}	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Chip Selection ($\overline{CS1}$) to O/P in Low Z	t_{CLZ1}	5	-	5	-	ns
Chip Selection (CS2) to O/P in Low Z	t_{CLZ2}	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	ns
Chip Deselect ($\overline{CS1}$) to O/P in high Z ⁽³⁾	t_{CHZ1}	0	20	0	25	ns
Chip Deselect (CS2) to O/P in high Z ⁽³⁾	t_{CHZ2}	0	20	0	25	ns
Output Disable to Output in High Z ⁽³⁾	t_{OHZ}	0	25	-	30	ns

Write Cycle

Parameter	Symbol	45		55		Units
		min	max	min	max	
Write Cycle Time	t_{WC}	45	-	55	-	ns
Chip Selection to End of Write	t_{CW}	40	-	45	-	ns
Address Valid to End of Write	t_{AW}	40	-	45	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	40	-	ns
Write Recovery Time (\overline{WE} , $\overline{CS1}$)	t_{WR1}	3	-	3	-	ns
Write Recovery Time (CS2)	t_{WR2}	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}	0	20	0	25	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	ns

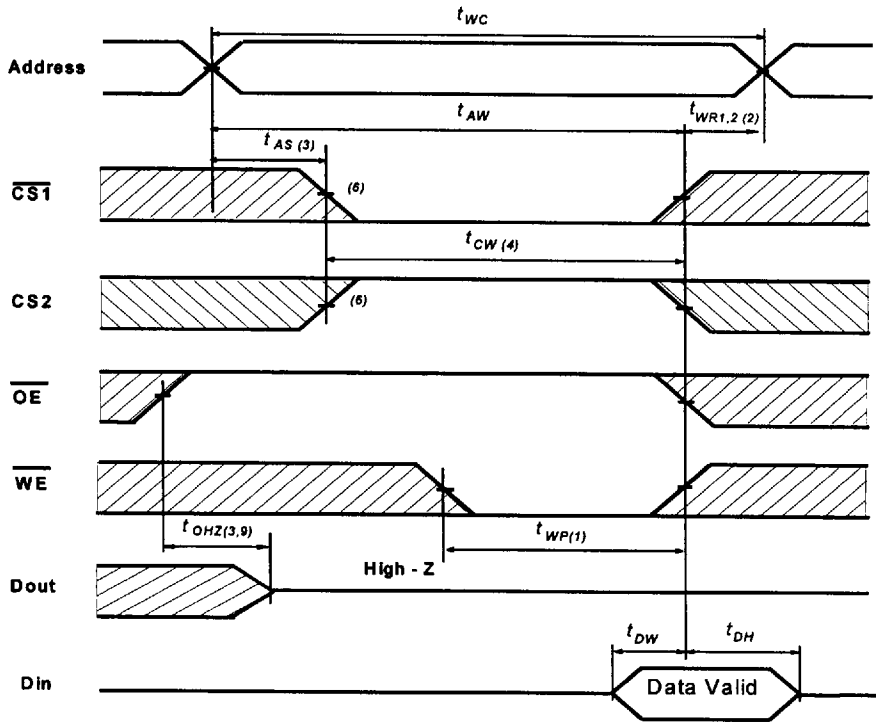
Read Cycle Timing Waveform ^(1,2)



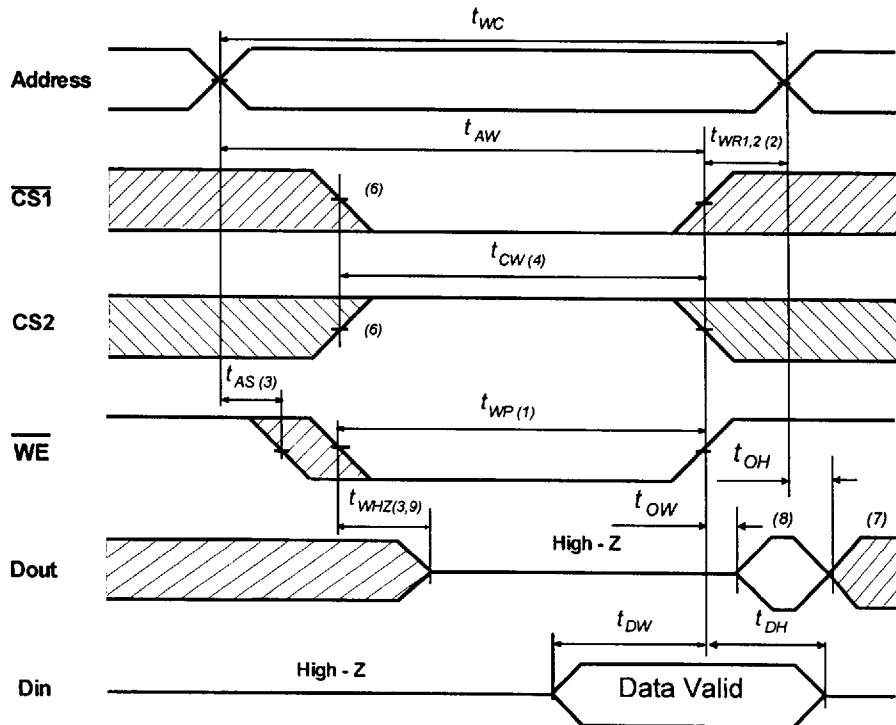
Notes:

- (1) \overline{WE} is High for Read Cycle.
- (2) Address valid prior to or coincident with $\overline{CS1}$ transition low or CS2 high.
- (3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.

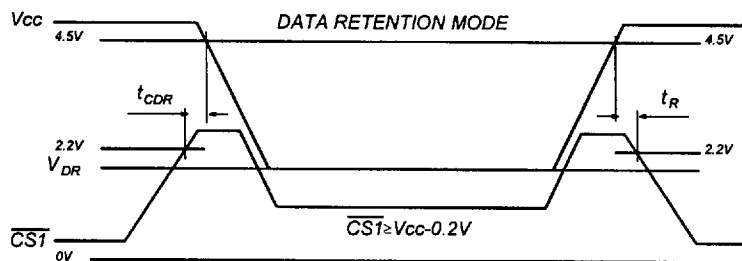
Write Cycle No.1 Timing Waveform



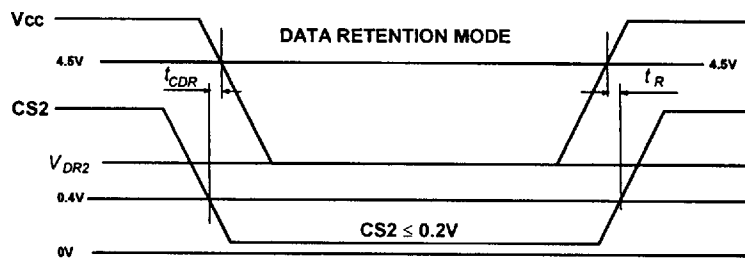
Write Cycle No.2 Timing Waveform ⁽⁵⁾



Low V_{CC} Data Retention Timing Waveform 1 (CS1 controlled)



Low V_{CC} Data Retention Timing Waveform 2 (CS2 controlled)

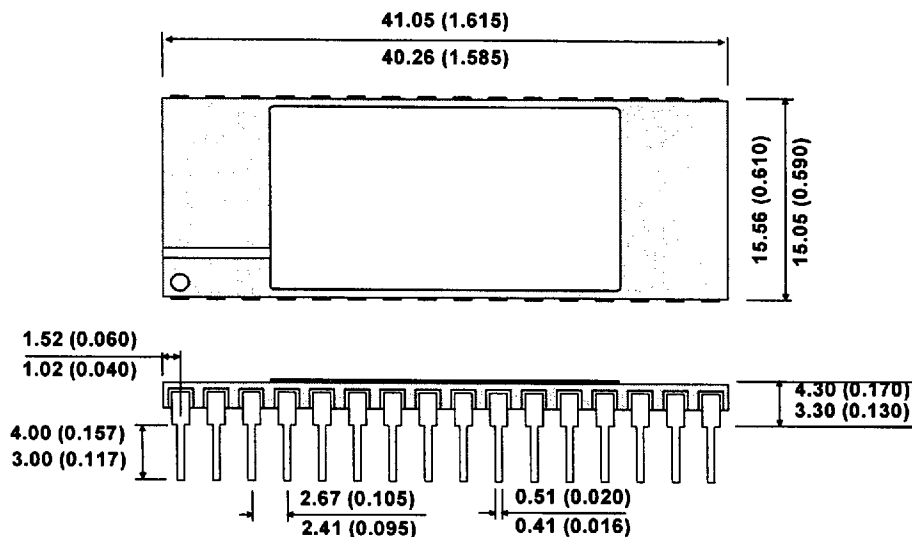


AC Characteristics Notes

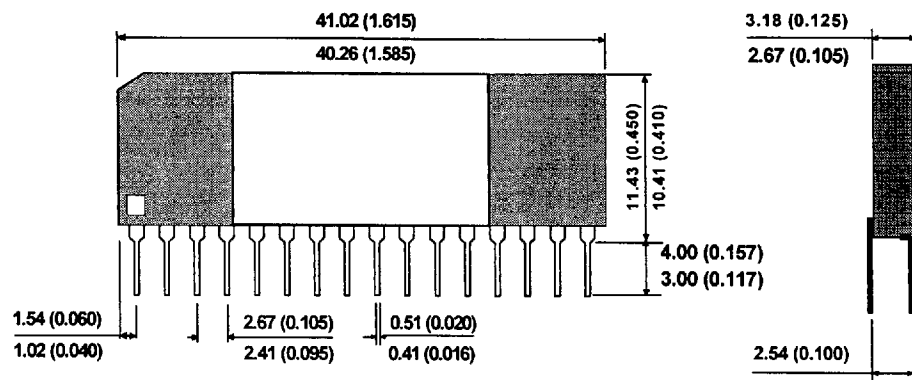
- (1) A write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, $CS2$ going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- (2) t_{WR} is measured from the earlier of $\overline{CS1}$ or \overline{WE} going high or $CS2$ going high to the end of write cycle.
- (3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (4) If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, outputs remain in high impedance state.
- (5) OE is continuously low. ($\overline{OE} = V_{IL}$)
- (6) Dout is in the same phase as written data of this write cycle.
- (7) Dout is the read data of next address.
- (8) If $\overline{CS1}$ is low and $CS2$ is high during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
- (9) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Package Details

32 pin 0.6" Dual-in-Line (DIP) - 'S' Package

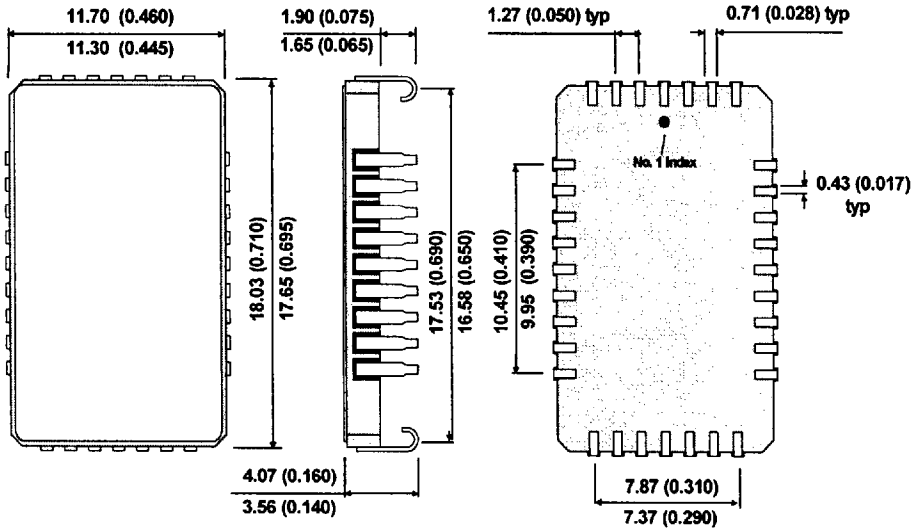


32 pin 0.1" Vertical-in-Line (VIL™) - 'V' Package



All dimensions in mm (inches).

32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'J' Package



SCREENING**Military Screening Procedure**

Component Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB COMPONENT SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at $T_A = +25^\circ\text{C}$	100%
Burn-in	Method 1015, Condition D, $T_A = +125^\circ\text{C}$, 160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100%
Functional	a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100%
Switching (ac)	a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at $T_A = +25^\circ\text{C}$	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM8128SLMB-45

