Advance Information/
Preliminary Data

CA3440A, CA3440

Nanopower BiMOS Op Amp

Features:

- *300-nW (typ.) standby power at $V^+ = 5$ V*
- *Supply current, BW, slew rate programmable using external resistor*
- *10-pA (typ.) input current*
- *5 to 15-V supply*
- *Output drives typical bipolar-type loads*
- *Low-cost 8-lead Mini-DIP, TO-5*

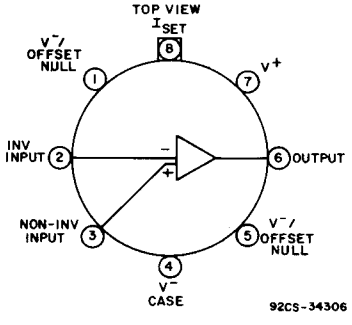
The RCA-CA3440A and CA3440* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440A and CA3440 BiMOS op amps feature gate-protected PMOS transistors in the input circuit to provide very-high-input impedance and very-low-input current (10 pA). These devices operate at total supply voltages from 5 to 15 volts and can be operated over the temperature range from -55°C to +125°C. Their virtues are programmability and very low standby power consumption (300 nW). These operational amplifiers are internally phase-compensated to achieve stable operation in the unity-gain follower configuration. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative-supply terminals, an important attribute for single-supply applications. The output stage uses MOS complementary source-follower form which permits moderate load driving capability (10 KΩ) at very low total standby currents (50 nA).

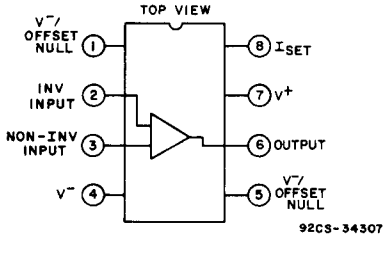
The CA3440A and CA3440 have the same 8-lead terminal pin-out used for "741" and other industry-standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

* Formerly Dev. Type No. TA10590.



S and T Suffixes



E Suffix

Functional diagrams for CA3440A and CA3440.

CA3440A, CA3440

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 25 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±9 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
AT 125°C ..... 418 mW
BELOW 125°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS V^+=+5 V; V^-=-5 V, R_{SET}=10 MΩ; T_A=25°C		CA3440A	CA3440	UNITS
Input Resistance, R_I			2	2	TΩ
Input Capacitance, C_T			3.5	3.5	pF
Ouput Resistance, R_O			450	450	Ω
Equivalent Input Noise Voltage, e_n	f= 1 kHz	R_S=100 Ω	110	110	$nV/\sqrt{Hz}$
	f=10 kHz	R_S=100 Ω	110	110	$nV/\sqrt{Hz}$
Short-Circuit Current Source IOM^+			15	15	mA
To Opposite Supply Sink IOM^-			4.5	4.5	mA
Gain-Bandwidth Product, f_T			63	63	kHz
Slew Rate, SR			0.03	0.03	V/μs
Transient Response Rise Time, t_r	R_L= 10 kΩ		5.6	5.6	μs
Overshoot	C_L=100 pF		10	10	%

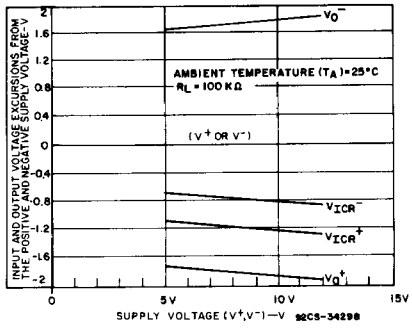


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

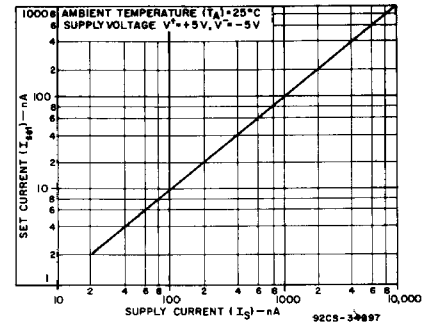


Fig. 2 - Set current versus supply current.

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ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = +5 V, V^- = -5 V, T_A = 25°C Unless Otherwise Specified, R_{SET}=10 MΩ

CHARACTERISTIC	LIMITS						UNITS
	CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current, $\|I_{IO}\|$	—	2.5	20	—	2.5	30	pA
Input Current, $\|I_I\|$	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL	10K	100K	—	10K	100K	—	V/V
(R_L=10 KΩ)	80	100	—	80	100	—	dB
Common-Mode	—	100	320	—	100	320	μV/V
Rejection Ratio, CMRR	70	80	—	70	80	—	dB
Common-Mode Input $VICR^+$	+3.5	+3.7	—	+3.5	+3.7	—	V
Voltage Range, $VICR^-$	−5.0	−5.3	—	−5.0	−5.3	—	V
Power Supply Rejection Ratio, $\Delta VIO/\Delta V$	—	32	320	—	32	320	μV/V
PSRR	70	90	—	70	90	—	dB
Maximum Output Voltage, VOM^+	+3	+3.2	—	+3	+3.2	—	V
VOM^-	−3	−3.2	—	−3	−3.2	—	V
Supply Current, I^+	—	10	17	—	10	17	μA
Device Dissipation, P_D	—	100	170	—	100	170	μW
Input Offset Voltage Temperature Drift, $\Delta VIO/\Delta T$	—	4	—	—	4	—	μV/°C

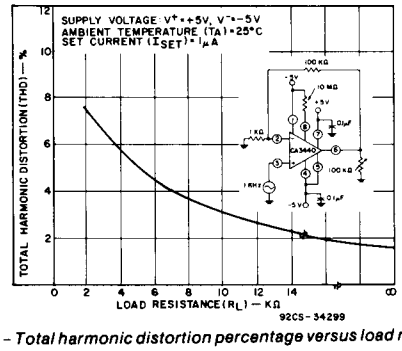

Fig. 3 - Total harmonic distortion percentage versus load resistance.

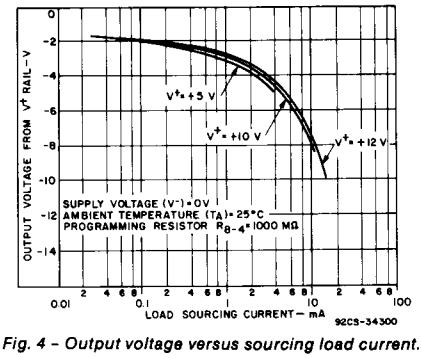

Fig. 4 - Output voltage versus sourcing load current.

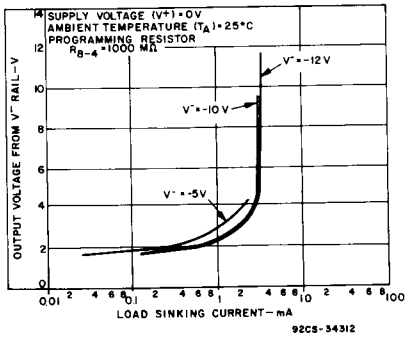

Fig. 5 - Output voltage versus sinking load current.

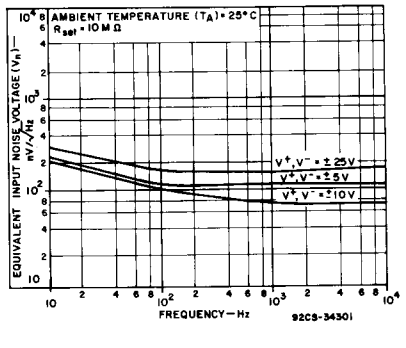

Fig. 6 - Input noise voltage versus frequency.

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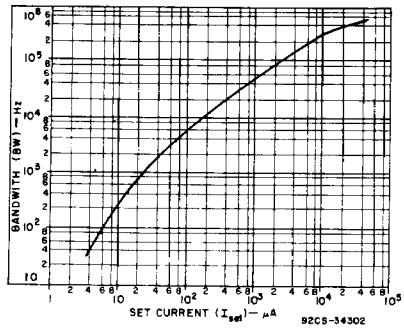

Fig. 7 - Bandwidth versus set current.

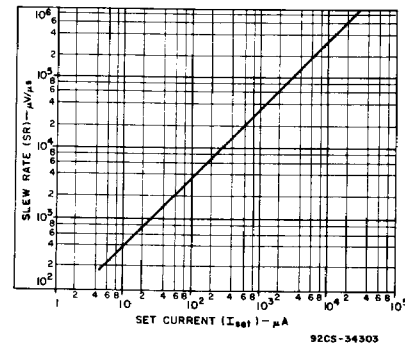

Fig. 8 - Slew rate versus set current.

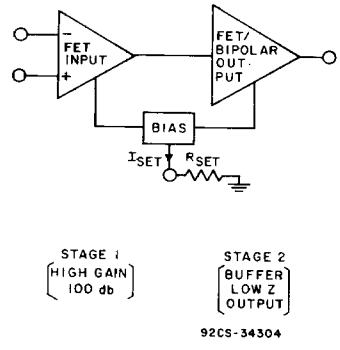

Fig. 9 - Nanopower op amp (supply current programmable using R_{SET}) 1-pA typical input bias current, 4.0 to 15-volt supply.

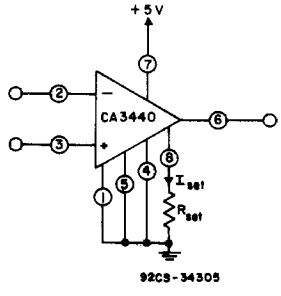

Fig. 10 - Nanopower op amp (usable standby power versus programming resistor R_{SET}).

As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	Standby Power	BW	SR
1 MΩ	250 μW	164 kHz	0.17 V/μs
10 MΩ	25 μW	27 kHz	0.017 V/μs
100 MΩ	2.5 μW	2.6 kHz	.0017 V/μs
1000 MΩ	250 nW	78 Hz	0.00017 V/μs

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or −V via R_{SET}.

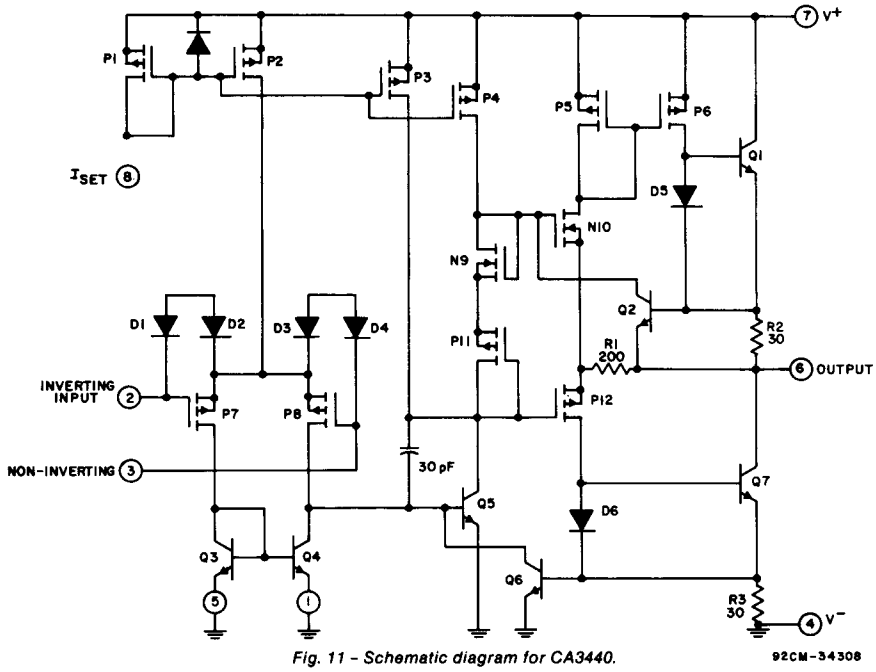

Fig. 11 - Schematic diagram for CA3440.

APPLICATIONS CIRCUITS

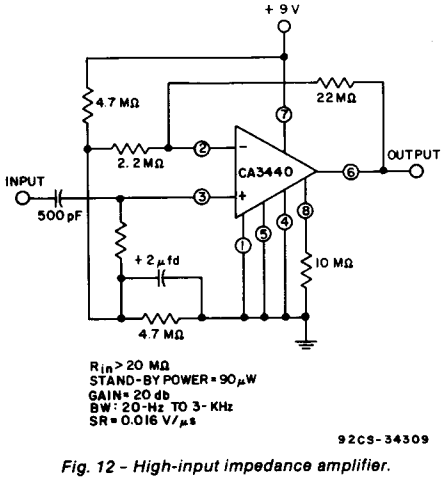

Fig. 12 - High-input impedance amplifier.

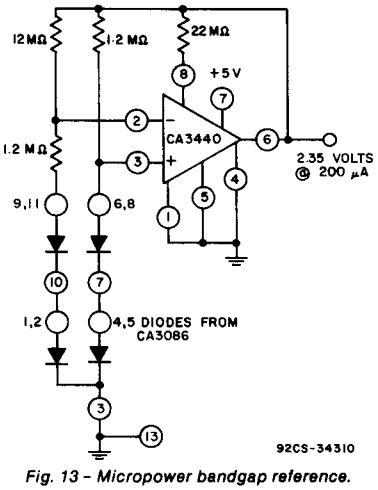

Fig. 13 - Micropower bandgap reference.

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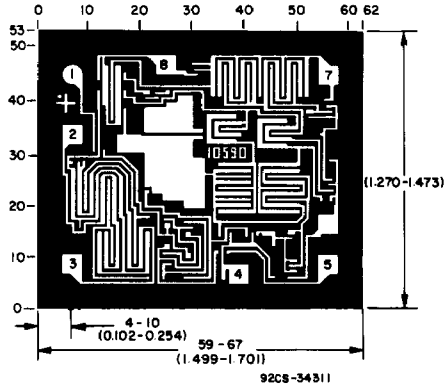

Dimensions and pad layout for CA3440H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.