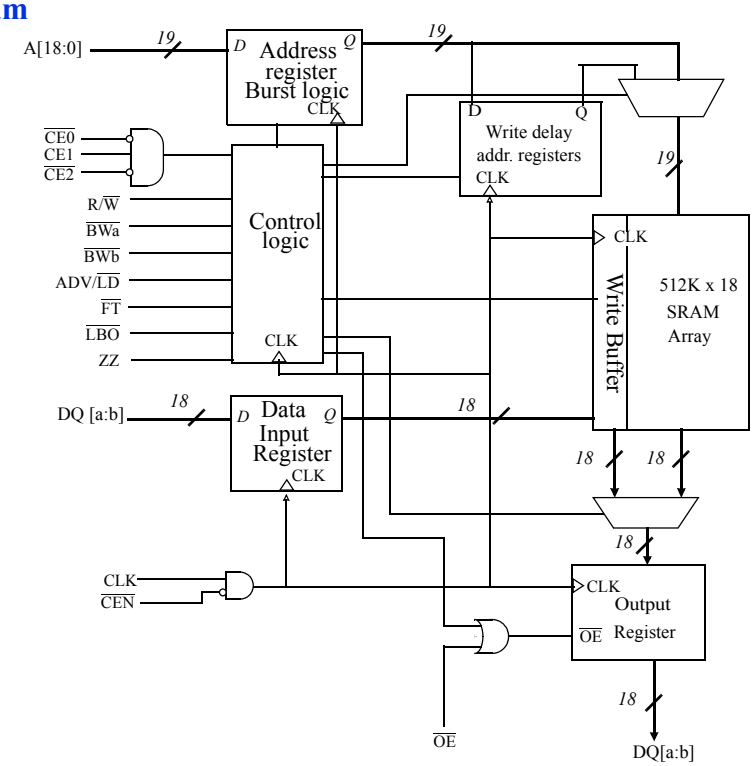
3.3V 512K × 18 SRAM with NTD™

Features

- Organization: 524,288 words × 18 bits
- NTD™[1] architecture for efficient bus operation
- Fast clock speeds to 166 MHz in LVTTL/LVCMOS
- Fast clock to data access: 3.0/3.5/3.8/4.0/5.0 ns
- Fast $\overline{OE}$ access time: 3.5/3.8/4.0/5.0 ns
- Fully synchronous register-to-register operation
- "Flow-through" or "Pipeline" modes
- Asynchronous output enable control
- Available in100-pin TQFP
- Byte write enables
- Multiple chip enables for easy expansion
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- 30 mW typical standby power in power down mode
- Self-timed WRITE cycles
- "Interleaved" or "Linear burst" modes
- Snooze mode for standby operation

1. NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners

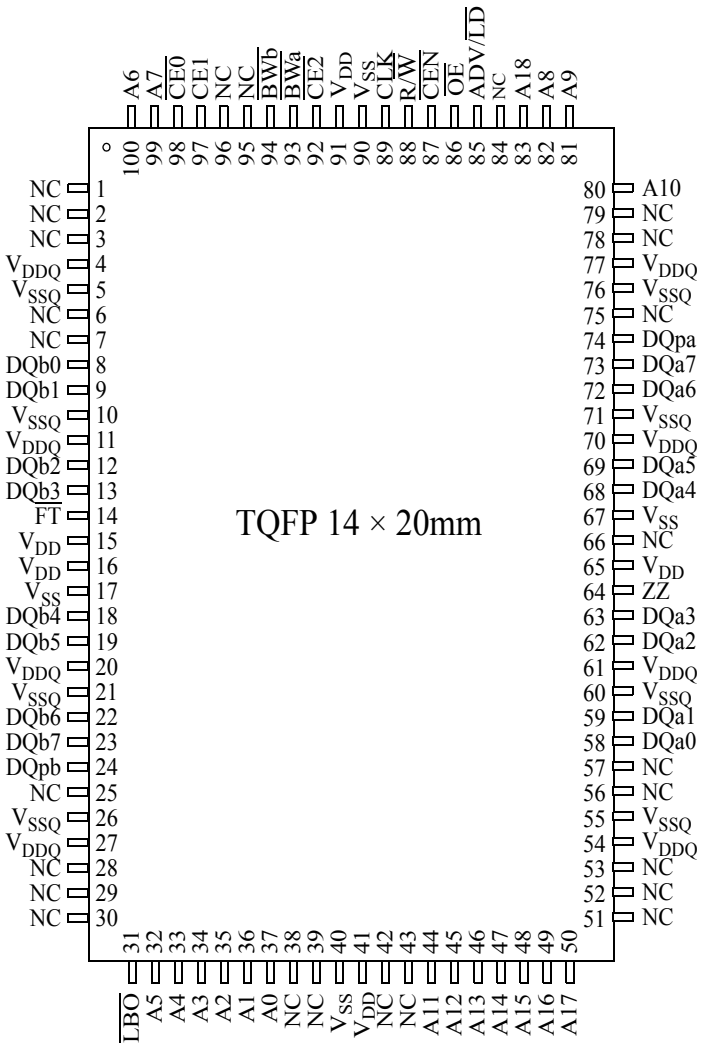
Logic block diagram



Selection Guide

	-166	–150	–133	–100	Units
Minimum cycle time	6	6.6	7.5	10	ns
Maximum pipelined clock frequency	166	150	133	100	MHz
Maximum pipelined clock access time	3.5	3.8	4	5	ns
Maximum operating current	475	425	400	300	mA
Maximum standby current	130	110	100	90	mA
Maximum CMOS standby current (DC)	30	30	30	30	mA

Pin arrangement for TQFP



Functional description

The AS7C33512NTD18A family is a high performance CMOS 8 Mbit synchronous Static Random Access Memory (SRAM) organized as 524,288 words × 18 bits and incorporates a LATE LATE Write.

This variation of the 8Mb sychronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipeline burst devices. In a normal pipeline burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write command, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write 'latency' which matches the two cycle pipeline and one cycle flowthrough read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

Assert R/$\overline{W}$ LOW to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied LOW for full 18 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable $\overline{OE}$ does not need to be toggled for write operations; it can be tied LOW for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs (refer to synchronous truth table on page 4.) In pipeline mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read, write and deselect operations. When ADV is HIGH, external addresses, chip select, R/$\overline{W}$ pins are ignored, and internal address counters increment in the count sequence specified by the $\overline{LBO}$ control. Any device operations, including burst, can be stalled using the $\overline{CEN}$=1, the clock enable input.

The AS7C33512NTD18A operate with a 3.3V ± 5% power supply for the device core (V_{DD}). DQ circuits use a separate power supply (V_{DDQ}) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin 14×20 mm TQFP.

Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{IN} = V_{OUT} = 0V	7	pF

TQFP thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient)[1]	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1–layer	θ_{JA}	40	°C/W
		4–layer	θ_{JA}	22	°C/W
Thermal resistance (junction to top of case)[1]			θ_{JC}	8	°C/W

1 This parameter is sampled

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$, $\overline{FT}$, $\overline{LBO}$, and ZZ are synchronous to this clock.
$\overline{CEN}$	I	SYNC	Clock enable. When de-asserted HIGH, the clock input signal is masked.
A, A0, A1	I	SYNC	Address. Sampled when all chip enables are active and ADV/$\overline{LD}$ is asserted.
DQ[a,b]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$, CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Sampled at the rising edge of CLK, when ADV/$\overline{LD}$ is asserted. Are ignored when ADV/$\overline{LD}$ is HIGH.
ADV/$\overline{LD}$	I	SYNC	Advance or Load. When sampled HIGH, the internal burst address counter will increment in the order defined by the $\overline{LBO}$ input value. (refer to table on page 2) When LOW, a new address is loaded.
R/$\overline{W}$	I	SYNC	A HIGH during LOAD initiates a READ operation. A LOW during LOAD initiates a WRITE operation. Is ignored when ADV/$\overline{LD}$ is HIGH.
$\overline{BW[a,b]}$	I	SYNC	Byte write enables. Used to control write on individual bytes. Sampled along with WRITE command and BURST WRITE.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are not driven when $\overline{OE}$ is inactive.
$\overline{LBO}$	I	STATIC	Selects Burst mode. When tied to V_{DD} or left floating, device follows Interleaved Burst order. When driven Low, device follows linear Burst order. *This signal is internally pulled High.*
$\overline{FT}$	I	STATIC	Selects Pipeline or Flow-through mode.When tied to V_{DD} or left floating, enables Pipeline mode. When driven Low, enables single register flow-through mode. *This signal is internally pulled High.*
ZZ	I	ASYNC	Snooze. Places device in low power mode; data is retained. Connect to VSS if unused.
NC	-	-	No connects. Note that pin 84 will be used for future address expansion to 18Mb density.

Burst Order

Interleaved burst order $\overline{LBO}$ = 1					Linear burst order $\overline{LBO}$ = 0				
	A1 A0	A1 A0	A1 A0	A1 A0		A1 A0	A1 A0	A1 A0	A1 A0
Starting address	0 0	0 1	1 0	1 1	Starting Address	0 0	0 1	1 0	1 1
First increment	0 1	0 0	1 1	1 0	First increment	0 1	1 0	1 1	0 0
Second increment	1 0	1 1	0 0	0 1	Second increment	1 0	1 1	0 0	0 1
Third increment	1 1	1 0	0 1	0 0	Third increment	1 1	0 0	0 1	1 0

Synchronous truth table[5,6,7,8,9]

$\overline{CE0}$	CE1	$\overline{CE2}$	ADV/$\overline{LD}$	R/$\overline{W}$	$\overline{BWn}$	$\overline{OE}$	$\overline{CEN}$	Address source	CLK	Operation	DQ	Notes
H	X	X	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	X	H	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	L	X	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	X	X	H	X	X	X	L	NA	L to H	CONTINUE DESELECT Cycle	High-Z	1
L	H	L	L	H	X	L	L	External	L to H	READ Cycle (Begin Burst)	Q	
X	X	X	H	X	X	L	L	Next	L to H	READ Cycle (Continue Burst)	Q	1,10
L	H	L	L	H	X	H	L	External	L to H	NOP/DUMMY READ (Begin Burst)	High-Z	2
X	X	X	H	X	X	H	L	Next	L to H	DUMMY READ (Continue Burst)	High-Z	1,2,10
L	H	L	L	L	L	X	L	External	L to H	WRITE CYCLE (Begin Burst)	D	3
X	X	X	H	X	L	X	L	Next	L to H	WRITE CYCLE (Continue Burst)	D	1,3,10
L	H	L	L	L	H	X	L	External	L to H	NOP/WRITE ABORT (Begin Burst)	High-Z	2,3
X	X	X	H	X	H	X	L	Next	L to H	WRITE ABORT (Continue Burst)	High-Z	1,2,3, 10
X	X	X	X	X	X	X	H	Current	L to H	INHIBIT CLOCK	-	4

Key: X = Don't Care, H = HIGH, L = LOW. $\overline{BW}$n = H means all byte write signals ($\overline{BW}$a and $\overline{BW}$b) are HIGH. $\overline{BW}$n = L means one or more byte write signals are LOW.

Notes:

1 CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONINUE DESELECT cycle can only be entered if a DESELECT CYCLE is executed first.

2 DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.

3 $\overline{OE}$ may be wired LOW to minimize the number of control signal to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. $\overline{OE}$ may be used when the bus turn-on and turn-off times do not meet an application's requirements.

4 If an INHIBIT CLOCK command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the INHIBIT CLOCK cycle.

5 $\overline{BW}$a enables WRITEs to byte "a" (DQa pins/balls); $\overline{BW}$b enables WRITEs to byte "b" (DQb pins/balls).

6 All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

7 Wait states are inserted by setting $\overline{CEN}$ HIGH.

8 This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.

9 The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST CYCLE.

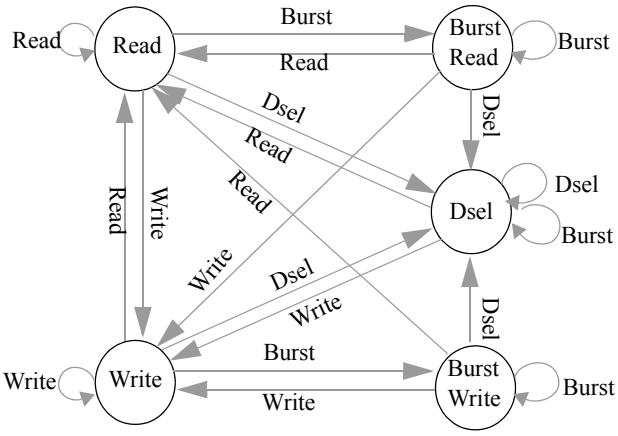
10 The address counter is incremented for all CONTINUE BURST cycles.

Absolute maximum ratings[1]

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	V_{DD} + 0.5	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_D	–	1.8	W
DC output current	I_{OUT}	–	50	mA
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature under bias	T_{bias}	–65	+135	°C

1 Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

State Diagram for NTD SRAM



Recommended operating conditions at 3.3V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	3.135	3.3	3.465	V
Ground supply	Vss	0	0	0	V

Recommended operating conditions at 2.5V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	2.375	2.5	2.625	V
Ground supply	Vss	0	0	0	V

DC electrical characteristics for 3.3V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current[1]	$\|I_{LI}\|$	V_{DD} = Max, OV ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, OV ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	2	V_{DD}+0.3	V
		I/O pins	2	V_{DDQ}+0.3	
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3*	0.8	V
		I/O pins	-0.5*	0.8	
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135V	2.4	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.465V	–	0.4	V

1 $\overline{FT}$, $\overline{LBO}$, and ZZ pins have an internal pull-up or pull-down, and input leakage = ±10 µA.

DC electrical characteristics for 2.5V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{DD} = Max, OV ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, OV ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	1.7	V_{DD}+0.3	V
		I/O pins	1.7	V_{DDQ}+0.3	V
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3*	0.7	V
		I/O pins	-0.3*	0.7	V
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375V	1.7	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 2.625V	–	0.7	V

*V_{IL} min = -1.5 for pulse width less than 0.2 X t_{CYC}

I_{DD} operating conditions and maximum limits

Parameter	Sym	Test conditions	-166	-150	-133	-100	Unit
Operating power supply current[1] (pipelined mode)	I_{CC}	$\overline{CE}_0$ = V_{IL}, CE_1 = V_{IH}, $\overline{CE}_2$ = V_{IL}, $f = f_{max}$, I_{out} = 0 mA	475	425	400	300	mA
Operating power supply current[2](flow-through mode)	I_{CC} (FT)		325	325	300	275	mA
Standby power supply current	I_{SB}	Deselected, $f = f_{max}$, ZZ ≤ V_{IL}	130	110	100	90	mA
	I_{SB1}	Deselected, f = 0, ZZ ≤ 0.2V all V_{IN} ≤ 0.2V or ≥ V_{DD} - 0.2V	30	30	30	30	
	I_{SB2}	Deselected, f = f_{Max}, ZZ ≥ V_{DD} - 0.2V, all V_{IN} ≤ V_{IL} or ≥ V_{IH}	30	30	30	30	

1 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.

Timing characteristics over operating range for 3.3V I/O

Parameter	Symbol	–166		–150		–133		–100		Unit	Notes[1]
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock frequency	f_{Max}	–	166	–	150	–	133	–	100	MHz	
Cycle time (pipelined mode)	t_{CYC}	6	–	6.6	–	7.5	–	10	–	ns	
Cycle time (flow-through mode)	t_{CYCF}	10	–	10	–	12	–	12	–	ns	
Clock access time (pipelined mode)	t_{CD}	–	3.5	–	3.8	–	4.0	–	5.0	ns	
Clock access time (flow-through mode)	t_{CDF}	–	9	–	10	–	10	–	12	ns	
Output enable LOW to data valid	t_{OE}	–	3.5	–	3.8	–	4.0	–	5.0	ns	
Clock HIGH to output Low Z	t_{LZC}	0	–	0	–	0	–	0	–	ns	2,3,4
Data output invalid from clock HIGH (Pipelined mode)	t_{OH}	1.5	–	1.5	–	1.5	–	1.5	–	ns	2
Data output invalid from clock HIGH (Flow-through mode)	t_{OHF}	3.0	–	3.0	–	3.0	–	3.0	–	ns	2
Output enable LOW to output Low Z	t_{LZOE}	0	–	0	–	0	–	0	–	ns	2,3,4
Output enable HIGH to output High Z	t_{HZOE}	–	3.5	–	3.8	–	4.0	–	4.5	ns	2,3,4
Clock HIGH to output High Z	t_{HZC}	–	3.5	–	3.8	–	4.0	–	5.0	ns	2,3,4
Output enable HIGH to invalid output	t_{OHOE}	0	–	0	–	0	–	0	–	ns	
Clock HIGH pulse width	t_{CH}	2.4	–	2.5	–	2.5	–	3.5	–	ns	5
Clock LOW pulse width	t_{CL}	2.4	–	2.5	–	2.5	–	3.5	–	ns	5
Address setup to clock HIGH	t_{AS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
Data setup to clock HIGH	t_{DS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
Write setup to clock HIGH	t_{WS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6,7
Chip select setup to clock HIGH	t_{CSS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6,8
Address hold from clock HIGH	t_{AH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
Data hold from clock HIGH	t_{DH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
Write hold from clock HIGH	t_{WH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6,7
Chip select hold from clock HIGH	t_{CSH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6,8
Clock enable setup to clock HIGH	t_{CENS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
Clock enable hold from clock HIGH	t_{CENH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
ADV/$\overline{LD}$ setup to clock HIGH	t_{ADVS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
ADV/$\overline{LD}$ hold from clock HIGH	t_{ADVH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6

1 Refer to “notes” on page 12.

Timing characteristics over operating range for 2.5 V I/O

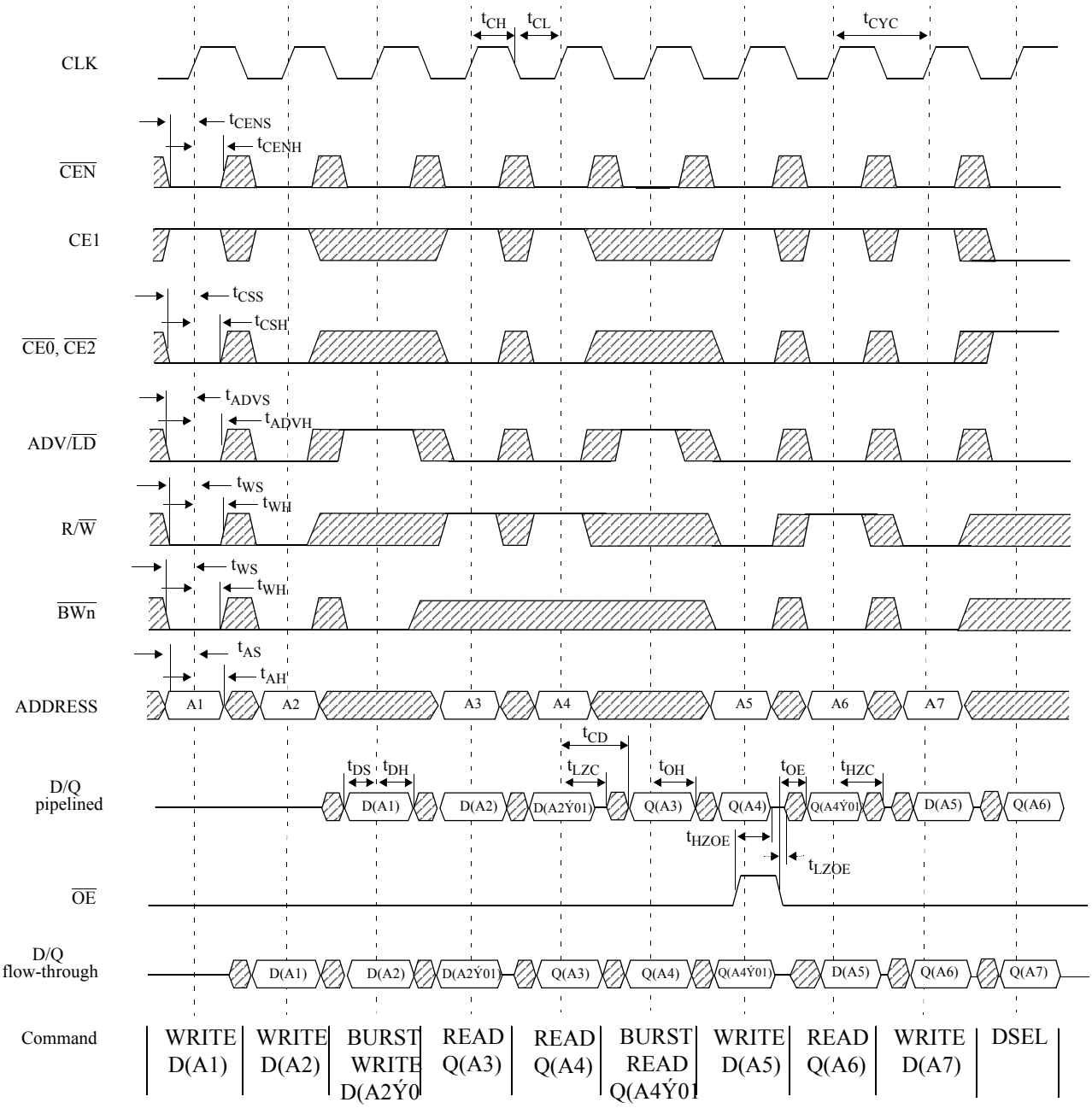
Parameter	Symbol	–166		–150		–133		–100		Unit	Notes[1]
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock frequency	f_{Max}	–	166	–	150	–	133	–	100	MHz	
Cycle time (pipelined mode)	t_{CYC}	6	–	6.6	–	7.5	–	10	–	ns	
Cycle time (flow-through mode)	t_{CYCF}	10	–	10	–	12	–	12	–	ns	
Clock access time (pipelined mode)	t_{CD}	–	4.0	–	4.3	–	4.5	–	5.0	ns	
Clock access time (flow-through mode)	t_{CDF}	–	9	–	10	–	10	–	12	ns	
Output enable low to data valid	t_{OE}	–	3.5	–	3.8	–	4.0	–	5.0	ns	
Clock high to output low Z	t_{LZC}	0	–	0	–	0	–	0	–	ns	2,3,4
Data output invalid from clock high (Pipelined Mode)	t_{OH}	1.5	–	1.5	–	1.5	–	1.5	–	ns	2
Data Output invalid from clock high (Flow-through Mode)	t_{OHF}	3.0	–	3.0	–	3.0	–	3.0		ns	2
Output enable low to output low Z	t_{LZOE}	0	–	0	–	0	–	0	–	ns	2,3,4
Output enable high to output High Z	t_{HZOE}	–	3.5	–	3.8	–	4.0	–	4.5	ns	2,3,4
Clock high to output High Z	t_{HZC}	–	3.5	–	3.8	–	4.0	–	5.0	ns	2,3,4
Output enable high to invalid output	t_{OHOE}	0	–	0	–	0	–	0	–	ns	
Clock high pulse width	t_{CH}	2.4	–	2.5	–	2.5	–	3.5	–	ns	5
Clock low pulse width	t_{CL}	2.3	–	2.5	–	2.5	–	3.5	–	ns	5
Address setup to clock high	t_{AS}	1.7	–	1.7	–	1.7	–	2.0	–	ns	6
Data setup to clock high	t_{DS}	1.7	–	1.7	–	1.7	–	2.0	–	ns	6
Write setup to clock high	t_{WS}	1.7	–	1.7	–	1.7	–	2.0	–	ns	6,7
Chip select setup to clock high	t_{CSS}	1.7	–	1.7	–	1.7	–	2.0	–	ns	6,8
Address hold from clock high	t_{AH}	0.7	–	0.7	–	0.7	–	0.7	–	ns	6
Data hold from clock high	t_{DH}	0.7	–	0.7	–	0.7	–	0.7	–	ns	6
Write hold from clock high	t_{WH}	0.7	–	0.7	–	0.7	–	0.7	–	ns	6,7
Chip select hold from clock high	t_{CSH}	0.7	–	0.7	–	0.7	–	0.7	–	ns	6,8
Clock enable setup to clock high	t_{CENS}	1.7	–	1.7	–	1.7	–	2.0	–	ns	6
Clock enable hold from clock high	t_{CENH}	0.7	–	0.7	–	0.7	–	0.7	–	ns	6
ADV/$\overline{LD}$ setup to clock high	t_{ADVS}	1.7	–	1.7	–	1.7	–	2.0	–	ns	6
ADV/$\overline{LD}$ hold from clock high	t_{ADVH}	0.7	–	0.7	–	0.7	–	0.7	–	ns	6

1 Refer to “notes” onpage 12.

Key to switching waveforms

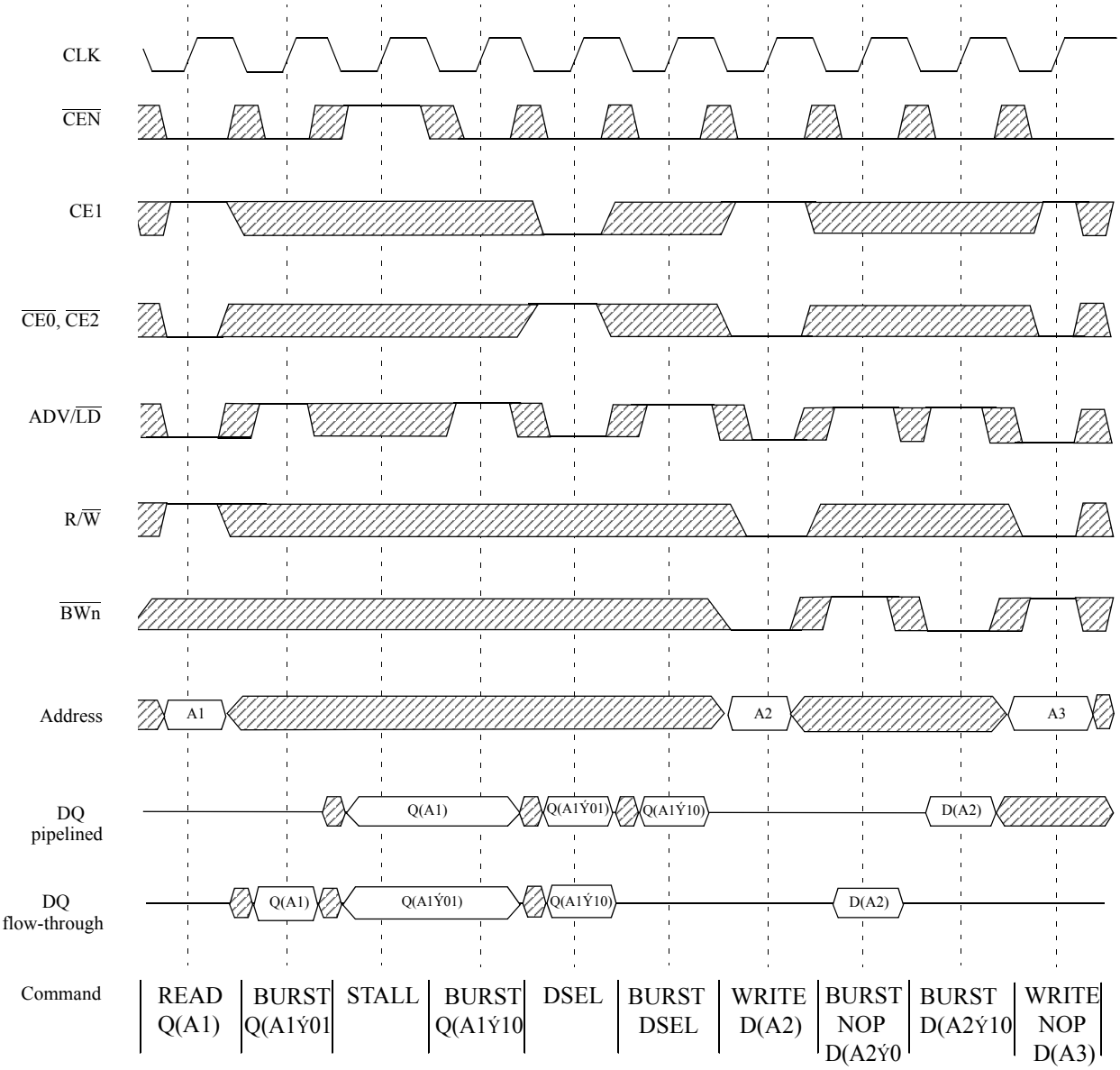
Rising input Falling input Undefined/don't care

Timing waveform of read/write cycle



Note: Ý = XOR when $\overline{LBO}$ = HIGH/No Connect; Ý = ADD when $\overline{LBO}$ = LOW.
$\overline{BW[a:b]}$ is don't care.

NOP, stall and deselect cycles



Note: Ý = XOR when $\overline{LBO}$ = HIGH/No Connect; Ý = ADD when $\overline{LBO}$ = LOW.

AC test conditions

- Output load: see Figure B, except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC}, see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

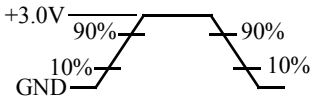


Figure A: Input waveform

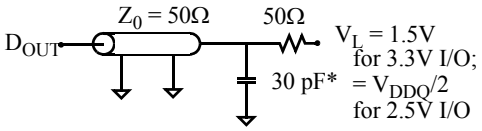


Figure B: Output load (A)

Thevenin equivalent:

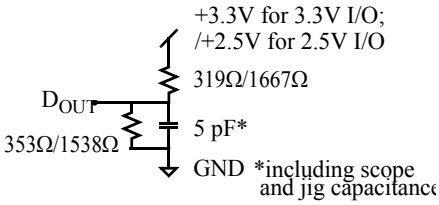
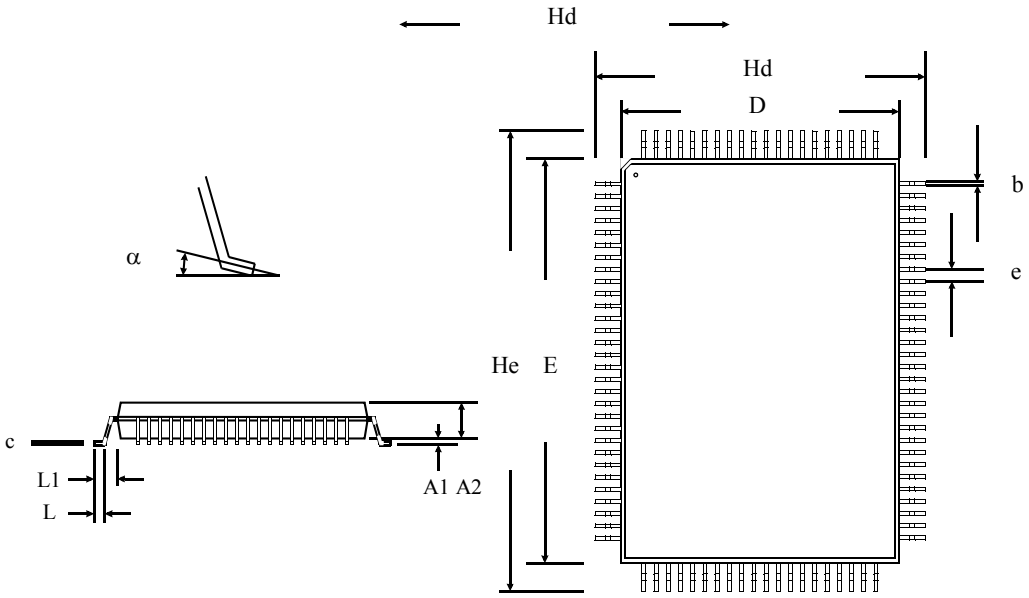


Figure C: Output load(B)

Notes:
1) For test conditions, see “AC Test Conditions”, Figures A, B, C
2) This paracmeter measured with output load conditon in Figure C.
3) This parameter is sampled, but not 100% tested.
4) t_{HZOE} is less than t_{LZOE} and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
5) t_{CH} measured HIGH above V_{IH} and t_{CL} measured as LOW below V_{IL}
6) This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs m meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
7) Write refers to R/$\overline{W}$, $\overline{BW[a:b]}$.
8) Chip select refers to $\overline{CE0}$, CE1, $\overline{CE2}$.

Package Dimensions :100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.90	16.10
He	21.90	22.10
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°
Dimensions in millimeters		



Ordering information

Package & Width	–166	–150	–133	–100
TQFP x18	AS7C33512NTD18A-166TQC	AS7C33512NTD18A-150TQC	AS7C33512NTD18A-133TQC	AS7C33512NTD18A-100TQC
TQFP x18	AS7C33512NTD18A-166TQI	AS7C33512NTD18A-150TQI	AS7C33512NTD18A-133TQI	AS7C33512NTD18A-100TQI

Notes: Add suffix 'N' to the above part numbers for Lead Free Parts (Ex. AS7C33512NTD18A-166TQCN)

Part numbering guide

AS7C	33	512	NTD	18	A	–XXX	TQ	C/I	X
1	2	3	4	5	6	7	8	9	10

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 33=3.3V
3. Organization: 512=512K
4. NTD™ = No-Turn Around Delay. Pipeline-Flowthrough (each device works in both modes)
5. Organization: 18=x18
6. Production version: A=first production version
7. Clock speed (MHz)
8. Package type: TQ=TQFP
9. Operating temperature: C=Commercial (0° C to 70° C); I=Industrial (-40° C to 85° C)
10. N = Lead free part

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Part Number: AS7C33512NTD18A
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