CY7C130/CY7C131
CY7C140/CY7C141

1K x 8 Dual-Port Static RAM

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **1K x 8 organization**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 15 ns**
- **Low operating power: I_{CC} = 110 mA (max.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141**
- **$\overline{BUSY}$ output flag on CY7C130/CY7C131; $\overline{BUSY}$ input on CY7C140/CY7C141**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 48-pin DIP (CY7C130/140), 52-pin PLCC and 52-pin TQFP**
- ***Pin-compatible and functionally equivalent to* IDT7130/IDT7140**

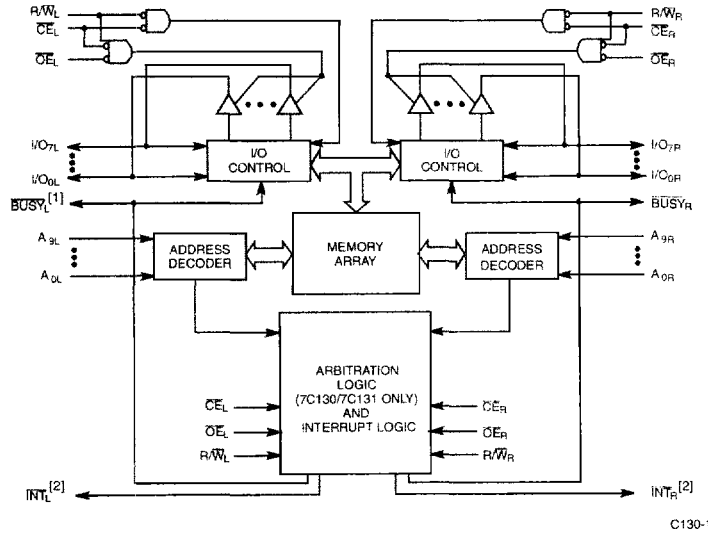
Functional Description

The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/ CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM *in conjunction with the CY7C140/CY7C141 slave* dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 and CY7C140 are available in 48-pin DIP. The CY7C131 and CY7C141 are available in 52-pin PLCC and PQFP.

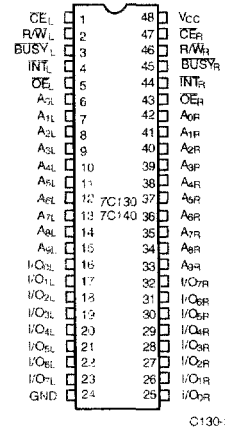
Logic Block Diagram



C130-1

Pin Configurations

DIP
Top View



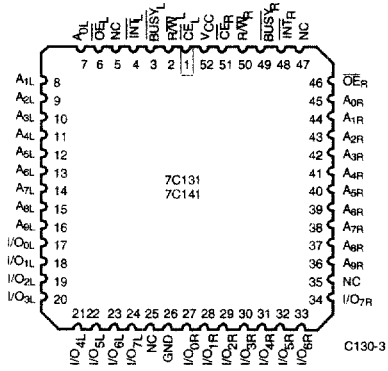
C130-2

Notes:

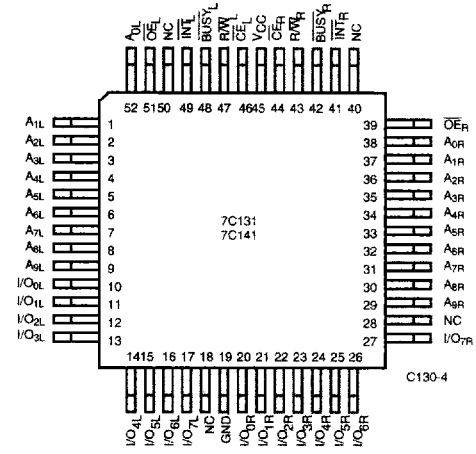
1. CY7C130/CY7C131 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor
   CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs: pull-up resistor required.

Pin Configurations (continued)

PLCC
Top View



PQFP
Top View



Selection Guide

		7C131-15[3] 7C141-15	7C131-25[3] 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		15	25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	190	170	170	120	120	110
	Military				170	170	120
Maximum Standby Current (mA)	Com'l/Ind	75	65	65	45	45	35
	Military				65	65	45

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Military[4]	–55°C to +125°C	5V ± 10%

Notes:

3. 15 and 25-ns version available only in PLCC/PQFP packages.
4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C131-15[3] 7C141-15 Min.	7C131-15[3] 7C141-15 Max.	7C130-30[3] 7C131-25,30 7C140-30 7C141-25,30 Min.	7C130-30[3] 7C131-25,30 7C140-30 7C141-25,30 Max.	7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45 Min.	7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45 Max.	7C130-55 7C131-55 7C140-55 7C141-55 Min.	7C130-55 7C131-55 7C140-55 7C141-55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[7, 8]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[9]	Com'l		190		170		120		110	mA
			Mil						170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[9]	Com'l		75		65		45		35	mA
			Mil						65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		135		115		90		75	mA
			Mil						115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15		15	mA
			Mil						15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		125		105		85		70	mA
			Mil						105		85	

Shaded area contains preliminary information.

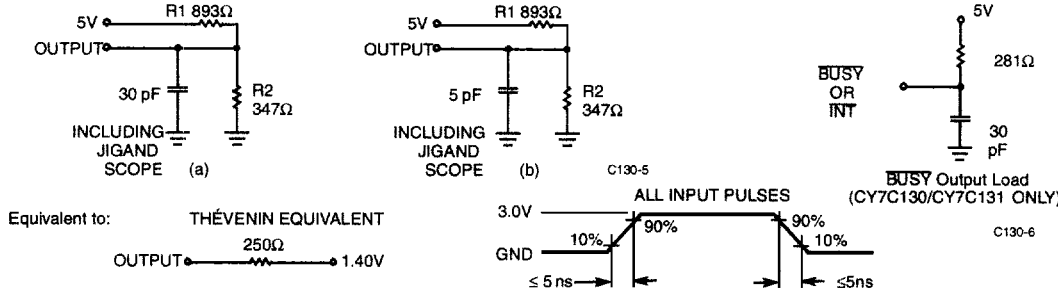
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. BUSY and INT pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. This parameter is guaranteed but not tested.
9. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[5,10]

Parameter	Description	7C131-15[3] 7C141-15		7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		30		ns
t_{AA}	Address to Data Valid[11]		15		25		30	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		15		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8,12, 13]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8,12, 13]		10		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8,12, 13]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,12, 13]		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up[8]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down[8]		15		25		25	ns
WRITE CYCLE[14]								
t_{WC}	Write Cycle Time	15		25		30		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		25		ns
t_{AW}	Address Set-Up to Write End	12		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	12		15		25		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[13]		10		15		15	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[13]	0		0		0		ns

Shaded area contains preliminary information.

Notes:

10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[5,10] (continued)

Parameter	Description	7C131-15[3] 7C141-15		7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		15		20		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		15		20		20	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		15		25		30	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		15		25		25	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		15		25		25	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		15		25		25	ns

Shaded area contains preliminary information.

Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C140/CY7C141 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    $\overline{BUSY}$ on Port B goes HIGH.
    Port B's address is toggled.
    $\overline{CE}$ for Port B is toggled.
    R/$\overline{W}$ for Port B is toggled during valid read.

Switching Characteristics Over the Operating Range[5,10]

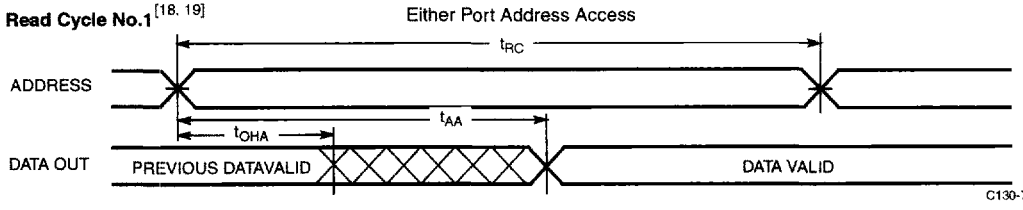
Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid[11]		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8,12,13]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8,12,13]		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8,12,13]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,12,13]		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up[8]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down[8]		35		35		35	ns

Switching Characteristics Over the Operating Range[5,10] (continued)

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE[14]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	30		35		40		ns
t_{AW}	Address Set-Up to Write End	30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[13]		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[13]	0		0		0		ns
BUSY/INTERRUPT TIMING								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		35		45	ns

Switching Waveforms

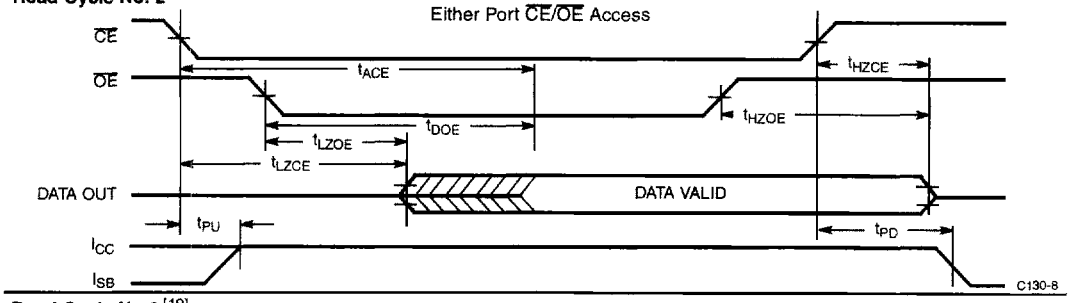
Read Cycle No.1[18, 19]



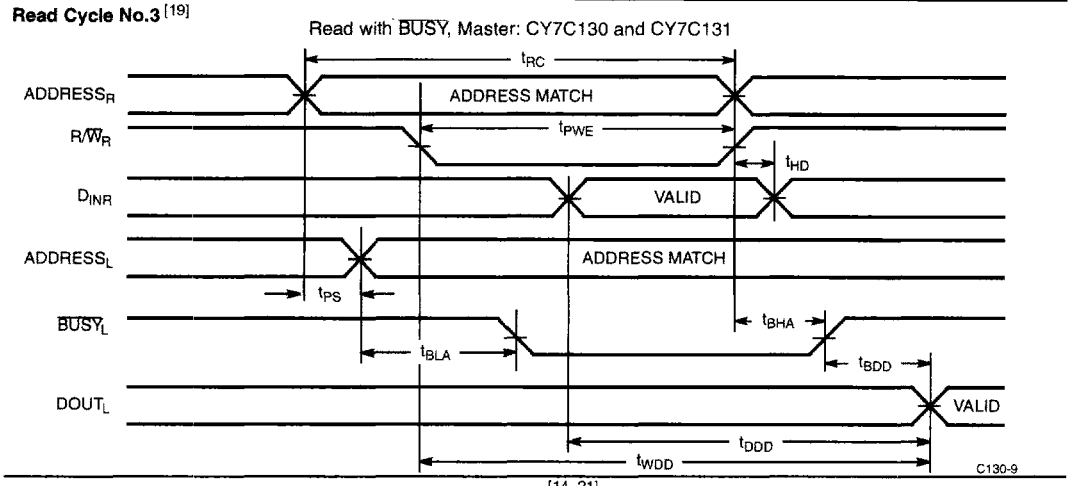
Notes:
18. R/$\overline{W}$ is HIGH for read cycle.
19. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.

Switching Waveforms (continued)

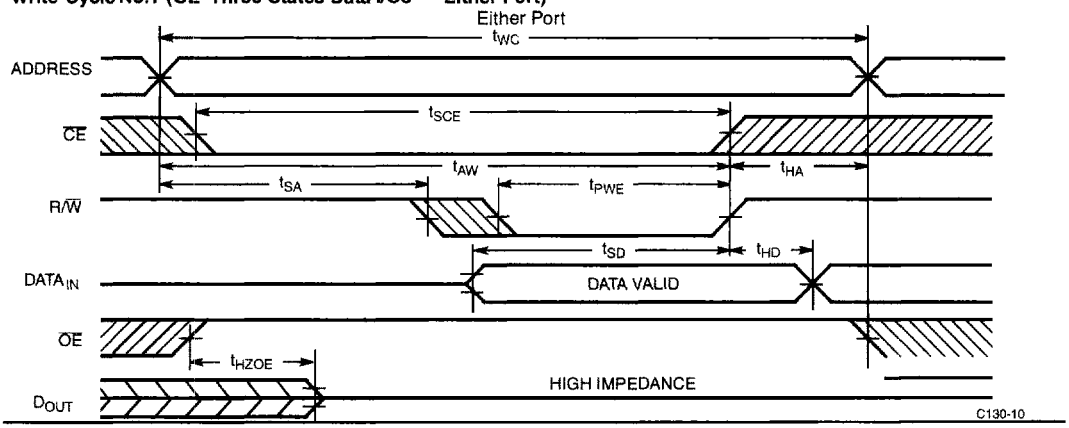
Read Cycle No. 2 [18, 20]



Read Cycle No.3 [19]



Write Cycle No.1 (OE Three-States Data I/Os - Either Port) [14, 21]

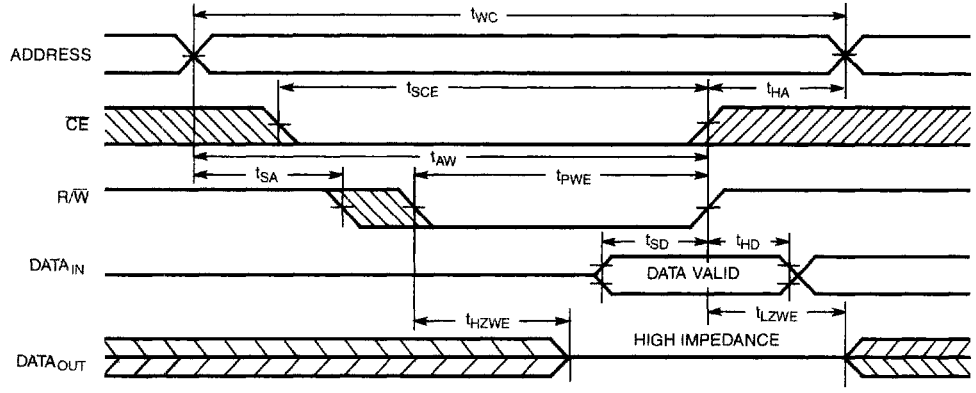


Notes:

20. Address valid prior to or coincident with CE transition LOW.
21. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

Switching Waveforms (continued)

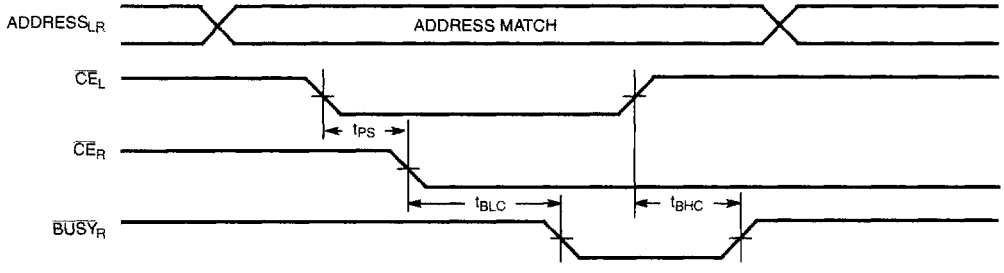
Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os - Either Port) [15, 22]



C130-11

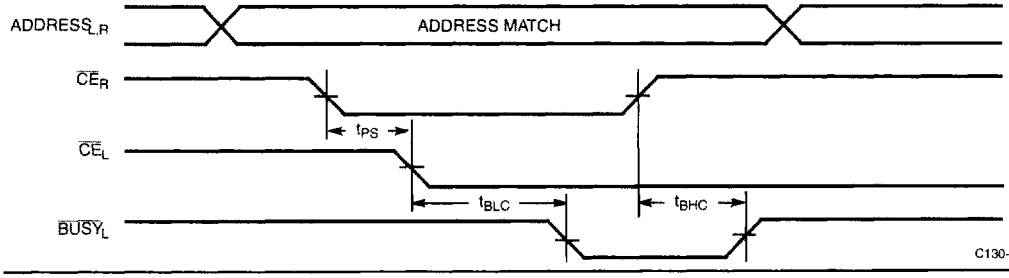
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



C130-12

$\overline{CE}_R$ Valid First:



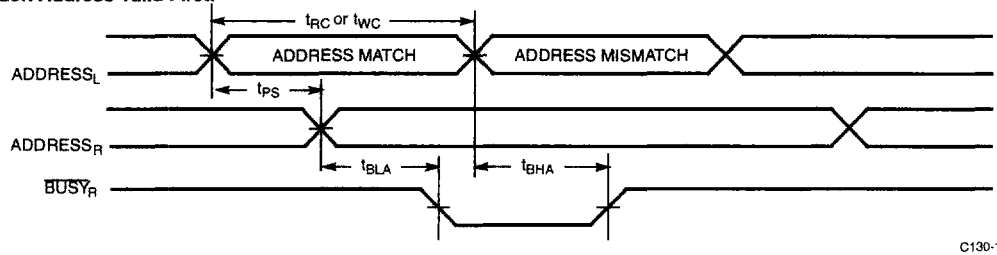
C130-13

Note:
22. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

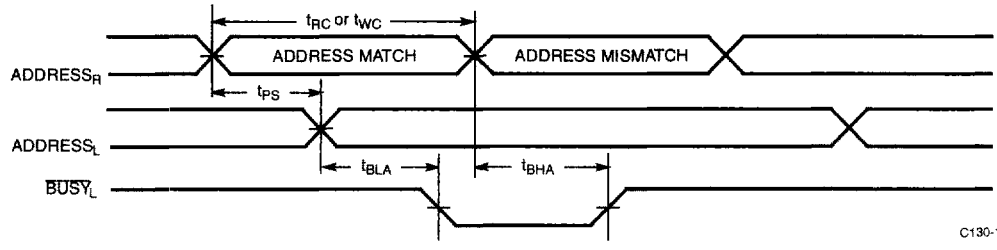
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

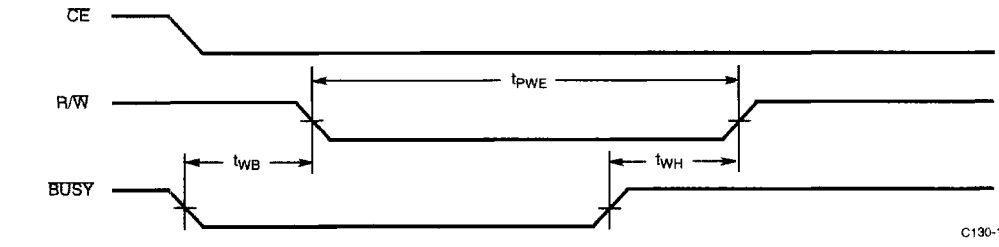


Right Address Valid First:



Busy Timing Diagram No. 3

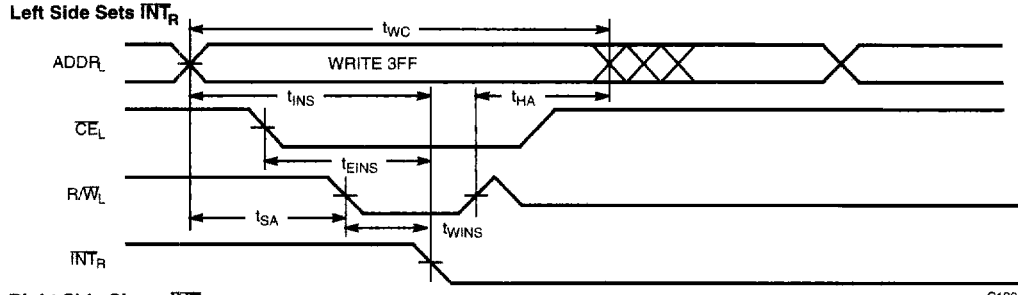
Write with $\overline{BUSY}$ (Slave:CY7C140/CY7C141)



Switching Waveforms (continued)

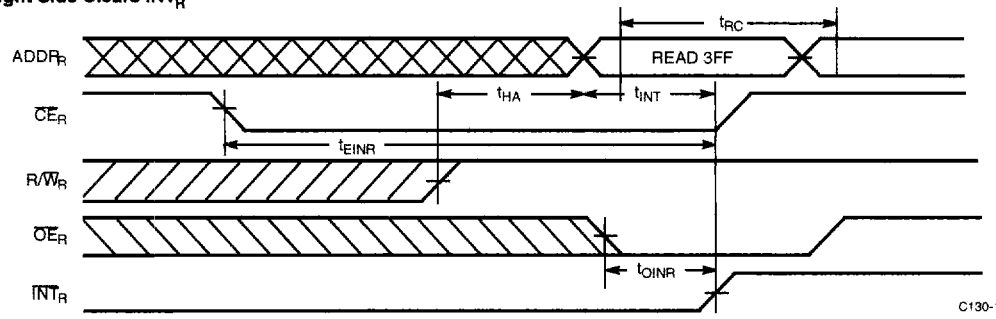
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$



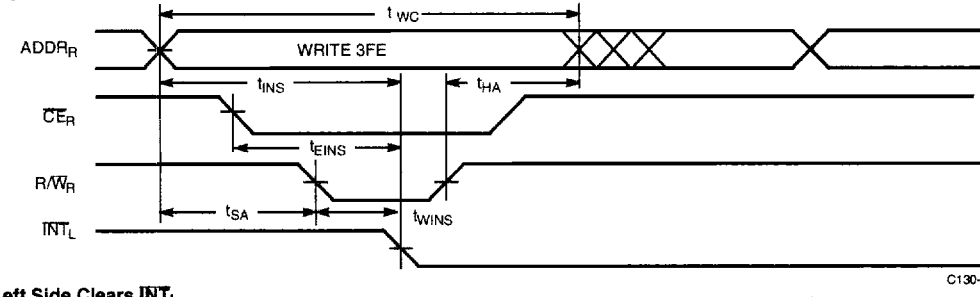
C130-17

Right Side Clears $\overline{INT}_R$



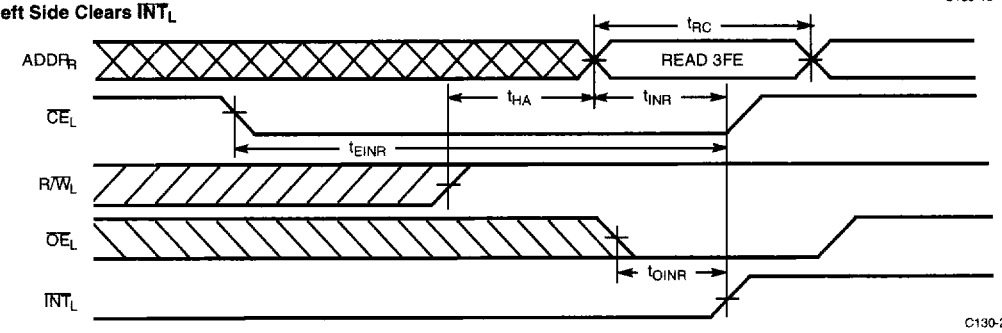
C130-18

Right Side Sets $\overline{INT}_L$



C130-19

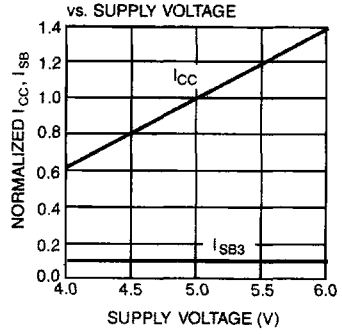
Left Side Clears $\overline{INT}_L$



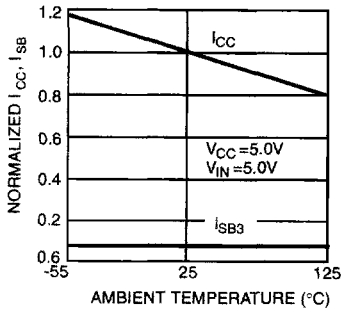
C130-20

Typical DC and AC Characteristics

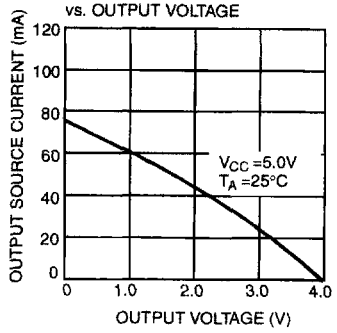
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



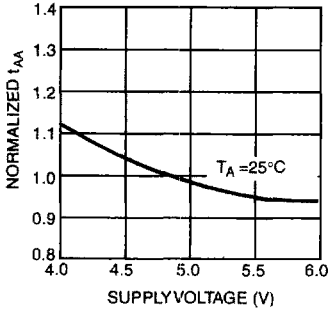
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



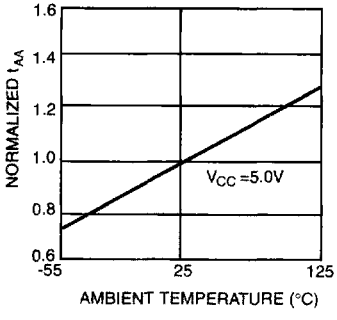
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



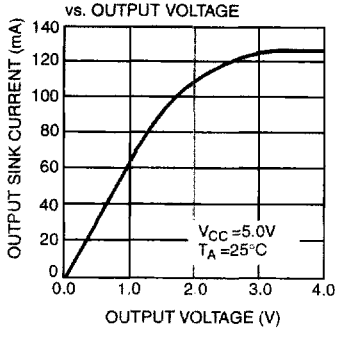
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



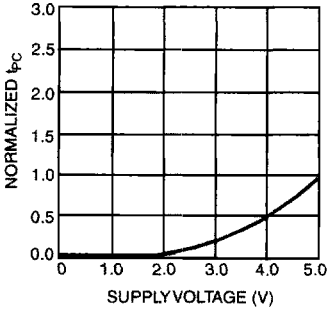
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



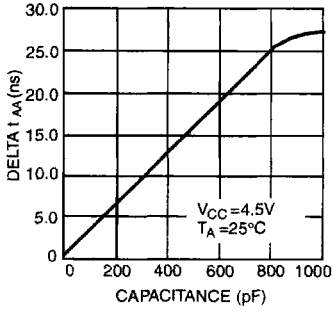
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



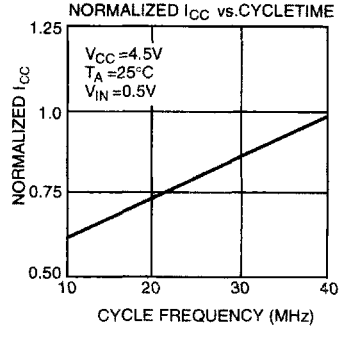
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs.CYCLETIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C130-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C130-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C131-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C131-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C131-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C131-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-55NI	N52	52-Pin Plastic Quad Flatpack	

Shaded area contains preliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C140-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C140-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C141-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C141-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C141-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C141-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-55NI	N52	52-Pin Plastic Quad Flatpack	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[23]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
23. CY7C140/CY7C141 only.

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