

FEATURES

- Spread Spectrum Clock Generator with selectable SST mode.
- Output frequency ranges: 24MHz to 200MHz.
- Selectable Center Spread Modulation.
- TTL/CMOS compatible outputs.
- 3.3V Operating Voltage.
- Low short-term jitter.
- Available in 8-Pin 150mil SOIC GREEN/RoHS compliant packaging.

PIN CONFIGURATION



FIN = 24 ~ 200 Mhz

Note: v: $30k\Omega$ Internal Pull down. ^: $30k\Omega$ Internal Pull up.

DESCRIPTION

The PLL701-21 is a Spread Spectrum Clock Generator designed for the purpose of reducing EMI in high-speed digital systems, with selectable Center Spread modulation magnitude (see table below). The device operates over a very wide range of input frequencies and provides a 1x modulated clock output.

SST BY-PASS SELECTOR

S3	Spread Spectrum Mode
0	OFF
1	ON (See below) Default

Note: S3 has an internal Pull Up. Default="1"

MODULATION MAGNITUDE SELECTION

S2 S1 S0	50	FIN Range	FOUT	Spread Spectrum Modulation		
52	01 01	30	(MHz)	FUUT	Frequency	Magnitude
0	0	0	24 - 200	X1		±0.75%
0	0	1	24 - 200	X1		±1.00%
0	1	0	24 - 200	X1		±1.25%
0	1	1	24 - 200	X1		±0.125%
1	0	0	24 - 200	X1	1111/1024	±0.25%
1	0	1	24 - 200	X1		±0.50%
1	1	0	24 - 200	X1		±0.375%
1	1	1	24 - 200	X1		±0.625%



BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Туре	Description			
FIN	1	I	Input Clock Frequency. 24MHz to 200MHz.			
S2	2	I	Digital control input for SST modulation magnitude selection. Has internal pull- up.			
S1	3	I	Digital control input for SST modulation magnitude selection. Has internal pup.			
S0	4	I	Digital control input for SST modulation magnitude selection. Has internal pull- down.			
GND	5	Р	Ground.			
FOUT	6	0	SST Modulated Clock Frequency Output.			
S3	7	I	SST By-Pass Selector. S3 has internal pull-up. Default ="1"			
VDD	8	Р	3.3V Power Supply.			

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD}		4.6	V
Input Voltage, dc	VI	-0.5	V_{DD} +0.5	V
Output Voltage, dc	Vo	-0.5	V _{DD} +0.5	V
Storage Temperature	Ts	-65	150	°C
Ambient Operating Temperature*	T _A	-40	85	°C
Junction Temperature	TJ		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.



2. DC/AC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V _{DD}		2.97		3.63	V
Input High Voltage	VIH		0.7* V _{DD}			V
Input Low Voltage	VIL				0.3* V _{DD}	V
Input High Current	Іін				100	μA
Input Low Current	١L				100	μA
Output High Voltage	V _{OH}	I_{OH} =5mA, V_{DD} =3.3V	2.4			V
Output Low Voltage	Vol	$I_{OL}=6mA$, $V_{DD}=3.3V$			0.4	V
Input Frequency	Fin		24		200	MHz
Maximum interruption of FIN					100	μs
Input Capacitance	Cin1			4		рF
Pull-up Resistor	Rpu	PIN 2, 3, 7		30		kΩ
Pull-down Resistor	R _{pd}	PIN 4		30		kΩ
Short Circuit Current	lsc			50		mA
3.3V Dynamic Supply Current	lcc	No Load		20		mA

3. TIMING CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Rise Time	Tr	Measured at 0.8V ~ 2.0V @ 3.3V, 15pF Load	0.8	0.95	1.1	ns
Fall Time	Tf	Measured at 2.0V ~ 0.8V @ 3.3V, 15pF Load	0.78	0.85	0.9	ns
Output Duty Cycle	DT		45	50	55	%
Cycle to Cycle Jitter	T _{cyc-cyc}	Over output frequency range @ 3.3V			100	ps

FUNCTIONAL DESCRIPTION

Selectable spread spectrum and modulation rates

The PLL701-21 provides Center Spread modulation, as well as a selectable modulation magnitude. Selection is made by connecting pins 2 (S2), 3 (S1) and 4 (S0) to a logical "zero" or "one", according to the modulation magnitude selection table on page 1.

Default values for S(0:3) through internal pull-up and pull-down resistor

Selection pin 4 (S0) has an internal pull-down resistor of $30k\Omega$ while pins 2, 3 and 7 (S2, S1 and S3) have an internal pull-up resistor of $30k\Omega$. This internal pull-down (or pull-up) resistor will pull the input value to a logical "zero" (or "one" respectively) by default, i.e. when no connection is made between the pin and VDD (GND respectively). In order to override the internal pull-down (pull-up), the pin has to be connected to VDD (GND respectively).



PACKAGE INFORMATION (GREEN PACKAGE COMPLIANT)



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)



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