10175-F

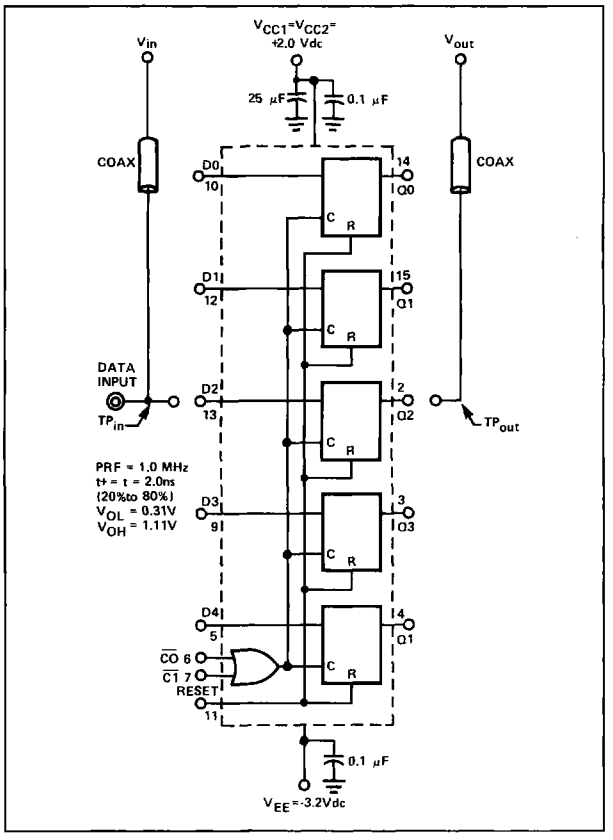
DESCRIPTION

The 10175 is a device which incorporates five D type latches with a common reset and two-input clock. While both of the clock inputs are low the outputs will follow the inputs. The outputs are latched when either of the clocks goes high. The reset is enabled only when the clock is in the high state. Open emitter outputs permit the device to be wire "OR"ed with other open emitter outputs.

FEATURES

- **High speed — 2.5ns data to output delay typical**
- **Common asynchronous reset function**
- **High Z inputs — internal 50kΩ resistors**
- **High fanout capability — drives 50 ohms**
- **Controlled output rise and fall times — 2ns typical**
- **Two separate clock pins — can be used for clock enable function**

SWITCHING TIME TEST CIRCUIT

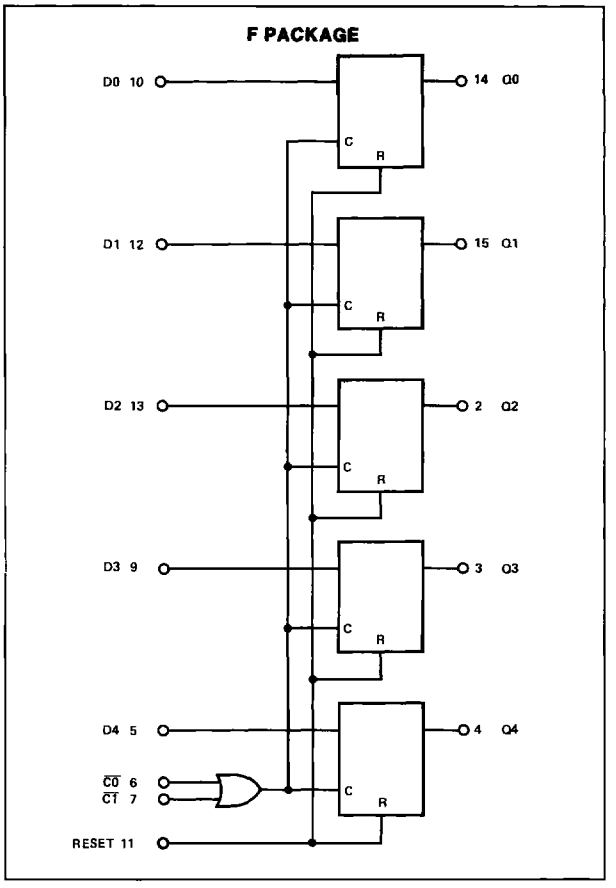


V_{CC1} = pin 1
V_{CC2} = pin 16
V_{EE} = pin 8
P_D = 400mW typ/pkg (no load)
t_{pd} = 2.5nS typ (data to output)

50-ohm termination to ground located in each scope channel input

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin.

LOGIC DIAGRAM

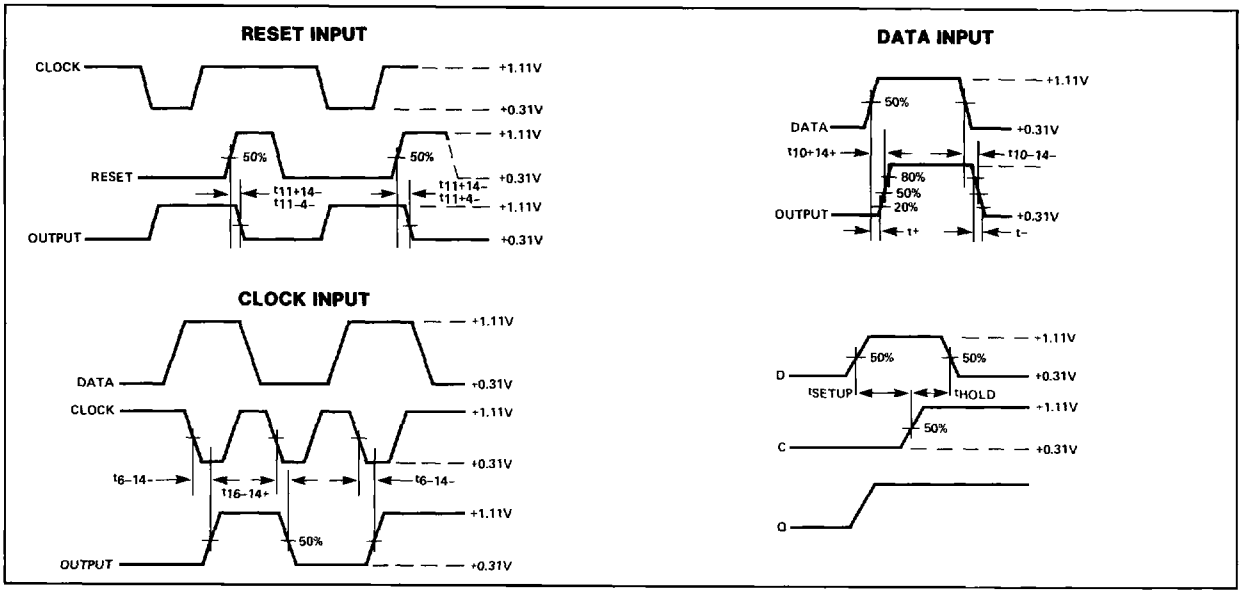


TRUTH TABLE

D	CO	C1	RESET	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Qn
X	X	H	L	Qn
X	H	X	H	L
X	X	H	H	L

10175F

VOLTAGE WAVEFORMS



NOTES:

1. t_{setup} is the minimum time before the positive transition of the clock pulse (c) that information must be present at the data input (D).
2. t_{hold} is the minimum time after the positive transition of the clock pulse (c) that information must remain unchanged at the data input (D).

LOGIC

10176-F

DESCRIPTION

The 10176 contains six D-type master-slave flip flops in a single package. Data present on the "D" inputs are entered into all six master bistables when the common clock input is low. This data is subsequently transferred to the slave bistable when the clock goes from low to high. Thus, outputs change only on a positive-going clock input transition. Data present at the inputs, therefore, will not affect the outputs except on the low to high clock transition.

FEATURES

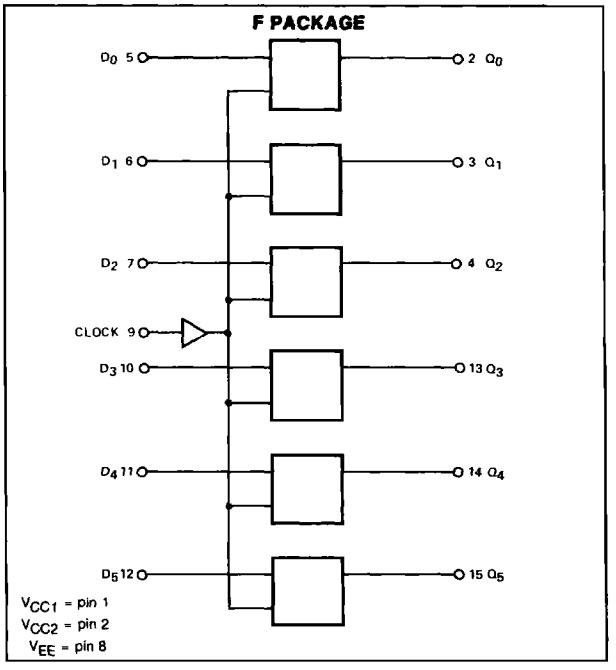
- **High speed**
  Toggle frequency = 150 MHz typical
  Propagation delay = 4.0 ns typical
- **Low power**
  480 mW per package typical
- **High fanout**
  50Ω drive capability
- **High Z inputs with 50KΩ pulldown resistors**
- **Open emitter outputs for bussing applications**

TRUTH TABLE

C	D	On+1
L	ø	Qn
L→H	L	L
L→H	H	H
H→L	ø	Qn

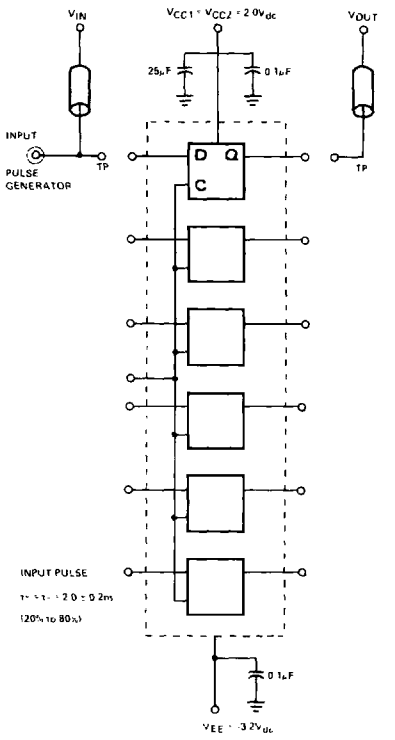
ø = Don't Care

LOGIC DIAGRAM



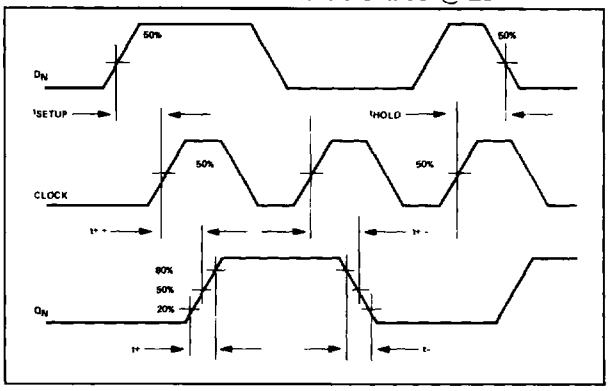
10176-F

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10179-F

DESCRIPTION

The 10179 is a look-ahead carry device that can be used with the 10180 (dual arithmetic unit) or the 10181 (4 bit ALU) to perform high speed arithmetic on long words. The device is capable of examining carry data from four arithmetic units and generating both 2nd and 4th order look-ahead carries to greatly increase system speed over that which can be obtained using ripple-carry techniques.

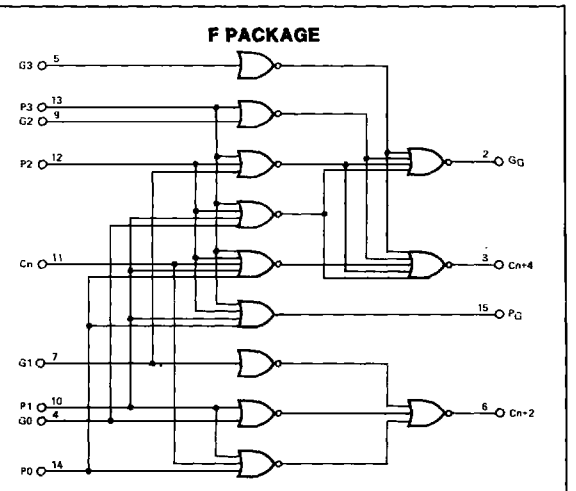
Additional features of the 10179 include high Z inputs with pull down resistors to allow unused inputs to be left open and open-emitter outputs with 50Ω drive capability.

FEATURES

- **High speed: propagation delay =**
  3.0ns TYP carry, propagate
  4.0ns TYP generate
- **Low power: 200mW TYP (no load)**
- **High fan out: can drive 50Ω lines**
- **High Z inputs with 50kΩ pull down resistors.**
- **Open emitter outputs**

LOGIC DIAGRAM

F PACKAGE



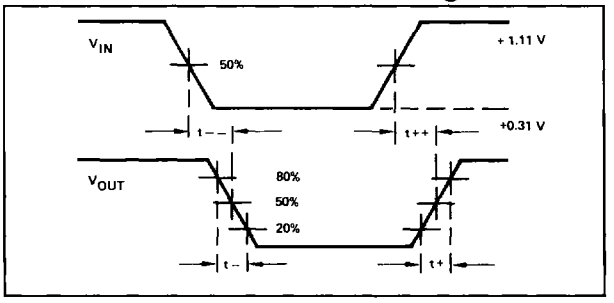
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level "1"

10179-F

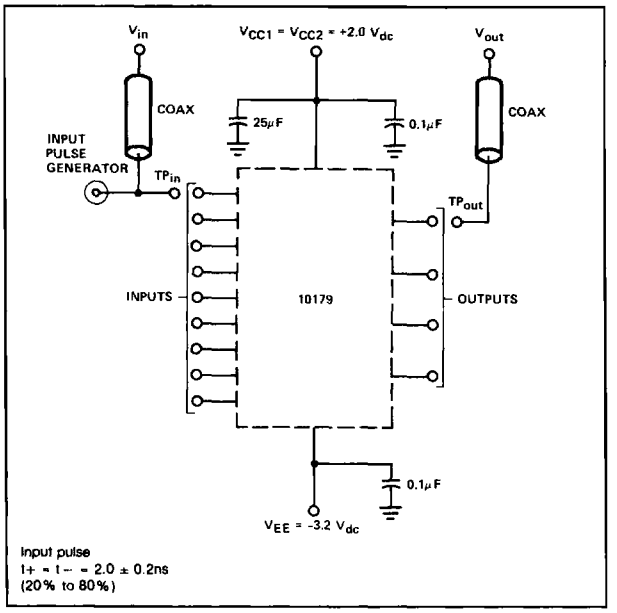
LOGIC EQUATIONS

PG= P0 + P1 + P2 + P3
GG= (G0 + P1 + P2 + P3)
(G1 + P2 + P3)
(G2 + P3) G3
Cn+2= (Cn + P0 + P1) (G0 + P1) G1
Cn+4= (Cn + P0 + P1 + P2 + P3)
(G0 + P1 + P2 + P3)
(G1 + P2 + P3) (G2 + P3) G3

PROPAGATION DELAY WAVEFORMS @ 25°C



SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t- = 2.0 ± 0.2ns
(20% to 80%)

NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
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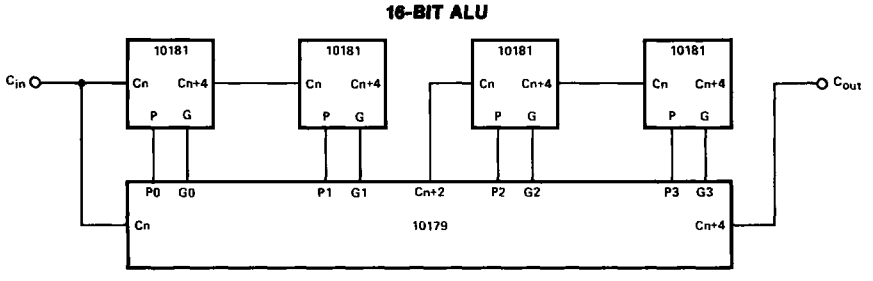
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

APPLICATION



LOGIC