MAXIM

CMOS 10 and 12 Bit Multiplying D/A Converters

T-51-09-10
T-51-09-12

General Description

The AD7530 and AD7531 are low cost CMOS multiplying digital-to-analog converters (DAC) with 10 and 12 bit resolution respectively. Both DACs operate from a single +5V to +15V supply and dissipate only 20mW.

Thin-film resistors provide typically 0.3% untrimmed gain error and 10ppm/°C maximum gain tempco. All digital inputs are compatible with both CMOS and TTL logic levels.

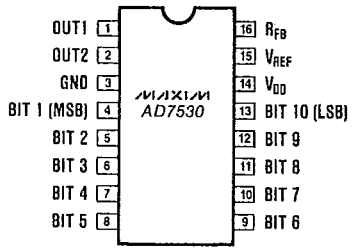
Maxim's AD7530 and AD7531 are electrically and pin compatible with Analog Devices' AD7530 and AD7531. The AD7530 is packaged in a 16-lead DIP and the AD7531 is packaged in an 18-lead DIP. Both parts are available in Small Outline packages as well.

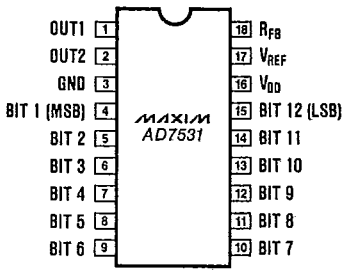
Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Pin Configurations

Top View





Features

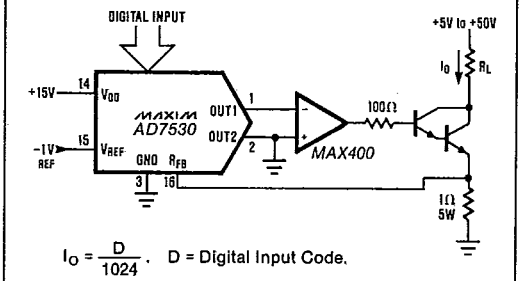
- 10 or 12 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption - 20mW
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7530JN	0°C to +70°C	Plastic DIP	0.2%
AD7530KN	0°C to +70°C	Plastic DIP	0.1%
AD7530LN	0°C to +70°C	Plastic DIP	0.05%
AD7530JCWE	0°C to +70°C	Small Outline	0.2%
AD7530KCWE	0°C to +70°C	Small Outline	0.1%
AD7530LCWE	0°C to +70°C	Small Outline	0.05%
AD7530JC/D	0°C to +70°C	Dice	0.2%
AD7530JD	-25°C to +85°C	Ceramic	0.2%
AD7530KD	-25°C to +85°C	Ceramic	0.1%
AD7530LD	-25°C to +85°C	Ceramic	0.05%
AD7530JQ	-25°C to +85°C	CERDIP**	0.2%
AD7530KQ	-25°C to +85°C	CERDIP**	0.1%
AD7530LQ	-25°C to +85°C	CERDIP**	0.05%

* *AD7530 — 16 lead package, AD7531 — 18 lead package*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*
Ordering information continued on last page.

Typical Operating Circuit



$I_O = \frac{D}{1024}$ · D = Digital Input Code.

Digital Current Controller

CMOS 10 and 12 Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature
Commercial (JN/KN/LN/JC/KC/LC) ..... 0°C to +70°C
Industrial (JD/KD/LD/JQ/KQ/LQ) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 2)						
Resolution		AD7530 AD7531	10 12			Bits
Relative Accuracy		-10V ≤ V_{REF} ≤ +10V, T_A = T_{MIN} to T_{MAX} 0.2% FSR = 8 Bits J 0.1% FSR = 9 Bits K 0.05% FSR = 10 Bits L			±0.2 ±0.1 ±0.05	% FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V, (Note 3)			2	ppm/°C
Gain Error		-10V ≤ V_{REF} ≤ +10V		0.3		% FSR
Gain Error Tempco		-10V ≤ V_{REF} ≤ +10V, (Note 3)			10	ppm/°C
Output Leakage Current		OUT1 or OUT2, T_A = T_{MIN} to T_{MAX}		300		nA
Power Supply Rejection	PSRR			50		ppm/%
V_{REF} Input Resistance	R_{REF}			10		kΩ
Reference Input Range		±10V typical input		±1		mA
AC ACCURACY						
Output Current Settling Time		To 0.05% of FSR, all digital inputs high to low and low to high.		500		ns
Feedthrough Error (Note 3,4)		All digital inputs low, V_{REF} = 20V_{P-P}, 50kHz sine			10	mV_{P-P}
ANALOG OUTPUTS						
Output Current Range		Both Outputs		±1		mA
Output Capacitance (Note 3)	C_{OUT}	All digital inputs high, OUT1 All digital inputs high, OUT2 All digital inputs low, OUT1 All digital inputs low, OUT2		120 37 37 120		pF
Output Noise (Note 3)	e_N	Both outputs, equivalent Johnson noise resistance		10		kΩ
DIGITAL INPUTS (T_A = T_{MIN} to T_{MAX})						
Low State Threshold	V_{INL}				0.8	V
High State Threshold	V_{INH}		2.4			V
Input Current		Low to high state		1		µA
Input Coding		Unipolar (Table 1) Bipolar (Table 2)	Binary Offset Binary			
POWER REQUIREMENTS						
Power Supply Range	V_{DD}		+5		+15	V
Power Supply Current	I_{DD}	Digital inputs at GND Digital inputs high or low		5	 2	nA mA
Total Power Dissipation		Including ladder		20		mW

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage if the current is limited to 30mA or less.
Note 2: Full Scale Range is 10V for unipolar mode and ±10V for bipolar mode.
Note 3: Guaranteed by design, but not 100% tested.
Note 4: To minimize feedthrough with the ceramic package, the metal lid must be grounded. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

CMOS 10 and 12 Bit Multiplying D/A Converters

Detailed Description

The basic AD7530/31 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and reference source. The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs.

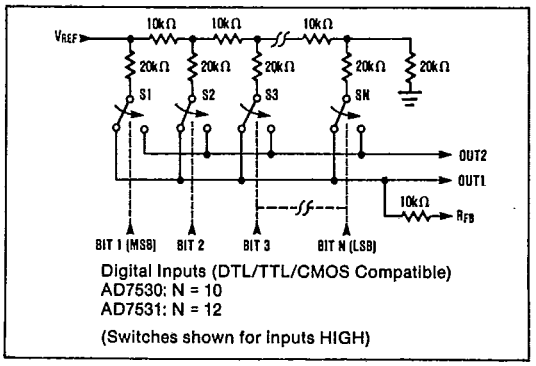


Figure 1. AD7530/AD7531 Functional Diagram

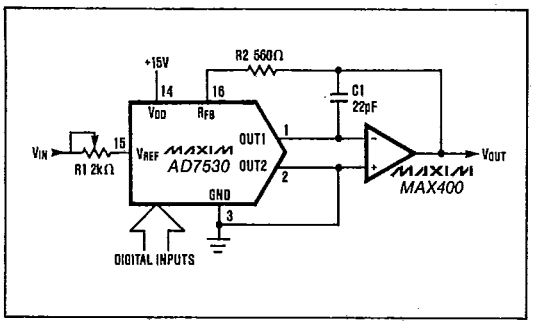


Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information

Unipolar Operation

The most common configuration for the AD7530/31 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 can be used for gain adjustment if desired, if not, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The value depends on the type of op-amp used but typically ranges from 10 to 50pF.

The output op-amp's offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the AD7530 and 250nA for the AD7531.

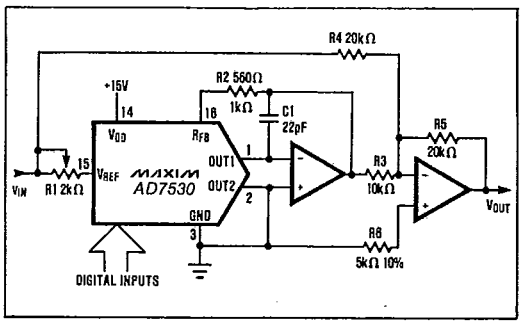


Figure 3. Bipolar Operation (4-Quadrant Multiplicaiton)

Table 1: Code Table (AD7530) — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(½+2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(½-2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Note: 1 LSB = 2^{-10} V_{REF} (AD7530)

Table 2: Code Table (AD7530) — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

Note: 1 LSB = 2^{-9} V_{REF} (AD7530)

CMOS 10 and 12 Bit Multiplying D/A Converters

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in figure 3. A second amplifier and three matched resistors are required. The output vs. code table is listed in Table 2. In multiplying applications, the MSB sets polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

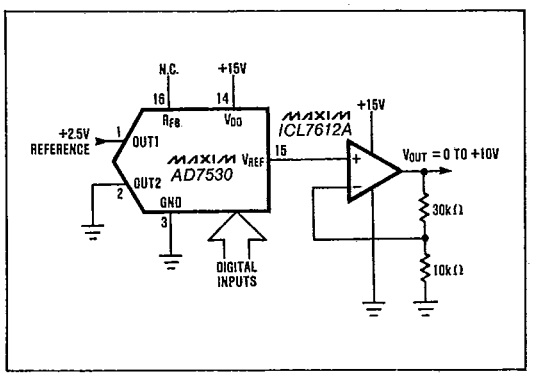


Figure 4. Single Operation Using Voltage Mode

Voltage Mode (Single Supply)

The AD7530 is connected as a voltage output DAC in Figure 4. OUT1 is connected to the reference input and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). This outptut is usually buffered with an op-amp.

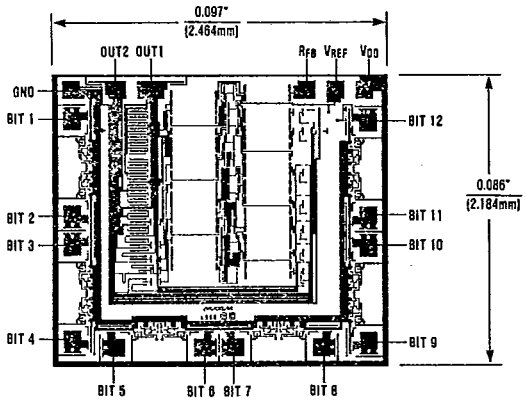
An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted in voltage mode. The reference input (voltage at OUT1) must always be positive and is limited to no more than +3.5V when V_{DD} is +15V. If the reference voltage is greater than +3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

A common error source in dymamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough from V_{REF} and the digital inputs can be minimized with guard traces to isolate the digital inputs, V_{REF}, and the DAC outputs.

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7531JN	0°C to +70°C	Plastic DIP	0.2%
AD7531KN	0°C to +70°C	Plastic DIP	0.1%
AD7531LN	0°C to +70°C	Plastic DIP	0.05%
AD7531JCWN	0°C to +70°C	Small Outline	0.2%
AD7531KCWN	0°C to +70°C	Small Outline	0.1%
AD7531LCWN	0°C to +70°C	Small Outline	0.05%
AD7531KJC/D	0°C to +70°C	Dice	0.2%
AD7531JD	-25°C to +85°C	Ceramic	0.2%
AD7531KD	-25°C to +85°C	Ceramic	0.1%
AD7531LD	-25°C to +85°C	Ceramic	0.05%
AD7531JQ	-25°C to +85°C	CERDIP**	0.2%
AD7531KQ	-25°C to +85°C	CERDIP**	0.1%
AD7531LQ	-25°C to +85°C	CERDIP**	0.05%

** AD7530 — 16 lead package, AD7531 — 18 lead package*

*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*