

# SONY CXK58257AP/AM -70LX/85LX/10LX/12LX -70LLX/85LLX/10LLX/12LLX\*

## 32768-word × 8-bit High Speed CMOS Static RAM

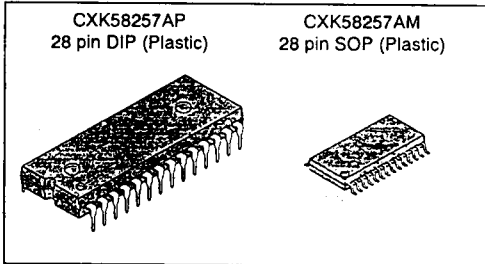
### Description

CXK58257AP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

\* DIP covers only LX-version.

### Features

- Extended operating temperature range: -25 to 85 °C
- Fast access time: (Access time)
  - CXK58257AP/AM-70LX,70LLX 70ns (Max.)
  - CXK58257AP/AM-85LX,85LLX 85ns (Max.)
  - CXK58257AP/AM-10LX,10LLX 100ns (Max.)
  - CXK58257AP/AM-12LX,12LLX 120ns (Max.)
- Low power operation:
  - CXK58257AM-70LLX, 85LLX,10LLX,12LLX;
    - Standby : 1 μW (Typ.)
    - Operation : 15mW (Typ.)
  - CXK58257AP/AM-70LX, 85LX,10LX,12LX;
    - Standby : 2.5 μW (Typ.)
    - Operation : 15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time



- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 600mil DIP and 450mil SOP

### Function

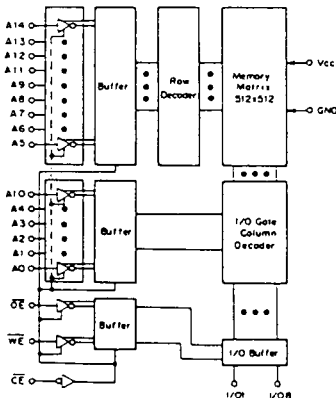
32768-word × 8-bit static RAM

### Structure

Silicon gate CMOS IC

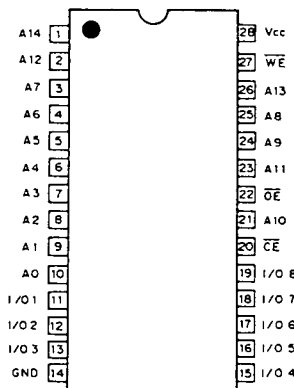
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### Block diagram



### Pin Configuration

(Top View)



### Pin Description

Symbol	Description
A <sub>0</sub> to A <sub>14</sub>	Address input
I/O <sub>1</sub> to I/O <sub>8</sub>	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

**Absolute Maximum Ratings**

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit	
Supply voltage	V <sub>CC</sub>	- 0.5 to +7.0	V	
Input voltage	V <sub>IN</sub>	- 0.5 * to V <sub>CC</sub> +0.5	V	
Input and output voltage	V <sub>I/O</sub>	- 0.5 * to V <sub>CC</sub> +0.5	V	
Allowable power dissipation	P <sub>D</sub>	CXK58257AP	1.0	W
		CXK58257AM	0.7	
Operating temperature	T <sub>opr</sub>	- 25 to +85	°C	
Storage temperature	T <sub>stg</sub>	- 55 to +150	°C	
Soldering temperature • time	T <sub>solder</sub>	260 • 10	°C • sec	

\* V<sub>IN</sub>, V<sub>I/O</sub> = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE	OE	WE	Mode	I/O1 to I/O8	V <sub>CC</sub> Current
H	x	x	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	Not selected	High Z	I <sub>CC1</sub> , I <sub>CC2</sub>
L	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub>
L	x	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub>

x : "H" or "L"

**DC Recommended Operating Conditions** (Ta= - 25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	- 0.3*	—	0.8	V

\* V<sub>IL</sub> = - 3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**

**• DC and operating characteristics**

(Vcc=5V ± 10%, GND=0V, Ta= - 25 to +85 °C)

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit	
			Min.	Typ. *	Max.	Min.	Typ. *	Max.		
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	- 0.5	—	0.5	- 0.5	—	0.5	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V <sub>I/O</sub> =GND to V <sub>CC</sub>	- 0.5	—	0.5	- 0.5	—	0.5	μA	
Operating power supply current	I <sub>CC1</sub>	$\overline{CE}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	—	3	10	—	3	10	mA	
		$\overline{CE} \leq 0.2V$ V <sub>IN</sub> ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V	—	1	5	—	1	5		
Average operating current	I <sub>CC2</sub>	Cycle=Min, Duty=100% I <sub>OUT</sub> =0mA	70LX/70LLX	—	30	60	—	30	60	mA
			85LX/85LLX	—	25	60	—	25	60	
			10LX/10LLX	—	23	60	—	23	60	
			12LX/12LLX	—	20	60	—	20	60	
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{CC}-0.2V$	-25 to 85 °C	—	—	50	—	—	10	μA
			-25 to 70 °C	—	—	25	—	—	5	
			-25 to 40 °C	—	—	5	—	—	1	
			25 °C	—	0.5	2	—	0.2	0.5	
	I <sub>SB2</sub>	$\overline{CE}=V_{IH}$	—	0.4	2	—	0.4	2	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	—	—	0.4	V	

\* Vcc=5V, Ta=25 °C

**I/O capacitance**

(Ta=25 °C, f=1MHz)

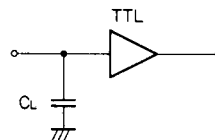
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	—	6	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	—	8	pF

**Note)** This parameter is sampled and is not 100% tested.

5

**AC characteristics****● AC test conditions** $(V_{CC}=5V \pm 10\%, T_a=-25 \text{ to } +85^\circ\text{C})$ 

Item		Conditions
Input pulse high level		$V_{IH}=2.4V$
Input pulse low level		$V_{IL}=0.6V$
Input rise time		$t_r=5ns$
Input fall time		$t_f=5ns$
Input and output reference level		1.5V
Output load conditions	85LX/85LLX/10LX/ 10LLX/12LX/12LLX/	$C_L^* = 100pF, 1TTL$
	70LX/70LLX	$C_L^* = 30pF, 1TTL$

\*  $C_L$  includes scope and jig capacitances.

### • Read cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	70	—	85	—	100	—	120	—	ns
Address access time	t <sub>AA</sub>	—	70	—	85	—	100	—	120	ns
Chip enable access time	t <sub>CO</sub>	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t <sub>OE</sub>	—	35	—	45	—	50	—	60	ns
Output hold from address change	t <sub>OH</sub>	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub>	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ</sub> *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	0	30	0	30	0	30	0	30	ns

\* t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

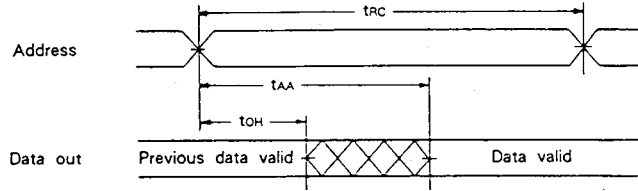
### • Write cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t <sub>AW</sub>	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t <sub>CW</sub>	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t <sub>DW</sub>	30	—	30	—	35	—	40	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	50	—	50	—	60	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	5	—	5	—	5	—	5	—	ns
Write recovery time ( $\overline{CE}$ )	t <sub>WR1</sub>	0	—	0	—	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	0	25	0	25	0	25	0	25	ns

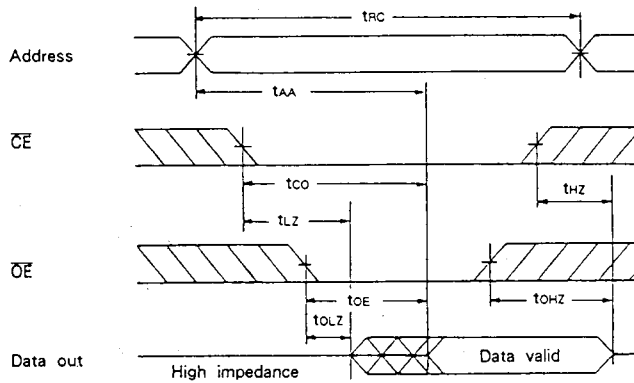
\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

**Timing Waveform**

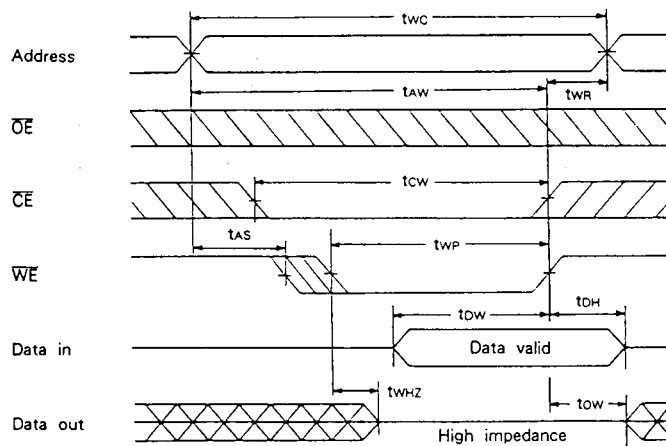
- Read cycle (1) :  $\overline{CE}=\overline{OE}=V_{IL}, \overline{WE}=V_{IH}$



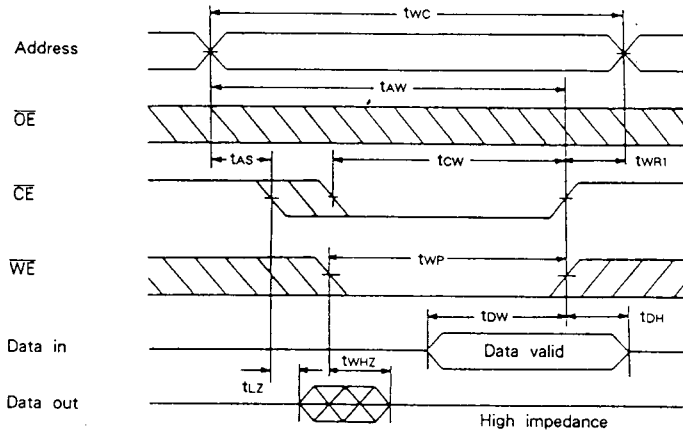
- Read cycle (2) :  $\overline{WE}=V_{IH}$



- Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE}$  control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

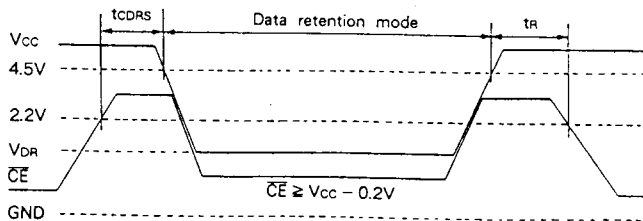
( $T_a = -25$  to  $85^\circ\text{C}$ )

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Data retention voltage	$V_{DR}$	$\overline{CE} \cong V_{CC} - 0.2V$	2.0	—	5.5	2.0	—	5.5	V	
Data retention current	$I_{CCDR1}$	$V_{CC} = 3.0V$ $\overline{CE} \cong 2.8V$	-25 to $85^\circ\text{C}$	—	—	20	—	—	6	$\mu\text{A}$
			-25 to $70^\circ\text{C}$	—	—	10	—	—	3	
			-25 to $40^\circ\text{C}$	—	—	2	—	—	0.6	
			$25^\circ\text{C}$	—	0.25	1	—	0.1	0.3	
	$I_{CCDR2}$	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \cong V_{CC} - 0.2V$	—	0.5**	50	—	0.2**	10	$\mu\text{A}$	
Data retention setup time	$t_{CDRS}$	Chip disable to data retention mode	0	—	—	0	—	—	ns	
Recovery time	$t_R$		$t_{RC}^*$	—	—	$t_{RC}^*$	—	—	ns	

\*  $t_{RC}$  : Read cycle time

\*\*  $V_{CC} = 5V, T_a = 25^\circ\text{C}$

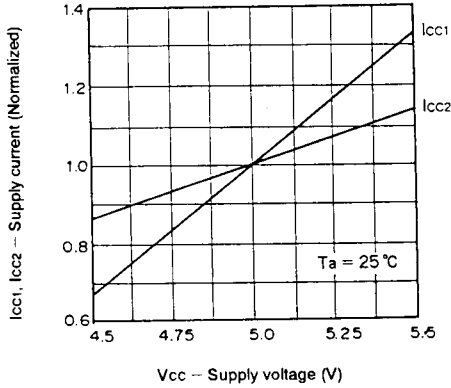
Data retention waveform



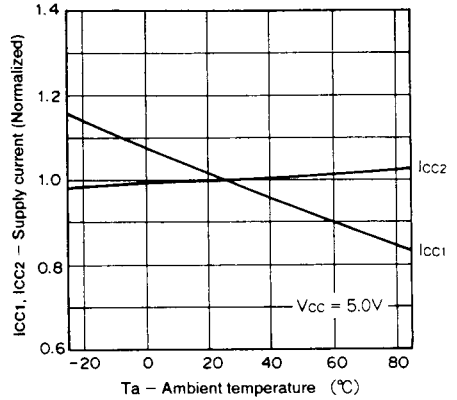
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Example of Representative Characteristics

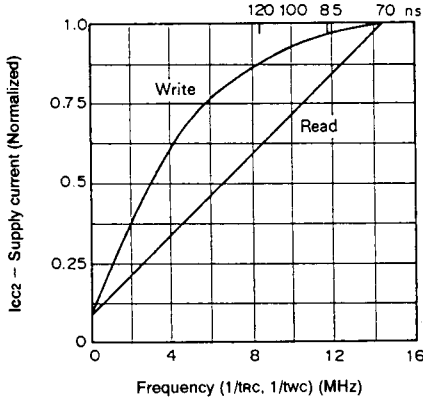
Supply current vs. Supply voltage



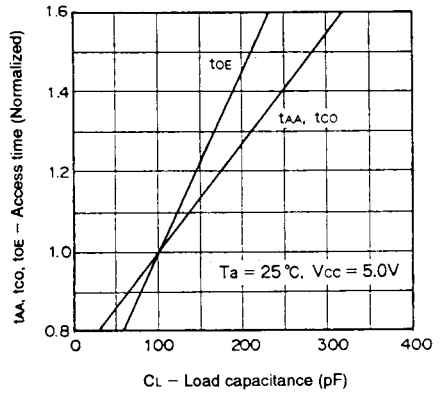
Supply current vs. Ambient temperature



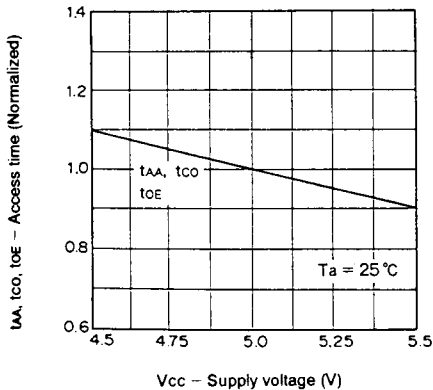
Supply current vs. Frequency



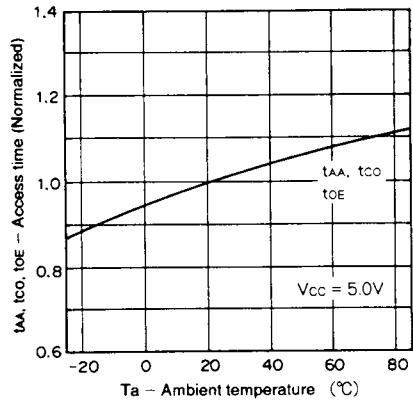
Access time vs. Load capacitance



Access time vs. Supply voltage

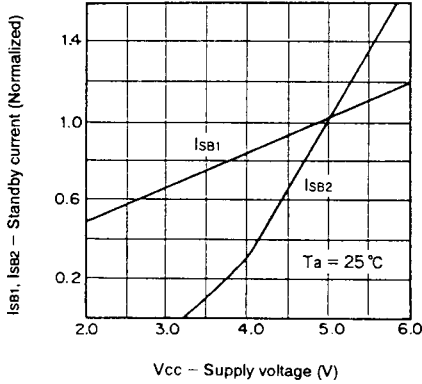


Access time vs. Ambient temperature

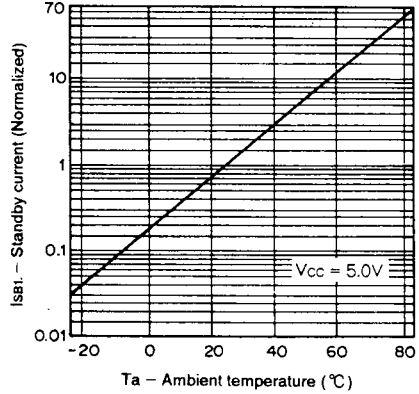




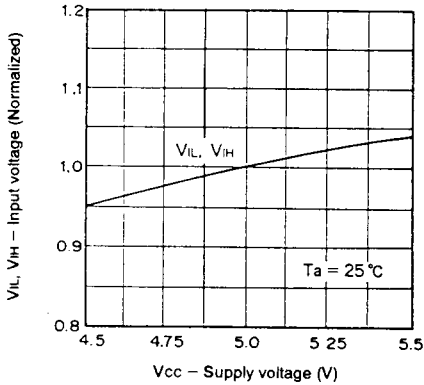
Standby current vs. Supply voltage



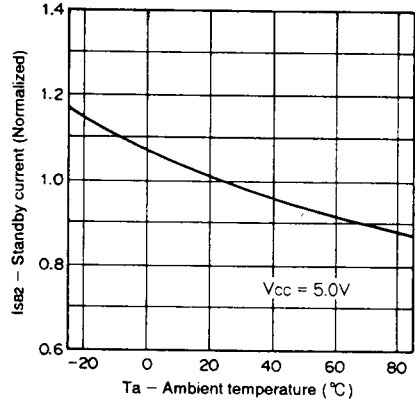
Standby current vs. Ambient temperature



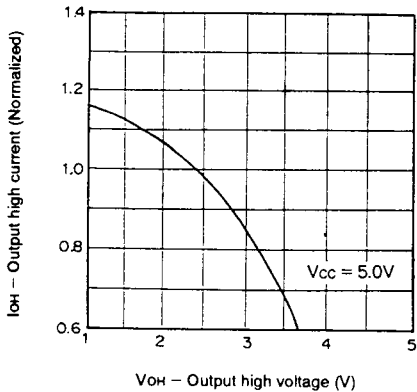
Input voltage level vs. Supply voltage



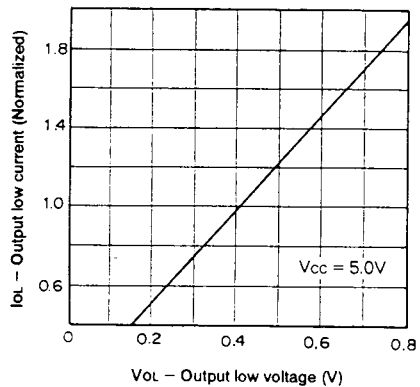
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage

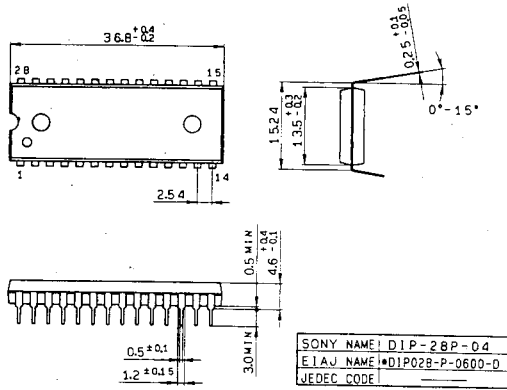


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Package Outline Unit : mm

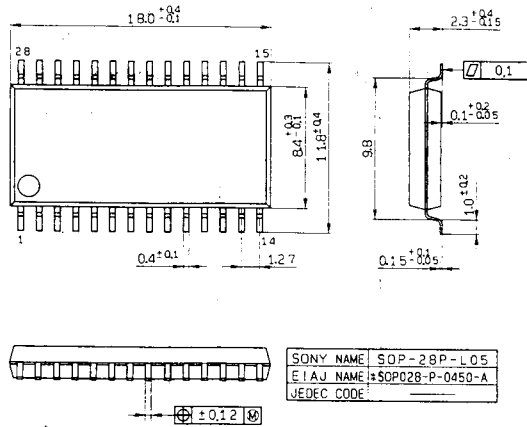
CXK58257AP

28pin DIP (Plastic) 600mil 4.2g

















CXK58257AM

28pin SOP (Plastic) 450mil



T-90-20

### 7. Sony Package Product Name

Type	Package name		Package	Features				
	Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction	
Inserted	Standard	D I P	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction	
Surface mounted	Standard flat package	Q F P	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		L C C	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

\*P.....Plastic, C.....Ceramic