Finisar

Product Specification

2.125 Gb/s Short-Wavelength 2x6 Pin SFF Transceiver

FTRJ8519U1xNL

PRODUCT FEATURES

- Up to 2.125 Gb/s bi-directional data links
- 2x6 pin SFF-"like" footprint
- Built-in digital diagnostic functions
- 850nm Oxide VCSEL laser transmitter
- Duplex LC connector
- Very low jitter
- Up to 500m on 50/125µm MMF, 300m on 62.5/125µm MMF
- Metal enclosure, for lower EMI
- Single 3.3V power supply
- Low power dissipation <750mW
- Extended operating temperature range: -10°C to 85°C

APPLICATIONS

- 1.25 Gb/s 1000Base-SX Ethernet
- Dual Rate 1.063/2.125 Gb/s Fibre Channel

Finisar's FTRJ8519U1xNL Small Form Factor (SFF) transceivers comply with the 2x5 standard package defined by the Small Form Factor Multi-Sourcing Agreement (MSA)[1] with the exception of two additional pins for the 2-wire interface. They are simultaneously compatible with with Gigabit Ethernet as specified in IEEE Std 802.3[2] and Fibre Channel FC-PH, PH2, PH3[2] and FC-PI 13.0[3].

PRODUCT SELECTION

FTRJ8519U1xNL

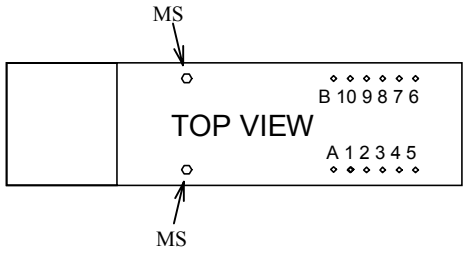
x	G	2 Grounding Pins, Short EMI shield
	K	2 Grounding Pins, Long EMI shield

I. Pin Descriptions

Pin	Symbol	Name/Description	Logic Family
MS	MS	Mounting Studs are for mechanical attachment and are connected to chassis ground. **Chassis ground is internally isolated from circuit grounds.** Connection to user's chassis ground plane is recommended.	NA
1	V_{EER}	Receiver Ground (Common with Transmitter Ground)	NA
2	V_{CCR}	Receiver Power Supply (Common with Transmitter Power)	NA
3	SD	Signal Detect. Logic 1 indicates normal operation.	LVTTL
4	RD-	Receiver Inverted DATA out. AC Coupled	See Rx spec.
5	RD+	Receiver Non-inverted DATA out. AC Coupled	See Rx spec.
6	V_{CCT}	Transmitter Power Supply	NA
7	V_{EET}	Transmitter Ground (Common with Receiver Ground)	NA
8	T_{DIS}	Transmitter Disable (Common with Receiver Power)	LVTTL
9	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	See Tx spec.
10	TD-	Transmitter Inverted DATA in. AC Coupled	See Tx spec.
A	SDA	Two Wire Digital Diagnostics Data Interface	See Note 1
B	SCL	Two Wire Digital Diagnostics Clock Interface	See Note 1

Notes:

1. Should be pulled up with 4.7k – 10kohms on host board to a voltage between 2.0V and V_{CC}.



II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	T_S	-40		100	°C	
Case Operating Temperature	T_{OP}	-10		85	°C	
Relative Humidity	RH	0		85	%	1
Lead Soldering Temperature/Time				260/10	°C/s	

Notes:
1. Non condensing.

III. Electrical Characteristics (T_{OP} = -10 to 85 °C, V_{CC} = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.0		3.6	V	
Supply Current	Icc		180	240	mA	
Transmitter						
Input differential impedance	R_{in}	90	100	110	Ω	1
Single ended data input swing	Vin,pp	250		1200	mV	
Transmit Disable Voltage	V_D	2		Vcc	V	
Transmit Enable Voltage	V_{EN}	Vee		Vee+ 0.8	V	2
Receiver						
Output differential impedance	Rout	90	100	110	Ω	1
Single ended data output swing	Vout,pp	250	350	550	mV	3
Data output rise/fall time	t_r/ t_f		90	180	ps	4
Mask Margin			45%			
Signal Detect Normal	SD_{normal}			Vcc_{HOST}	V	5
Signal Detect Fault	SD_{fault}	Vee		Vee+0.5	V	5
Power Supply Rejection	PSR			100	mVpp	6
Deterministic Jitter Contribution (p-p)	RX ΔDJ			51.7	ps	7
Total Jitter Contribution (p-p)	RX ΔTJ		<65	122.4	ps	8

Notes:
1. AC coupled.
2. Or open circuit.
3. Into 100 Ω differential termination. Data pattern is PRBS 2^7-1.
4. 20 – 80 %.
5. Signal detect is LVTTL. Logic 1 indicates normal operation; logic 0 indicates no signal detected.
6. All transceiver specifications are compliant with a power supply sinusoidal modulation of 20 Hz to 1.5 MHz up to specified value applied through the power supply filtering network shown on page 23 of the Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA), September 14, 2000.
7. Measured with DJ-free data input signal. In actual application, output DJ will be the sum of input DJ and ΔDJ.
8. If measured with TJ-free data input signal. In actual application, output TJ will be given by:

$$TJ_{OUT} = DJ_{IN} + \Delta DJ + \sqrt{(TJ_{IN} - DJ_{IN})^2 + (\Delta TJ - \Delta DJ)^2}$$

IV. Optical Characteristics (T_{OP} = -10 to 85 °C, V_{CC} = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Output Opt. Pwr: 50 or 62.5 MMF	P_{OUT}	-9		-4	dBm	1
Optical Wavelength	λ	830		860	nm	
Spectral Width	σ			0.85	nm	
Optical Modulation Amplitude	OMA_{Tx}	196			µW	2
Optical Rise/Fall Time	t_r/ t_f		100	150	ps	3
Relative Intensity Noise	RIN			-120	dB/Hz	
Deterministic Jitter Contribution (p-p)	TX ΔDJ		20	56.5	ps	4
Total Jitter Contribution (p-p)	TX ΔTJ		<65	119	ps	5
Extinction Ratio	ER	9				6
Mask Margin			45%			
Receiver						
Receiver Sensitivity = 1.0625 Gb/s	Rx_{SENS}		-22	-20	dBm	7
Receiver Sensitivity = 2.125 Gb/s	Rx_{SENS}		-20	-18	dBm	7
Receiver Sensitivity = 1.25 Gb/s	Rx_{SENS}		-22	-20	dBm	8
Stressed RX sens. =1.0625 Gb/s		0.055			mW	9
Stressed RX sens. =2.125 Gb/s		0.096			mW	9
Stressed RX sens. = 1.25 Gb/s			-18	-13.5	dBm	10
Average Received Power	Rx_{MAX}			0	dBm	
Receiver Elec. 3 dB cutoff freq.				1500	MHz	
Optical Center Wavelength	λ_C	770		860	nm	
Return Loss	RL	12			dB	
Signal Detect Normal	SD_{normal}			-18	dBm	
Signal Detect Fault	SD_{fault}	-30			dBm	
Signal Detect Hysteresis		0.5			dB	

Notes:
1. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
2. Equivalent extinction ratio specification for Fibre Channel. Allows smaller ER at higher average power.
3. Unfiltered, 20-80%. Complies with FC 1x and 2x eye mask when filtered.
4. Measured with DJ-free data input signal. In actual application, output DJ will be the sum of input DJ and ΔDJ.
5. If measured with TJ-free data input signal. In actual application, output TJ will be given by:

$$TJ_{OUT} = DJ_{IN} + \Delta DJ + \sqrt{(TJ_{IN} - DJ_{IN})^2 + (\Delta TJ - \Delta DJ)^2}$$

6. Gigabit Ethernet data rate only (1.25 Gb/s)
7. Specifications are for 50 micro-meter or 62.5 micro-meter fiber at 10^{-12} BER.
8. As measured with 9dB extinction ratio
9. Measured with conformance signals defined in FC-PI 13.0 specifications.
10. Measured with conformance signals defined in IEEE 802.3 specifications.

V. General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Data Rate	BR		1.062, 1.25 2.125		Gb/sec	1
Bit Error Rate	BER			10^{-12}		4
Fiber Length on 50/125µm MMF	L			550 300	m	2 3
Fiber Length on 62.5/125µm MMF	L			300 150	m	2 3
EMI Margin		10			dB	5
ESD Air Discharge		15			kV	6
ESD Contact Discharge		2			kV	7

Notes:
1. Gigabit Ethernet and 1x, 2x Fibre Channel compatible, per IEEE 802.3 and FC-PI 13.0 respectively. Typical maximum data rate extends to 2.5Gb/s.
2. At 1.0625 Gb/s Fibre Channel and 1.25 Gb/s Gigabit Ethernet data rates.
3. At 2.125 Gb/s Fibre Channel data rate.
4. At 1.0625 and 2.125Gb/s with PRBS 2^7-1.
5. EMI testing is performed with four operating modules in standard Finisar four port EMI chassis. Minimum margin with four modules operating is 10dB using FCC Class A limits.
6. Air Discharge ESD testing is performed by applying 15kV to the transmit and receive ports to a non-operating module. Passing criteria is that no damage to the module occurs.
7. Contact discharge ESD testing is performed by applying 2kV directly to the transmit and receive ports while transmitting live traffic. Passing criteria is that no errors can occur during or after the discharges.

VI. Environmental Specifications

Finisar SFF transceivers have an extended operating temperature range from –10°C to +85°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	-10		85	°C	
Storage Temperature	T_{sto}	-40		100	°C	

Notes:
1. SFF transceivers may be water washed. However, the process must be followed by a baking step at 80°C for one hour, to ensure the drying of any water which may be trapped inside the shells of the modules.

VII. Regulatory Compliance

Finisar transceivers are Class 1 Laser Products and comply with US FDA regulations. These products are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950. Copies of certificates are available at Finisar Corporation upon request.

VIII. Digital Diagnostic Functions

Finisar FTRJ8519U1xNL 2x6 transceivers provide a unique digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

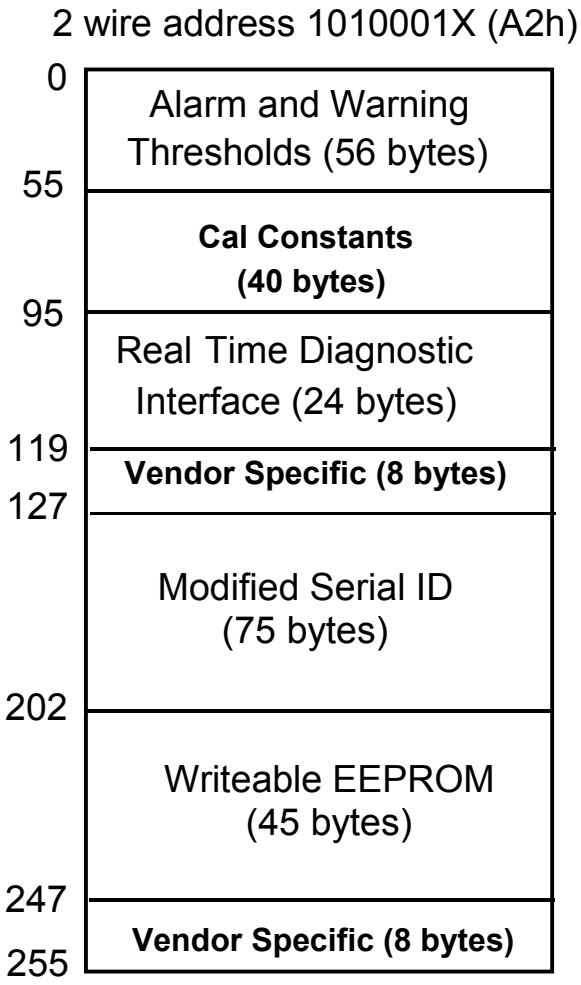
In order to access the digital diagnostics functionality, the transceivers have a 2-wire serial communication protocol that is similar to that defined in the SFP MSA[4]. The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h) only. The memory map for this interface is defined below. Additional information, including details on the electrical interface, is described in Finisar Application Note AN-2030: "Digital Diagnostics Monitoring Interface for SFP Optical Transceivers". (Note: only pages 17-35 of this Application note, including Section 4 are relevant to Finisar 2x6 transceivers.)

The standard SFP MSA serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information. Finisar 2x6 transceivers provide access to a condensed version of this information, over the 2-wire serial interface at the 8 bit address 1010000X (A2h) in bytes 128-190.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL) is generated by the host. The positive edge clocks data into the 2x6 transceiver into those segments of the E^2PROM that are not write-protected. The negative edge clocks data from the 2x6 transceiver. The serial data signal (SDA) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

Digital diagnostics for the FTRJ8519U1xNL are internally calibrated by default.

IX. Digital Diagnostic Memory Map



256 Byte Memory Map at Address 1010001X (A2h)				
Byte Address	***Size*** *(Bytes) or (bits)*	**Field Name**	***Value***	***Value Meaning***
ALARM AND WARNING THRESHOLDS				
00-01	2	Temp High Alarm		MSB at low address
02-03	2	Temp Low Alarm		MSB at low address
04-05	2	Temp High Warning		MSB at low address
06-07	2	Temp Low Warning		MSB at low address
08-09	2	Voltage High Alarm		MSB at low address
10-11	2	Voltage Low Alarm		MSB at low address
12-13	2	Voltage High Warning		MSB at low address
14-15	2	Voltage Low Warning		MSB at low address
16-17	2	Bias High Alarm		MSB at low address
18-19	2	Bias Low Alarm		MSB at low address

20-21	2	Bias High Warning		MSB at low address
22-23	2	Bias Low Warning		MSB at low address
24-25	2	TX Power High Alarm		MSB at low address
26-27	2	TX Power Low Alarm		MSB at low address
28-29	2	TX Power High Warning		MSB at low address
30-31	2	TX Power Low Warning		MSB at low address
32-33	2	RX Power High Alarm		MSB at low address
34-35	2	RX Power Low Alarm		MSB at low address
36-37	2	RX Power High Warning		MSB at low address
38-39	2	RX Power Low Warning		MSB at low address
40-55	16	Reserved		Reserved for future monitored quantities
CALIBRATION CONSTANTS FOR EXTERNAL CALIBRATION OPTION				
56-59	4	Rx_PWR(4)		0 (32 bit IEEE floating point)
60-63	4	Rx_PWR(3)		0 (32 bit IEEE floating point)
64-67	4	Rx_PWR(2)		0 (32 bit IEEE floating point)
68-71	4	Rx_PWR(1)		1 (32 bit IEEE floating point)
72-75	4	Rx_PWR(0)		0 (32 bit IEEE floating point)
76-77	2	Tx_I(Slope)		1 (unsigned fixed decimal)
78-79	2	Tx_I(Offset)		0 (signed fixed decimal twos complement)
80-81	2	Tx_PWR(Slope)		1 (unsigned fixed decimal)
82-83	2	Tx_PWR(Offset)		0 (signed fixed decimal twos complement)
84-85	2	T (Slope)		1 (unsigned fixed decimal)
86-87	2	T (Offset)		0 (signed fixed decimal twos complement)
88-89	2	V (Slope)		1 (unsigned fixed decimal)
90-91	2	V (Offset)		0 (signed fixed decimal twos complement)
92-94	3	Reserved		Reserved
95	1	Checksum		Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.
A/D VALUES AND STATUS BITS				
96	All	Temperature MSB		Internally measured module temperature.
97	All	Temperature LSB		
98	All	Vcc MSB		Internally measured supply voltage in transceiver.
99	All	Vcc LSB		
100	All	TX Bias MSB		Internally measured TX Bias Current.
101	All	TX Bias LSB		
102	All	TX Power MSB		Measured TX output power.
103	All	TX Power LSB		
104	All	RX Power MSB		Measured RX input power.
105	All	RX Power LSB		
106	All	Reserved MSB		Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB		Reserved for 1st future definition of digitized

				analog input
108	All	Reserved MSB		Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB		Reserved for 2nd future definition of digitized analog input
110	7	TX Disable State		Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin.
110	6	Soft TX Disable		Read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100 msec max from acknowledgement of serial byte transmission. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.
110	5	Reserved		
110	4	RX Rate Select State		Digital state of the SFP RX Rate Select Input Pin. Updated within 100msec of change on pin.
110	3	Soft RX Rate Select		Read/write bit that allows software RX rate select. Writing '1' selects full bandwidth operation. This bit is "OR'd with the hard RX RATE_SELECT pin value. Enable/disable time is 100msec max from acknowledgement of serial byte transmission. Soft RX rate select does not meet the autonegotiation requirements specified in FC-FS. Default at power up is zero. If Soft RX Rate Select is not implemented, the transceiver ignores the value of this bit.
110	2	TX Fault		Digital state of the TX Fault Output Pin. Updated within 100msec of change on pin.
110	1	SD (Signal Detect)		Digital state of the Signal Detect (SD) Pin. Updated within 100msec of change on pin.
110	0	Data_Ready_Bar		Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.
111	7-0	Reserved		Reserved.
ALARM AND WARNING FLAG BITS				
112	7	Temp High Alarm		Set when internal temperature exceeds high alarm level.
112	6	Temp Low Alarm		Set when internal temperature is below low alarm level.
112	5	Vcc High Alarm		Set when internal supply voltage exceeds high alarm level.
112	4	Vcc Low Alarm		Set when internal supply voltage is below low alarm level.
112	3	TX Bias High Alarm		Set when TX Bias current exceeds high alarm level.

112	2	TX Bias Low Alarm		Set when TX Bias current is below low alarm level.
112	1	TX Power High Alarm		Set when TX output power exceeds high alarm level.
112	0	TX Power Low Alarm		Set when TX output power is below low alarm level.
113	7	RX Power High Alarm		Set when Received Power exceeds high alarm level.
113	6	RX Power Low Alarm		Set when Received Power is below low alarm level.
113	5	Reserved Alarm		
113	4	Reserved Alarm		
113	3	Reserved Alarm		
113	2	Reserved Alarm		
113	1	Reserved Alarm		
113	0	Reserved Alarm		
114	All	Reserved		
115	All	Reserved		
116	7	Temp High Warning		Set when internal temperature exceeds high warning level.
116	6	Temp Low Warning		Set when internal temperature is below low warning level.
116	5	Vcc High Warning		Set when internal supply voltage exceeds high warning level.
116	4	Vcc Low Warning		Set when internal supply voltage is below low warning level.
116	3	TX Bias High Warning		Set when TX Bias current exceeds high warning level.
116	2	TX Bias Low Warning		Set when TX Bias current is below low warning level.
116	1	TX Power High Warning		Set when TX output power exceeds high warning level.
116	0	TX Power Low Warning		Set when TX output power is below low warning level.
117	7	RX Power High Warning		Set when Received Power exceeds high warning level.
117	6	RX Power Low Warning		Set when Received Power is below low warning level.
117	5	Reserved Warning		
117	4	Reserved Warning		
117	3	Reserved Warning		
117	2	Reserved Warning		
117	1	Reserved Warning		
117	0	Reserved Warning		
118	All	Reserved		
119	All	Reserved		
VENDOR SPECIFIC MEMORY ADDRESSES				

120-122	All	Reserved		Reserved
123	All	Password Byte 3		High order byte of 32 bit password
124	All	Password Byte 2		Second highest order byte of 32 bit password
125	All	Password Byte 1		Second lowest byte of 32 bit password
126	All	Password Byte 0		Low order byte of 32 bit password
127	All	User EEPROM Select		'1' selects user writable EEPROM at locations 128 - 247

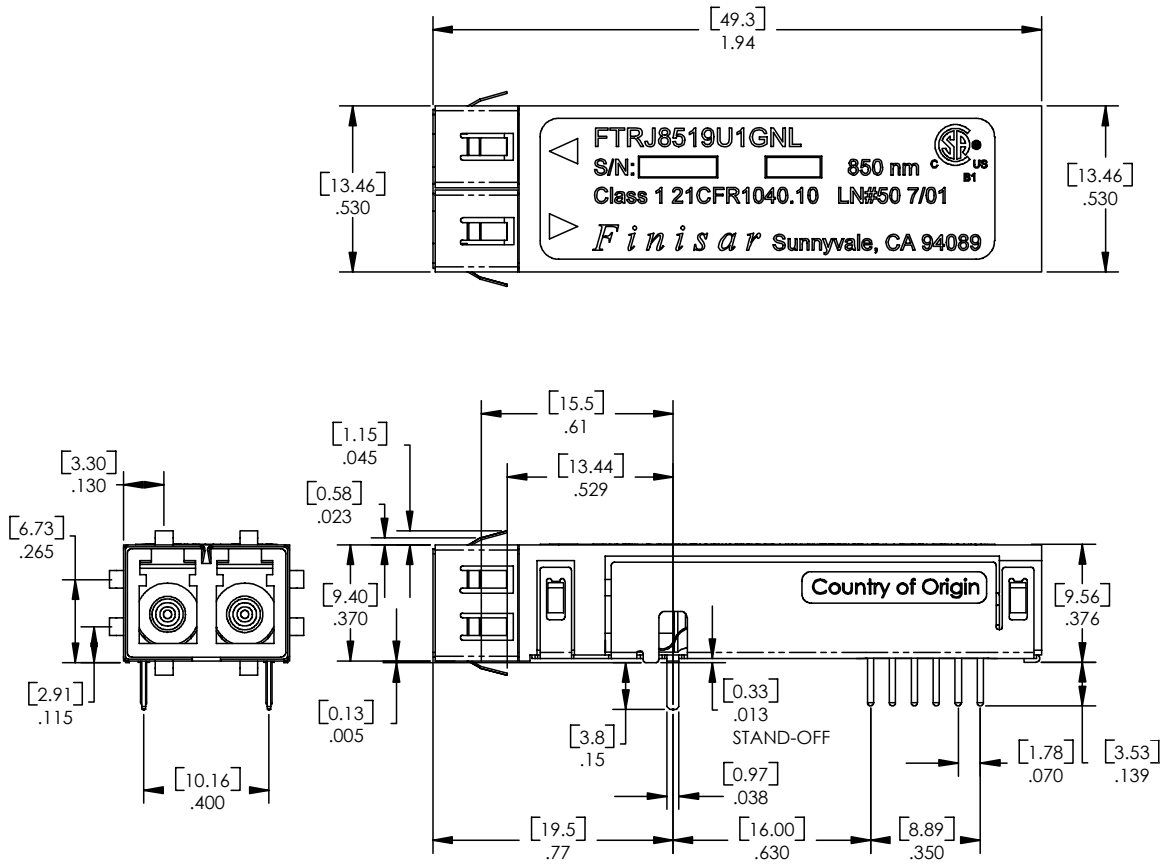
The information below would be contained in bytes 128-246 (54 bytes are free - 45 available for use)

Simplified Serial ID

Byte Address	***Bit Address***	***Size*** *(Bytes) or (bits)*	**Field Name**		***Value***	***Value Meaning***
128-143	NA	16B	Vendor name	SFP vendor name (ASCII) blank padded		
144-146	NA	3B	Vendor OUI	SFP vendor IEEE company ID		IEEE assigned
147-162	NA	16B	Vendor PN	Part number provided by SFP vendor (ASCII)		Finisar part number
163-166	NA	4B	Vendor rev	Revision level for part number provided by vendor (ASCII)		Hardware revision level
167-182	NA	16B	Vendor SN	Serial number provided by vendor (ASCII) blank padded		
183-188	NA	6B	Date code	Vendor's manufacturing date		yymmdd
189-190	NA	2B	Lot Code	Vendor lot code		May be blank
	Diagnostic Monitoring Type					
191	7	1b	Analog Diagnostic			
	6	1b	Digital Diagnostic			
	5	1b	Internally calibrated			
	4	1b	Externally calibrated			
	3	1b	Received power measurement type			
	2	1b	Address mode change required			
	1-0	2b	Reserved			
	Enhanced Options					
192	7	1b	Alarm/Warning			
	6	1b	Soft TX_DISABLE			
	5	1b	Soft TX_FAULT			
	4	1b	Soft RX_LOS			
	3	1b	Soft RATE_SELECT			
	2-0	3b	Reserved			
193	NA	1B	SFF-8472 Compliance			
194-200	NA	7B	Reserved			Reserved for future use
201	NA	1B	Checksum			Byte 201 contains the low order 8 bits of the sum of bytes 128 - 200
202-246	NA	45B	User EEPROM			User-writable/readable EEPROM
247-255	NA	8B	Vendor Specific			Vendor specific control functions

X. Mechanical Specifications

Finisar's Small Form Factor (SFF) transceivers comply with the standard dimensions defined by the Small Form Factor Multi-Sourcing Agreement (MSA).



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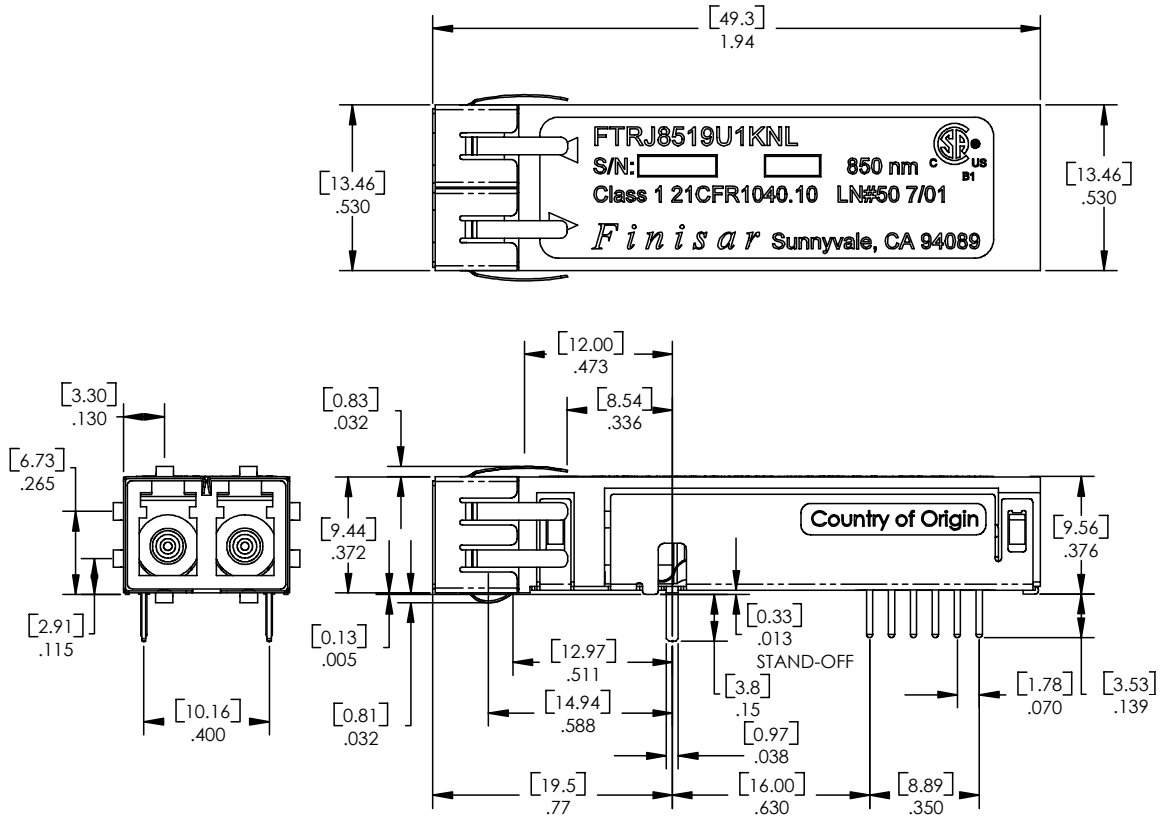

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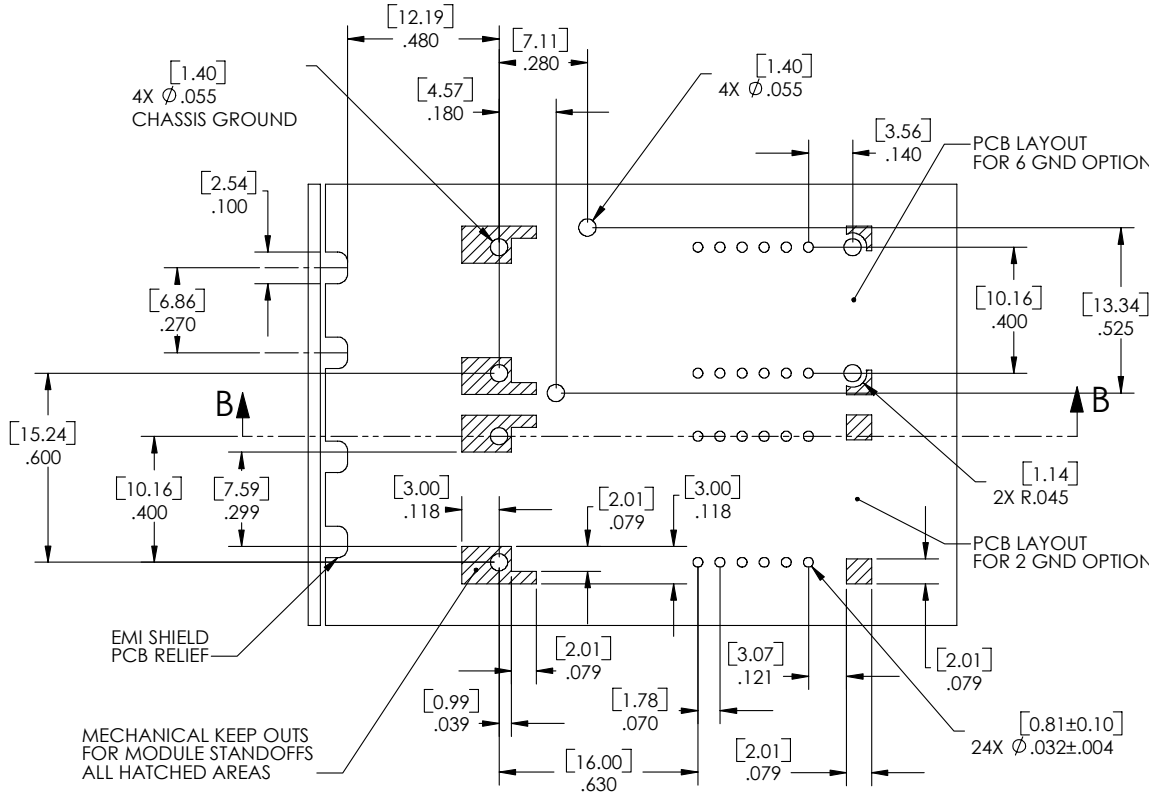
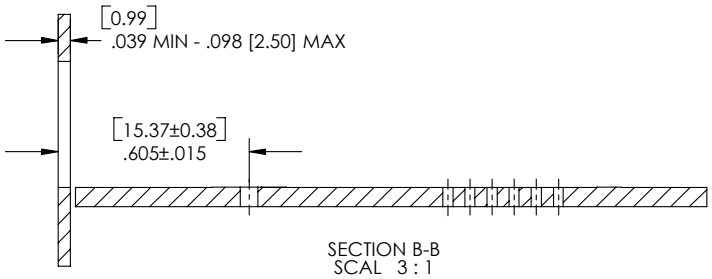
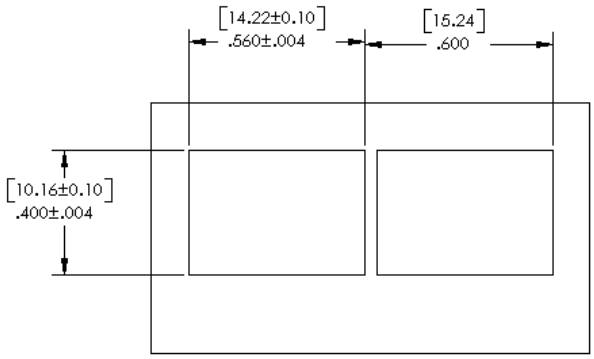
XI. PCB Layout and Bezel Recommendations







Minimum Recommended Pitch is 0.600”

XII. References

1. Small Form Factor (SFF) Transceiver Multi-source Agreement (MSA). January 6, 1998.

2. IEEE 802.3, 2002 Edition, Clause 38, PMD Type 1000BASE-SX. IEEE Standards Department, 2002.

3. "Fibre Channel Physical and Signaling Interface (FC-PH, FC-PH2, FC-PH3)". American National Standard for Information Systems.

4. "Fibre Channel Draft Physical Interface Specification (FC-PI 13.0)". American National Standard for Information Systems.

5. Small Form-factor Pluggable (SFP) Transceiver Multi-source Agreement (MSA), September 14, 2000.

XIII. For More Information

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