



# CMOS 16-BIT LEVEL SHIFTING BUS TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74AUC164245

## FEATURES:

- $V_{DDA}$  AND  $V_{DDB} = 0.8V - 2.7V$
- Inputs/outputs tolerant up to 3.6V
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Supports Hot insertion:
- A and B port output drivers:  $\pm 9mA @ 2.3V$
- Available in TSSOP, TVSOP, and VFBGA packages

## APPLICATIONS:

- High performance, low voltage communications systems
- High performance, low voltage computing systems

## DESCRIPTION:

This 16-bit level shifting bus transceiver is built using advanced CMOS technology. The AUC164245 is ideal for asynchronous communications between data buses. The control function implementation minimizes external timing requirements.

The AUC164245 16-bit level shifting bus transceiver contains two separate supply rails. The B port is designed to track  $V_{DDB}$ , which accepts voltages from 0.8V to 2.7V. The A port and control inputs are designed to track  $V_{DDA}$ , which accepts voltages from 0.8V to 2.7V. This allows for user-selectable translation for various level shifting system environments.

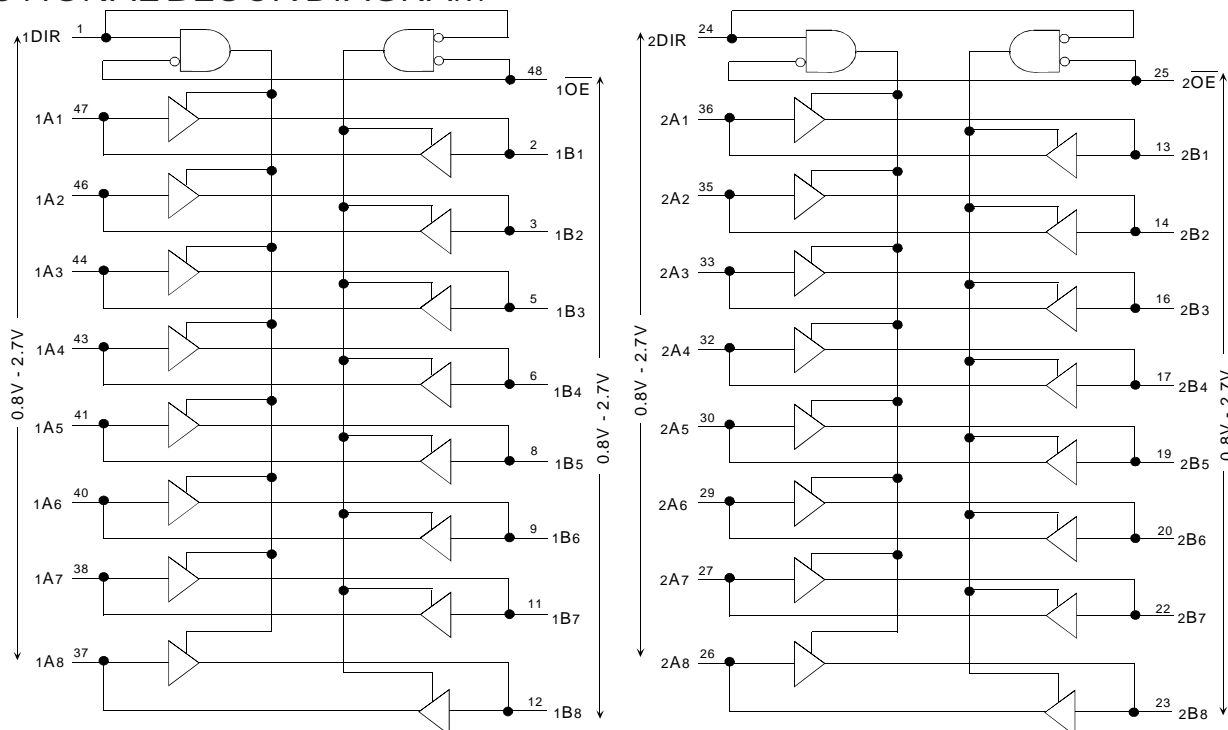
This device can be used as one 16-bit transceiver or two 8-bit transceivers. It allows data transmission from A bus to B bus or from B bus to A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

This device is fully specified for partial power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AUC164245 A and B ports are designed with  $\pm 9mA$  output drivers. These drivers are capable of driving moderate loads while maintaining high speed performance.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{DDA}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2003

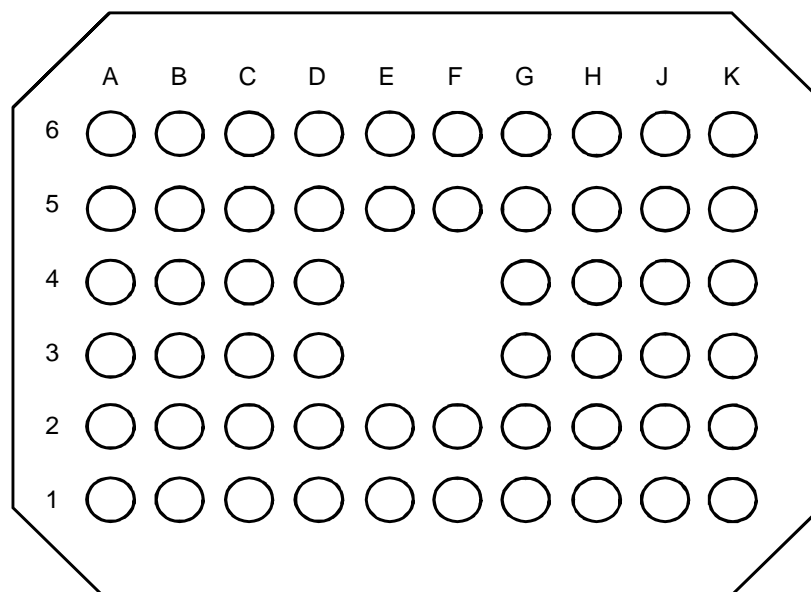
### PINOUT CONFIGURATION

6	$\overline{1OE}$	1A2	1A4	1A6	1A8	2A1	2A3	2A5	2A7	$\overline{2OE}$
5	NC	1A1	1A3	1A5	1A7	2A2	2A4	2A6	2A8	NC
4	NC	GND	VDDA	GND			GND	VDDA	GND	NC
3	NC	GND	Vddb	GND			GND	Vddb	GND	NC
2	NC	1B1	1B3	1B5	1B7	2B2	2B4	2B6	2B8	NC
1	1DIR	1B2	1B4	1B6	1B8	2B1	2B3	2B5	2B7	2DIR
	A	B	C	D	E	F	G	H	J	K

NOTE:  
 NC = No Internal Connection

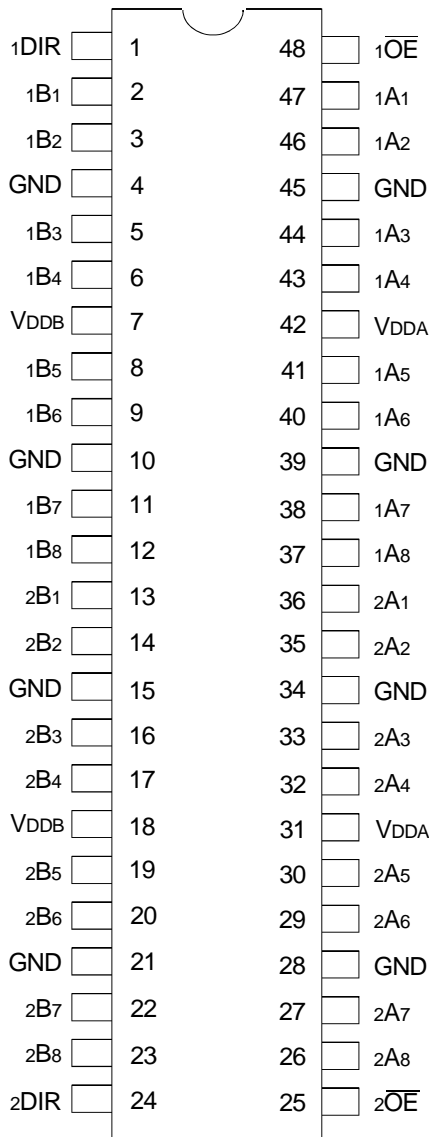
VFBGA

### 56 BALL VFBGA PACKAGE LAYOUT



TOP VIEW

## PIN CONFIGURATION



TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS FOR V<sub>DDA</sub> OR V<sub>DDB</sub>(<sup>1</sup>)

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND (all input and V <sub>DD</sub> terminals)	-0.5 to +3.6	V
V <sub>TERM</sub>	Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state)	-0.5 to +3.6	V
V <sub>TERM</sub>	Terminal Voltage with Respect to GND (any I/O or Output terminals in high or low state)	-0.5 to +3.6	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	Continuous DC Output Current	±20	mA
I <sub>IK</sub>	Continuous Clamp Current	V <sub>i</sub> > V <sub>DD</sub>	+50
		V <sub>i</sub> < 0	-50
I <sub>OK</sub>	Continuous Clamp Current, V <sub>o</sub> < 0	-50	mA
I <sub>DD</sub>	Continuous Current through each V <sub>DD</sub> or GND	±100	mA
I <sub>SS</sub>			

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz, V<sub>DDA</sub> or V<sub>DDB</sub> = 2.5V)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance <sup>(1)</sup>	V <sub>IN</sub> = V <sub>DD</sub> or GND	2.5	4	pF
C <sub>I/O</sub>	I/O Port Capacitance <sup>(2)</sup>	V <sub>I/O</sub> = V <sub>DD</sub> or GND	6	7	pF

### NOTES:

- Applies to the Control Inputs.
- Applies to ports A and B.

## PIN DESCRIPTION

Pin Names	Description
x $\overline{OE}$	3-State Output Enable Control Inputs (Active Low) <sup>(1)</sup>
xDIR	Direction Control Inputs <sup>(1)</sup>
xAX	A Side Inputs or 3-State Outputs <sup>(1)</sup>
xBX	B Side Inputs or 3-State Outputs <sup>(2)</sup>
V <sub>DDA</sub>	Supply for A port, x $\overline{OE}$ , xDIR
V <sub>DDB</sub>	Supply for B port

### NOTES:

- Powered from V<sub>DDA</sub>.
- Powered from V<sub>DDB</sub>.

## FUNCTION TABLE (EACH 8-BIT SECTION)<sup>(1)</sup>

Inputs		Outputs
x $\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

RECOMMENDED OPERATING CHARACTERISTICS<sup>(1)</sup>

Symbol <sup>(2)</sup>	Parameter	Test Conditions <sup>(2)</sup>	Min. <sup>(2)</sup>	Max. <sup>(2)</sup>	Unit
V <sub>DDX</sub>	Supply Voltage		0.8	2.7	V
V <sub>IH</sub> <sup>(3)</sup>	Input HIGH Voltage Level	V <sub>DDX</sub> = 0.8V	V <sub>DDX</sub>	—	V
		V <sub>DDX</sub> = 1.1V to 1.3V	0.65 x V <sub>DDX</sub>	—	
		V <sub>DDX</sub> = 1.4V to 1.6V	0.65 x V <sub>DDX</sub>	—	
		V <sub>DDX</sub> = 1.65V to 1.95V	0.65 x V <sub>DDX</sub>	—	
		V <sub>DDX</sub> = 2.3V to 2.7V	1.7	—	
V <sub>IL</sub> <sup>(3)</sup>	Input LOW Voltage Level	V <sub>DDX</sub> = 0.8V	—	0	V
		V <sub>DDX</sub> = 1.1V to 1.3V	—	0.35 x V <sub>DDX</sub>	
		V <sub>DDX</sub> = 1.4V to 1.6V	—	0.35 x V <sub>DDX</sub>	
		V <sub>DDX</sub> = 1.65V to 1.95V	—	0.35 x V <sub>DDX</sub>	
		V <sub>DDX</sub> = 2.3V to 2.7V	—	0.7	
V <sub>I</sub>	Input Voltage		0	2.7	V
V <sub>O</sub>	Output Voltage	Active State	0	V <sub>DDX</sub>	V
		3-State	0	2.7	
I <sub>OH</sub>	HIGH Level Output Current	V <sub>DDX</sub> = 0.8V	—	-0.7	mA
		V <sub>DDX</sub> = 1.1V	—	-3	
		V <sub>DDX</sub> = 1.4V	—	-5	
		V <sub>DDX</sub> = 1.65V	—	-8	
		V <sub>DDX</sub> = 2.3V	—	-9	
I <sub>OL</sub>	LOW Level Output Current	V <sub>DDX</sub> = 0.8V	—	0.7	mA
		V <sub>DDX</sub> = 1.1V	—	3	
		V <sub>DDX</sub> = 1.4V	—	5	
		V <sub>DDX</sub> = 1.65V	—	8	
		V <sub>DDX</sub> = 2.3V	—	9	
Δt/Δv	Input Transition Rise or Fall Time		—	5	ns/V
T <sub>A</sub>	Operating Free-Air Temperature		-40	+85	°C

NOTES:

1. All unused inputs of the device must be held at V<sub>DD</sub> or GND to ensure proper operation.
2. Where V<sub>DDX</sub> refers to either V<sub>DDA</sub> or V<sub>ddb</sub>, depending on which side output A or B is on.
3. V<sub>IL</sub>, V<sub>IH</sub> limits apply for outputs operating at adjacent voltage ranges. For example, 1.8V V<sub>IL</sub>/V<sub>IH</sub> limits apply for outputs operating at 1.5V or 2.5V.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT OR B PORT)<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions <sup>(2)</sup>	Min. <sup>(2)</sup>	Typ. <sup>(2)</sup>	Max. <sup>(2)</sup>	Unit	
I <sub>IH</sub>	Input HIGH or LOW Current	Data Inputs	V <sub>DDX</sub> = 2.7V, V <sub>I</sub> = V <sub>DDX</sub> or GND	—	—	±10	μA
I <sub>IL</sub>		Control Inputs		—	—	±5	
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>DDX</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 2.7V	—	—	±10	μA	
I <sub>OZH</sub> <sup>(3)</sup>	High Impedance Output Current (3-State Output Pins)	V <sub>DDX</sub> = 2.7V	V <sub>O</sub> = V <sub>DDX</sub>	—	—	±10	μA
I <sub>OZL</sub> <sup>(3)</sup>			V <sub>O</sub> = GND	—	—	±10	
I <sub>DDL</sub>	Quiescent Power Supply Current	V <sub>DDX</sub> = 0.8V to 2.7V V <sub>IN</sub> = GND or V <sub>DDX</sub>	—	—	20	μA	
I <sub>DDH</sub>							
I <sub>DDZ</sub>							

### NOTES:

- All unused inputs of the device must be held at V<sub>DD</sub> or GND to ensure proper operation.
- Where V<sub>DDX</sub> refers to either V<sub>DDA</sub> or V<sub>ddb</sub>, depending on which side output A or B is on.
- For the I/O ports, the parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

## OUTPUT DRIVE CHARACTERISTICS (A PORT OR B PORT)

Symbol	Parameter	Test Conditions <sup>(1,6)</sup>	Min. <sup>(6)</sup>	Typ.	Max. <sup>(6)</sup>	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DDX</sub> = 0.8V - 2.7V	I <sub>OH</sub> = -100μA	V <sub>DDX</sub> - 0.1	—	—	V
		V <sub>DDX</sub> = 0.8V	I <sub>OH</sub> = -0.7mA	—	0.55	—	
		V <sub>DDX</sub> = 1.1V <sup>(2)</sup>	I <sub>OH</sub> = -3mA	0.8	—	—	
		V <sub>DDX</sub> = 1.4V <sup>(3)</sup>	I <sub>OH</sub> = -5mA	1	—	—	
		V <sub>DDX</sub> = 1.65V <sup>(4)</sup>	I <sub>OH</sub> = -8mA	1.2	—	—	
		V <sub>DDX</sub> = 2.3V <sup>(5)</sup>	I <sub>OL</sub> = -9mA	1.8	—	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DDX</sub> = 0.8V - 2.7V	I <sub>OL</sub> = 100μA	—	—	0.2	V
		V <sub>DDX</sub> = 0.8V	I <sub>OL</sub> = 0.7mA	—	0.25	—	
		V <sub>DDX</sub> = 1.1V <sup>(2)</sup>	I <sub>OL</sub> = 3mA	—	—	0.3	
		V <sub>DDX</sub> = 1.4V <sup>(3)</sup>	I <sub>OL</sub> = 5mA	—	—	0.4	
		V <sub>DDX</sub> = 1.65V <sup>(4)</sup>	I <sub>OL</sub> = 8mA	—	—	0.45	
		V <sub>DDX</sub> = 2.3V <sup>(5)</sup>	I <sub>OL</sub> = 9mA	—	—	0.6	

### NOTES:

- V<sub>IL</sub> and V<sub>IH</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate V<sub>DD</sub> range.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .
- Demonstrates operation for nominal V<sub>DDA</sub> or V<sub>ddb</sub> = 1.2V.
- Demonstrates operation for nominal V<sub>DDA</sub> or V<sub>ddb</sub> = 1.5V.
- Demonstrates operation for nominal V<sub>DDA</sub> or V<sub>ddb</sub> = 1.8V.
- Demonstrates operation for nominal V<sub>DDA</sub> or V<sub>ddb</sub> = 2.5V.
- Where V<sub>DDX</sub> refers to either V<sub>DDA</sub> or V<sub>ddb</sub>, depending on which side output A or B is on.

OPERATING CHARACTERISTICS, A TO B,  $V_{DDA}$  AND  $V_{DDB} = 2.5V$ ,  $T_A = 25^\circ C$ 

Symbol	Parameter		Test Conditions	Typ.	Unit
CPDA	Power Dissipation Capacitance	Outputs Enabled	$C_L = 0pF$	3	pF
		Outputs Disabled	$f = 10MHz$	0.4	
CPDB	Power Dissipation Capacitance	Outputs Enabled	$C_L = 0pF$	1.4	pF
		Outputs Disabled	$f = 10MHz$	1.5	

OPERATING CHARACTERISTICS, B TO A,  $V_{DDA}$  AND  $V_{DDB} = 2.5V$ ,  $T_A = 25^\circ C$ 

Symbol	Parameter		Test Conditions	Typ.	Unit
CPDA	Power Dissipation Capacitance	Outputs Enabled	$C_L = 0pF$	14	pF
		Outputs Disabled	$f = 10MHz$	1.5	
CPDB	Power Dissipation Capacitance	Outputs Enabled	$C_L = 0pF$	3	pF
		Outputs Disabled	$f = 10MHz$	0.4	

SWITCHING CHARACTERISTICS,  $V_{DDA} = 0.8^{(1,2)}$ 

Symbol	Parameter	$V_{DDB} = 0.8V$	$V_{DDB} = 1.2V \pm 0.1V$	Unit
		Typ.	Typ.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay <sup>(3)</sup> xAx to xBx	10	5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay <sup>(3)</sup> xBx to xAx	10	11	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(4)</sup> $\overline{xOE}$ to xAx	7.5	7.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(4)</sup> $\overline{xOE}$ to xAx	8.5	8.5	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOE}$ to xBx	10.5	4.8	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOE}$ to xBx	12	6.8	ns

SWITCHING CHARACTERISTICS,  $V_{DDA} = 1.2V \pm 0.1^{(1)}$ 

Symbol	Parameter	$V_{DDB} = 0.8V$	$V_{DDB} = 1.2V \pm 0.1V$		$V_{DDB} = 1.5V \pm 0.1V$		$V_{DDB} = 1.8V \pm 0.15V$			$V_{DDB} = 2.5V \pm 0.2V$		Unit
		Typ.	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay <sup>(3)</sup> xAx to xBx	11	1	4.5	0.5	3.5	0.5	2	3.5	0.5	3	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay <sup>(3)</sup> xBx to xAx	5	1	4.5	0.5	4.5	0.5	3	4.2	0.5	4	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(4)</sup> $\overline{xOE}$ to xAx	3.2	0.7	4.6	0.7	4.6	0.7	3.2	4.6	0.7	4.6	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(4)</sup> $\overline{xOE}$ to xAx	4.6	0.8	6.2	0.8	6.2	0.8	4.6	6.2	0.8	6.2	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOE}$ to xBx	9	0.7	4.6 <sup>(4)</sup>	0.7	3.6	0.7	2.2	3.6	0.7	3.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOE}$ to xBx	9.5	0.8	6.2 <sup>(4)</sup>	0.8	5	0.8	3.5	4.8	0.8	4.3	ns

## NOTES:

- See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
- The temperature range for the 0.8V node is  $0^\circ C$  to  $+85^\circ C$ .
- Propagation delay is symmetrical A-B, depending only on input and output  $V_{DD}$ .
- Enable/Disable to xAx depends on  $V_{DDA}$  only. Times for xBx same if  $V_{DDA} = V_{DDB}$ .

SWITCHING CHARACTERISTICS,  $V_{DDA} = 1.5V \pm 0.1^{(1)}$ 

Symbol	Parameter	$V_{DDB} = 1.2V \pm 0.1V$		$V_{DDB} = 1.5V \pm 0.1V$		$V_{DDB} = 1.8V \pm 0.15V$			$V_{DDB} = 2.5V \pm 0.2V$		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(2)</sup> xAx to xBx	0.5	4.5	0.5	3.3	0.5	2.3	3.1	0.5	2.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(2)</sup> xBx to xAx	0.5	3.5	0.5	3.3	0.5	2	3	0.5	2.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time <sup>(3)</sup> xOE to xAx	0.7	3.3	0.7	3.1	0.7	2.3	3.3	0.7	3.3	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time <sup>(3)</sup> xOE to xAx	0.8	4.5	0.8	4.7	0.8	3	4.5	0.8	4.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xOE to xBx	0.7	4.3	0.7	3.1 <sup>(3)</sup>	0.7	2.3	3.3	0.7	3.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time xOE to xBx	0.8	5.5	0.8	4.7 <sup>(3)</sup>	0.8	3	4.5	0.8	3.7	ns

SWITCHING CHARACTERISTICS,  $V_{DDA} = 1.8V \pm 0.15^{(1)}$ 

Symbol	Parameter	$V_{DDB} = 1.2V \pm 0.1V$		$V_{DDB} = 1.5V \pm 0.1V$		$V_{DDB} = 1.8V \pm 0.15V$			$V_{DDB} = 2.5V \pm 0.2V$		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(2)</sup> xAx to xBx	0.5	4.2	0.5	3	0.5	2	2.8	0.5	2.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(2)</sup> xBx to xAx	0.5	3.5	0.5	3.1	0.5	2	2.8	0.5	2.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time <sup>(3)</sup> xOE to xAx	0.7	3	0.7	3	0.7	2.1	3	0.7	3	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time <sup>(3)</sup> xOE to xAx	0.8	4.3	0.8	4.3	0.8	3.2	4.3	0.8	4.3	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xOE to xBx	0.7	4	0.7	3	0.7	2.1 <sup>(3)</sup>	3 <sup>(3)</sup>	0.7	2.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time xOE to xBx	0.8	5.3	0.8	4.3	0.8	3.2 <sup>(3)</sup>	4.3 <sup>(3)</sup>	0.8	3	ns

SWITCHING CHARACTERISTICS,  $V_{DDA} = 2.5V \pm 0.2^{(1)}$ 

Symbol	Parameter	$V_{DDB} = 1.2V \pm 0.1V$		$V_{DDB} = 1.5V \pm 0.1V$		$V_{DDB} = 1.8V \pm 0.15V$			$V_{DDB} = 2.5V \pm 0.2V$		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(2)</sup> xAx to xBx	0.5	4	0.5	2.8	0.5	1.8	2.6	0.5	2.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(2)</sup> xBx to xAx	0.5	3	0.5	2.6	0.5	1.7	2.5	0.5	2.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time <sup>(3)</sup> xOE to xAx	0.7	2.6	0.7	2.6	0.7	1.8	2.6	0.7	2.6	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time <sup>(3)</sup> xOE to xAx	0.8	2.9	0.8	2.9	0.8	2	2.9	0.8	2.9	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xOE to xBx	0.7	4	0.7	2.8	0.7	2	3.1	0.7	2.6 <sup>(3)</sup>	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time xOE to xBx	0.8	5.3	0.8	4.1	0.8	3	4.3	0.8	2.9 <sup>(3)</sup>	ns

## NOTES:

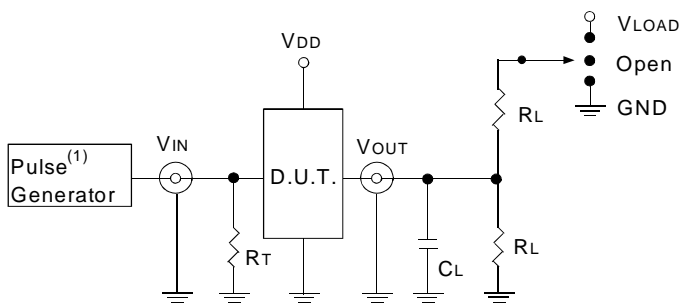
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2. Propagation delay is symmetrical A-B, depending only on input and output  $V_{DD}$ .
3. Enable/Disable to xAx depends on  $V_{DDA}$  only. Times for xBx same if  $V_{DDA} = V_{DDB}$ .

### TEST CIRCUITS AND WAVEFORMS

Symbol	V <sub>DDX</sub> <sup>(1)</sup> = 0.8V	V <sub>DDX</sub> <sup>(1)</sup> = 1.2V±0.1V	V <sub>DDX</sub> <sup>(1)</sup> = 1.5V±0.1V	V <sub>DDX</sub> <sup>(1)</sup> = 1.8V±0.15V	V <sub>DDX</sub> <sup>(1)</sup> = 2.5V±0.2V	Unit
V <sub>LOAD</sub>	2xV <sub>DDX</sub> <sup>(1)</sup>	2xV <sub>DDX</sub> <sup>(1)</sup>	2xV <sub>DDX</sub> <sup>(1)</sup>	2xV <sub>DDX</sub> <sup>(1)</sup>	2xV <sub>DDX</sub> <sup>(1)</sup>	V
V <sub>T</sub>	V <sub>DDX</sub> /2 <sup>(1)</sup>	V <sub>DDX</sub> /2 <sup>(1)</sup>	V <sub>DDX</sub> /2 <sup>(1)</sup>	V <sub>DDX</sub> /2 <sup>(1)</sup>	V <sub>DDX</sub> /2 <sup>(1)</sup>	V
V <sub>LZ</sub>	100	100	100	100	150	mV
V <sub>HZ</sub>	100	100	100	100	150	mV
R <sub>L</sub>	2	2	2	1	0.5	kΩ
C <sub>L</sub>	15	15	15	30	30	pF

**NOTE:**

1. Where V<sub>DDX</sub> refers to either V<sub>DDA</sub> or V<sub>DDB</sub>.



*Test Circuits for All Outputs*

**DEFINITIONS:**

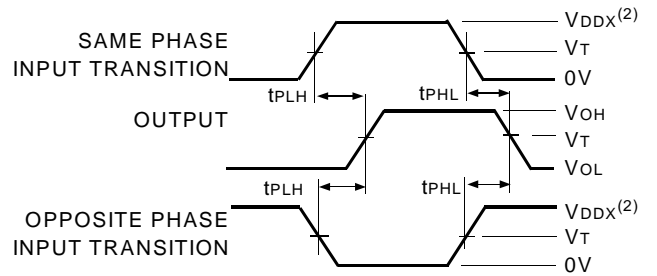
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

**NOTE:**

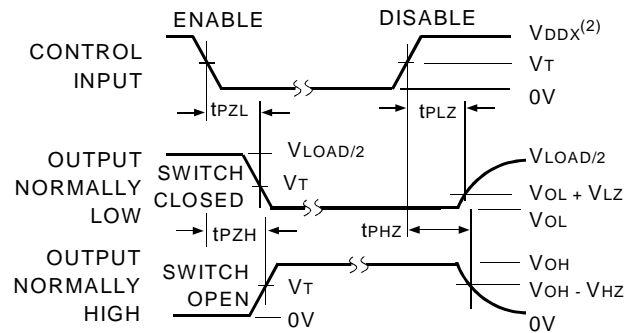
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; Slew Rate ≥ 1V/ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open



*Propagation Delay*



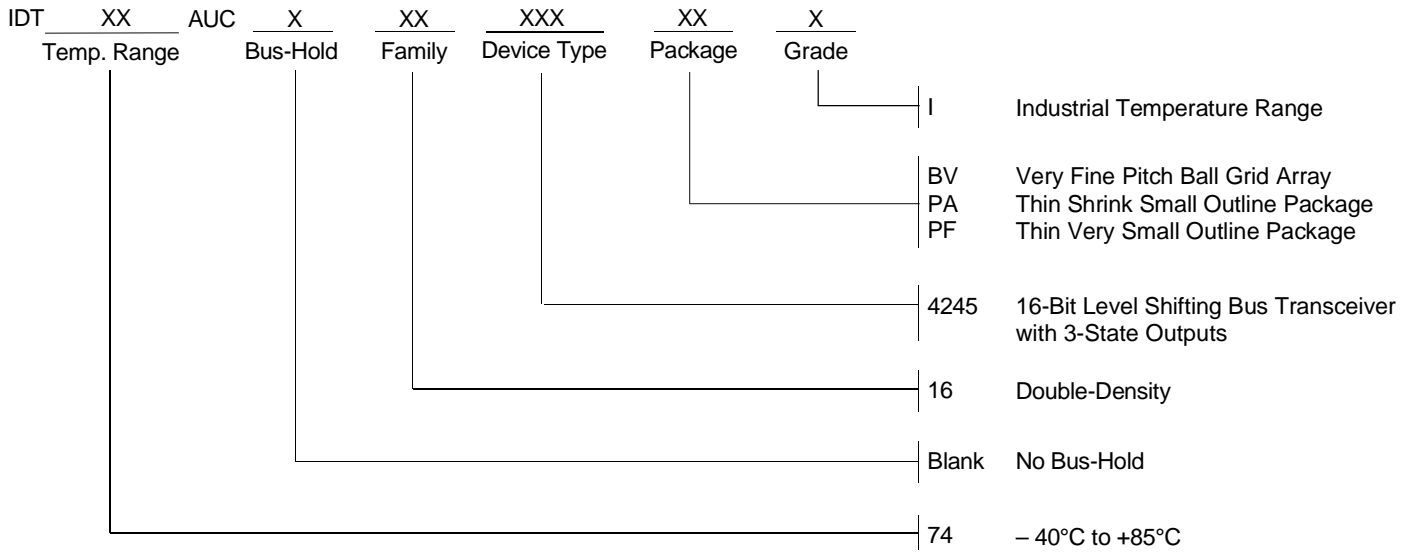
**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Where V<sub>DDX</sub> refers to either V<sub>DDA</sub> or V<sub>DDB</sub>

*Enable and Disable Times*



ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
 www.idt.com

**for Tech Support:**  
 logichelp@idt.com  
 (408) 654-6459