

# Dual J-K negative edge-triggered flip-flop with common clock and reset

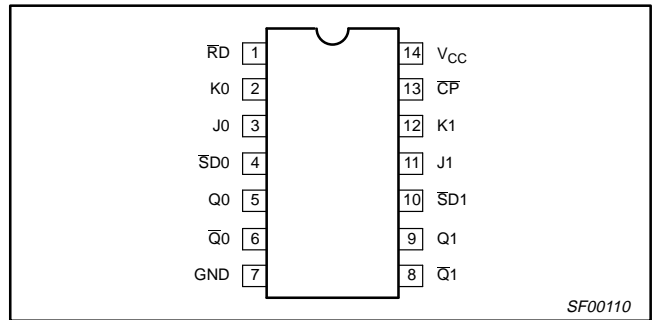
74F114

## DESCRIPTION

The 74F114, Dual Negative edge-triggered JK-Type Flip-Flop with common clock and reset inputs, features individual J, K, Clock ( $\overline{CP}$ ), Set ( $\overline{SD}$ ) and Reset ( $\overline{RD}$ ) inputs, true and complementary outputs. The  $\overline{SD}$  and  $\overline{RD}$  inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ( $\overline{CP}$ ) input enables the J and K inputs and data will be accepted. The logic levels and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the  $\overline{CP}$  is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the  $\overline{CP}$ .

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F114	100MHz	15mA

## ORDERING INFORMATION

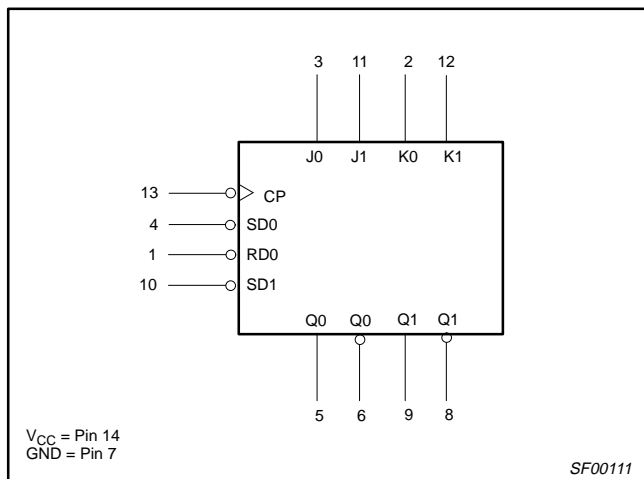
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG. DWG. #
14-pin plastic DIP	N74F114N	SOT27-1
14-pin plastic SO	N74F114D	SOT108-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

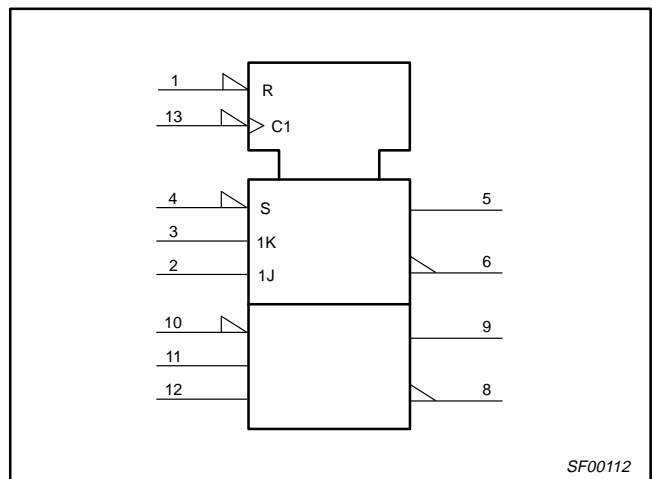
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20 $\mu$ A/0.6mA
K0, K1	K inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{SD}$ 0, $\overline{SD}$ 1	Set inputs (active Low)	1.0/5.0	20 $\mu$ A/3.0mA
$\overline{RD}$	Reset input (active Low)	1.0/10.0	20 $\mu$ A/6.0mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/8.0	20 $\mu$ A/4.8mA
Q0, $\overline{Q}$ 0; Q1, $\overline{Q}$ 1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



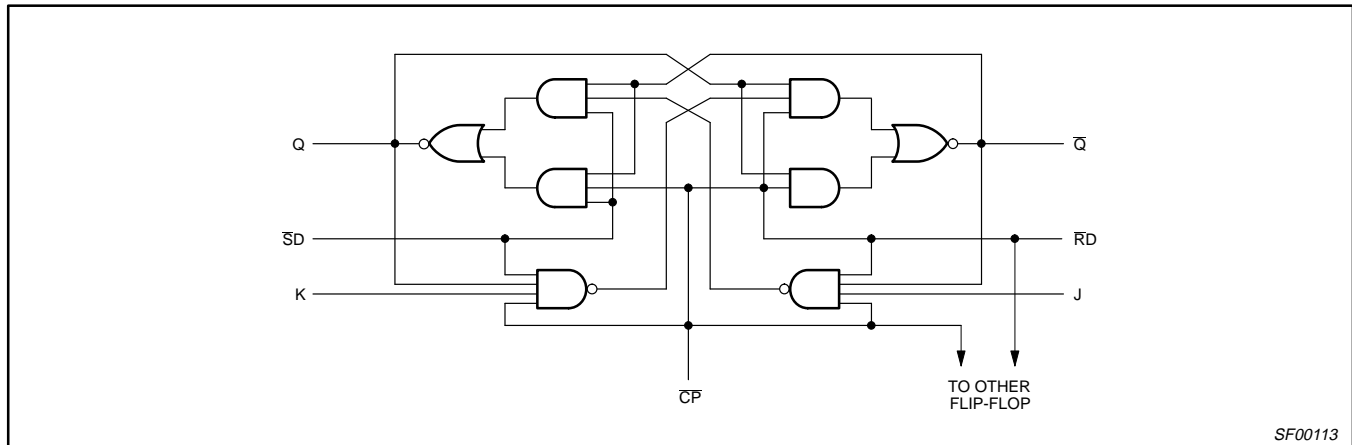
## IEC/IEEE SYMBOL



# Dual J-K negative edge-triggered flip-flop with common clock and reset

74F114

## LOGIC DIAGRAM



SF00113

## FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
S $\bar{D}$	R $\bar{D}$	C $\bar{P}$	J	K	Q	Q $\bar{}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	l	q $\bar{}$	q	Toggle
H	H	↓	l	h	L	H	Load "0" (Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	q $\bar{}$	Hold "no change"

H = High voltage level

h = High voltage level one setup time prior to High-to-Low clock transition

L = Low voltage level

l = Low voltage level one setup time prior to High-to-Low clock transition

q = Lower case letters indicate the state of the reference output prior to the High-to-Low clock transition

X = Don't care

↓ = High-to-Low clock transition

Asynchronous inputs: Low input to S $\bar{D}$  sets Q to High level, Low input to R $\bar{D}$  sets Q to Low level

Set and Reset are independent of clock

Simultaneous Low on both S $\bar{D}$  and R $\bar{D}$  makes both Q and Q $\bar{}$  High.

\* = Both outputs will be High while both S $\bar{D}$  and R $\bar{D}$  are Low, but the output states are unpredictable if S $\bar{D}$  and R $\bar{D}$  go High simultaneously.

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

# Dual J-K negative edge-triggered flip-flop with common clock and reset

74F114

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
			MIN	TYP <sup>2</sup>	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.4	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.35	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current	Jn, Kn	$V_{CC} = \text{MAX}, V_I = 0.5V$		-0.6	mA
		$\overline{CP}$			-4.8	mA
		$\overline{SDn}$			-3.0	mA
		$\overline{RD}$			-6.0	mA
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$		-60	-150	mA
$I_{CC}$	Supply current (total) <sup>4</sup>	$V_{CC} = \text{MAX}$		15	21	mA

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5V, T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.
- Measure  $I_{CC}$  with the clock input grounded and all outputs open, with the Q and  $\overline{Q}$  outputs High in turn.

# Dual J-K negative edge-triggered flip-flop with common clock and reset

74F114

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	85	100		80		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn or Qn	Waveform 1	2.0 2.0	5.0 5.5	6.5 7.5	2.0 2.0	7.5 8.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SDn, RD to Qn or Qn	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

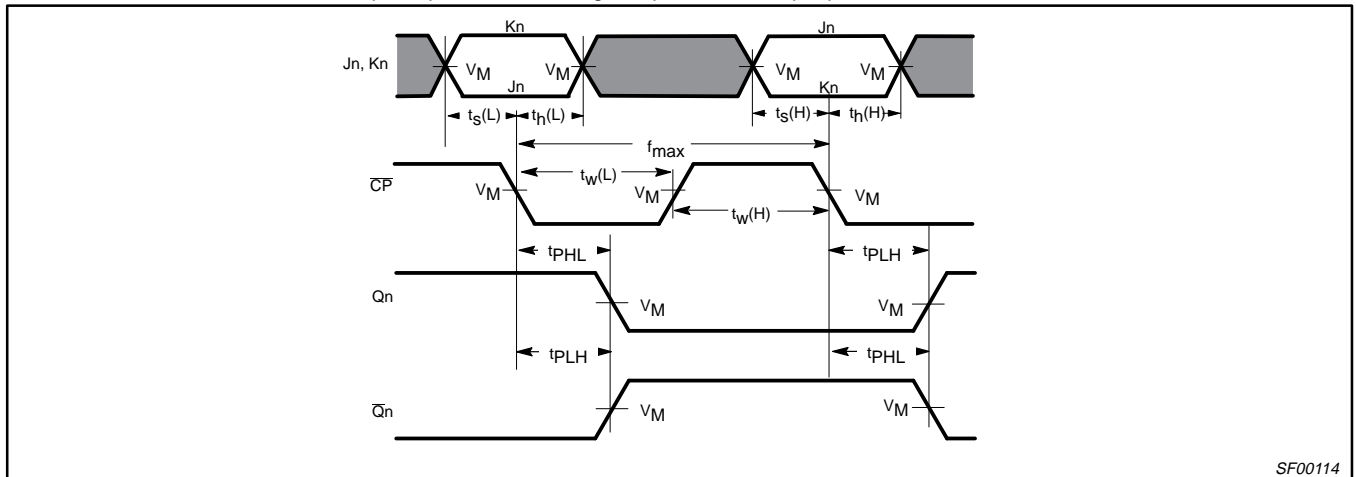
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>S(H)</sub> t <sub>S(L)</sub>	Setup time, High or Low Jn, Kn to CP	Waveform 1	4.0 3.5			5.0 4.0		ns
t <sub>H(H)</sub> t <sub>H(L)</sub>	Hold time, High or Low Jn, Kn to CP	Waveform 1	0.0 0.0			0.0 0.0		ns
t <sub>W(H)</sub> t <sub>W(L)</sub>	CP Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		ns
t <sub>W(L)</sub>	SDn, RD Pulse width Low	Waveform 2,3	4.5			5.0		ns
t <sub>REC</sub>	Recovery time SDn, RD to CP	Waveform 2,3	4.5			5.0		ns

## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

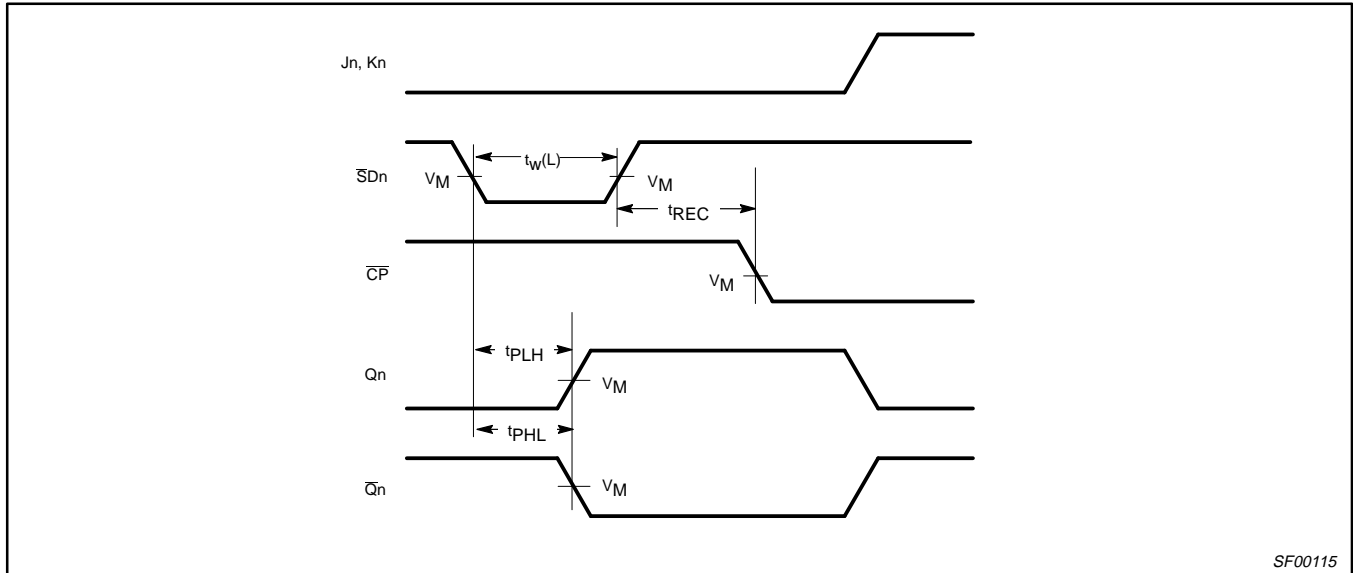


SF00114

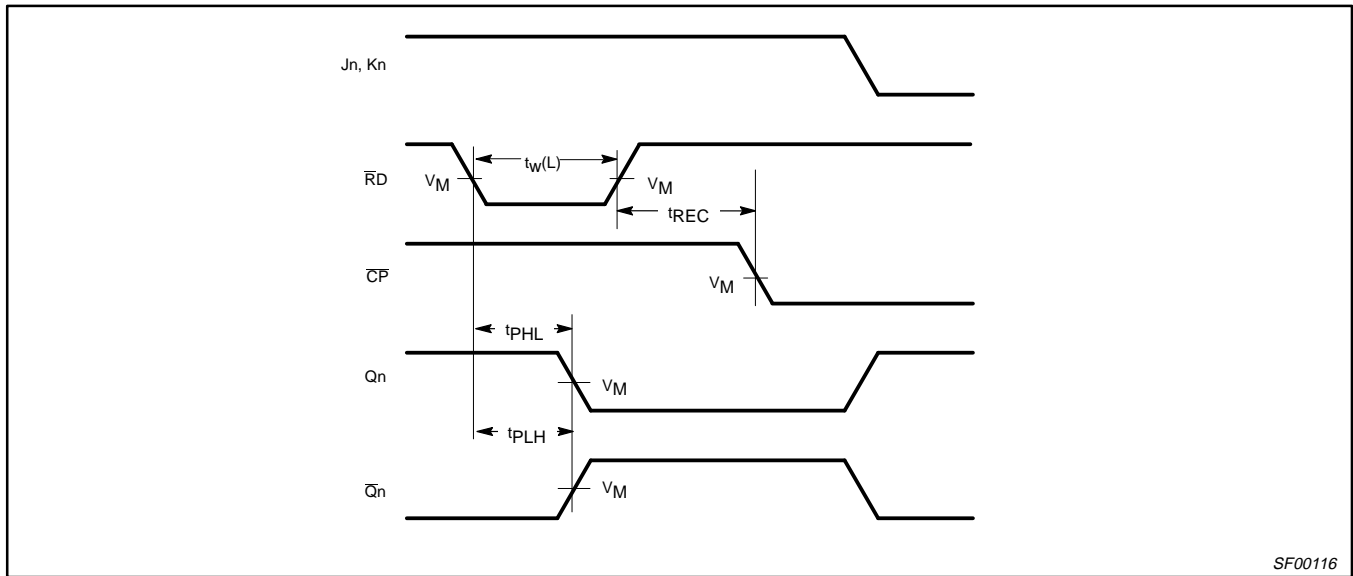
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Pulse Width

# Dual J-K negative edge-triggered flip-flop with common clock and reset

74F114



Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

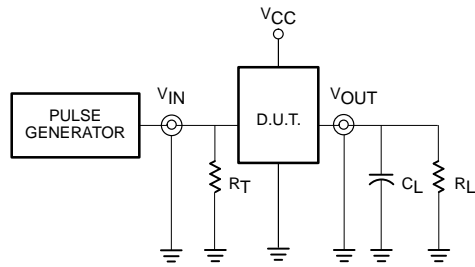


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

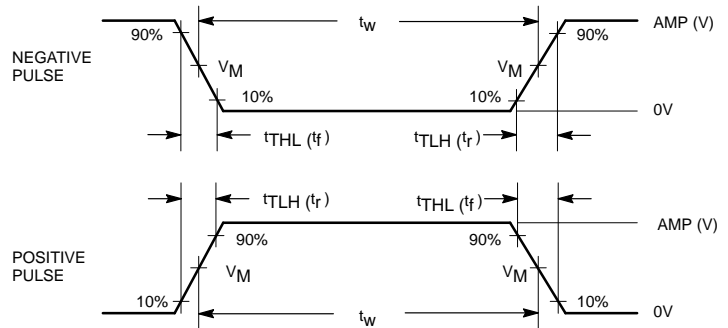
# Dual J-K negative edge-triggered flip-flop with common clock and reset

74F114

## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006