LH538000-S

CMOS 8M (1M × 8/512K × 16)
3 V-Drive Mask-Programmable ROM

FEATURES

- Low power supply:
  2.6 to 5.5 V
- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- Access time:
  500 ns (MAX.) at 2.6 V ≤ V_{CC} < 4.5 V
  200 ns (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Static operation
- Three-state output
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  64-pin, 14 × 20 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH538000-S is a CMOS 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

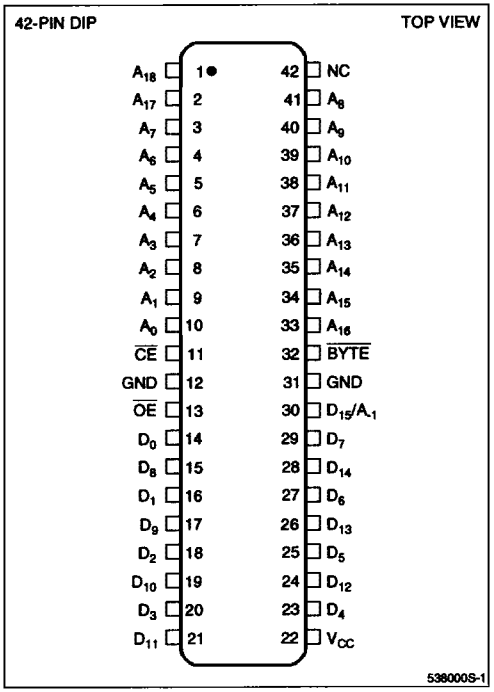

Figure 1. Pin Connections for DIP Package

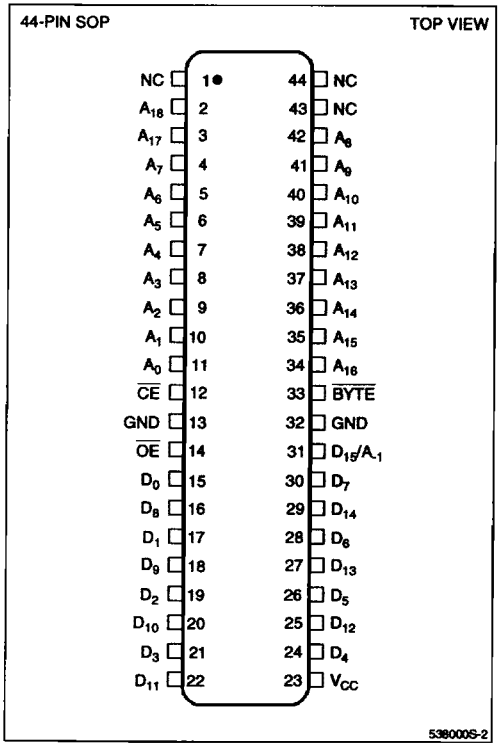

Figure 2. Pin Connections for SOP Package

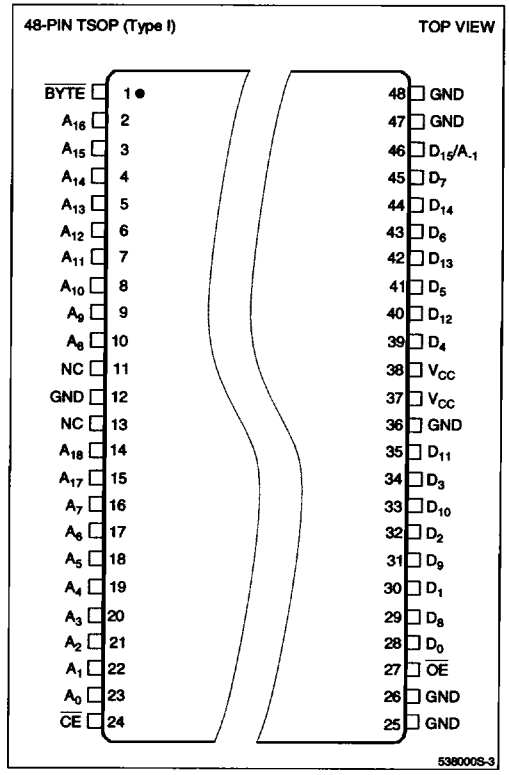

Figure 3. Pin Connections for TSOP Package

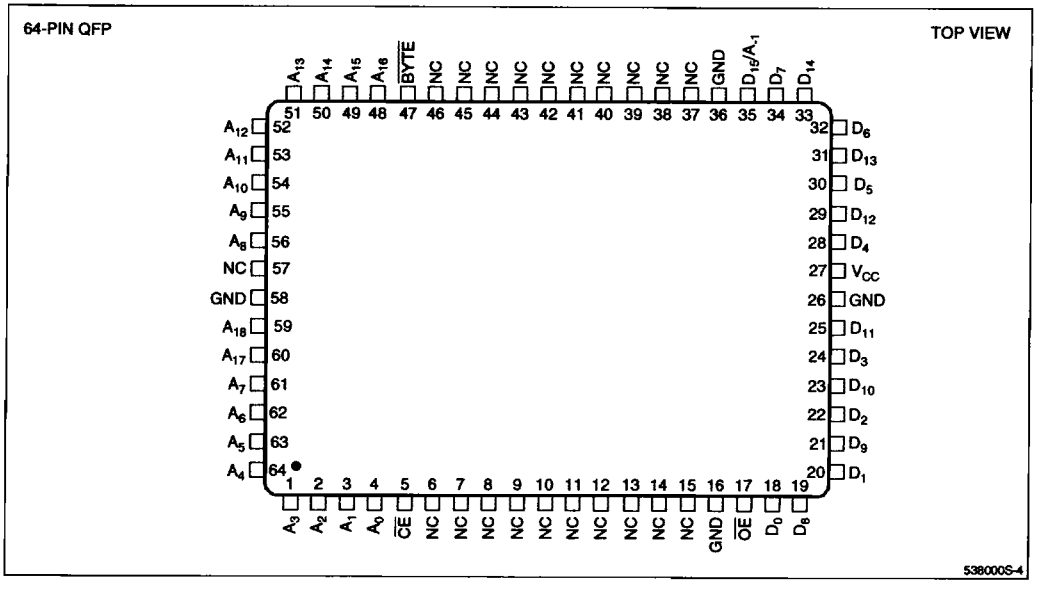

Figure 4. Pin Connections for QFP Package

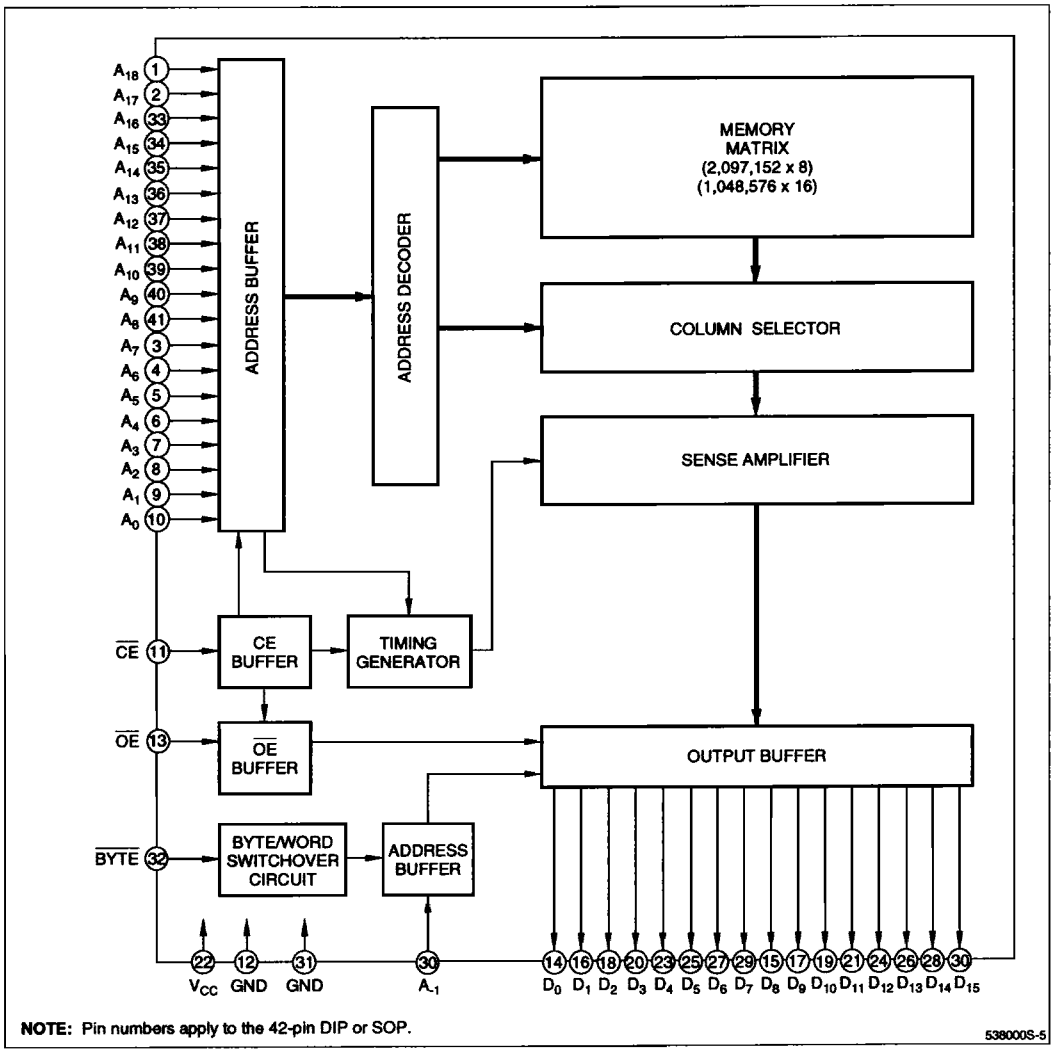

Figure 5. LH538000-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{18}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	Byte/Word switch
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output enable input
V_{CC}	Power supply
GND	Ground

NOTE:
The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. The $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		MODE	ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}		LSB	MSB	
H	X	X	X	High-Z	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z		–	–	Operating (I_{CC})
L	L	H	Inhibit	D_0 - D_7	D_8 - D_{15}	16-bit	A_0	A_{18}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	8-bit	A_{-1}	A_{18}	Operating (I_{CC})
L	L	L	H	D_8 - D_{15}	High-Z	8-bit	A_{-1}	A_{18}	Operating (I_{CC})

NOTE:
X = Don't care, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to + 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		0.8V_{CC}	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	0.8V_{CC}		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA		0.4	V	
Input leakage current	$\|I_{LI}\|$	V_{IN}= 0 V to V_{CC}		10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40	mA	2
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35	mA	3
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = +25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}, V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V), 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	2.6 ≤ V_{CC} < 4.5		4.5 ≤ V_{CC} ≤ 5.5		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		200		ns	
Address access time	t_{AA}		500		200	ns	
Chip enable time	t_{ACE}		500		200	ns	
Output enable time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		5		ns	
CE to output in High-Z	t_{CHZ}		150		70	ns	1
OE to output in High-Z	t_{OHZ}		150		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

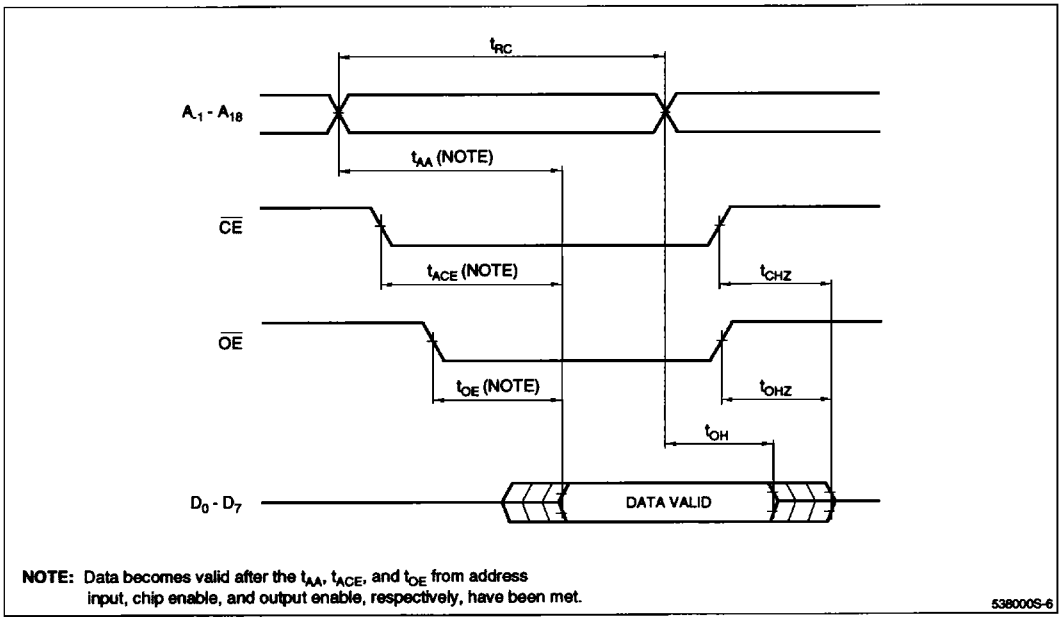

Figure 6. Byte Mode ($\overline{BYTE}$ = V_{IL})

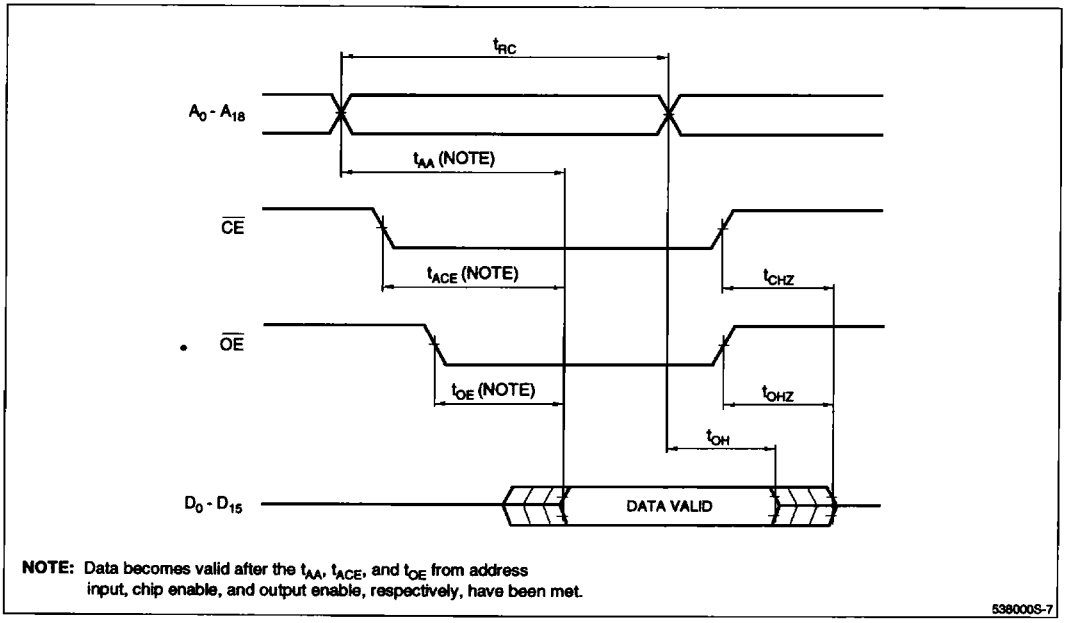

Figure 7. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION