

MSM51V18160B/BSL

1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V18160B/BSL is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V18160B/BSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V18160B/BSL is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP. The MSM51V18160BSL (the self-refresh version) is specially designed for lower-power applications.

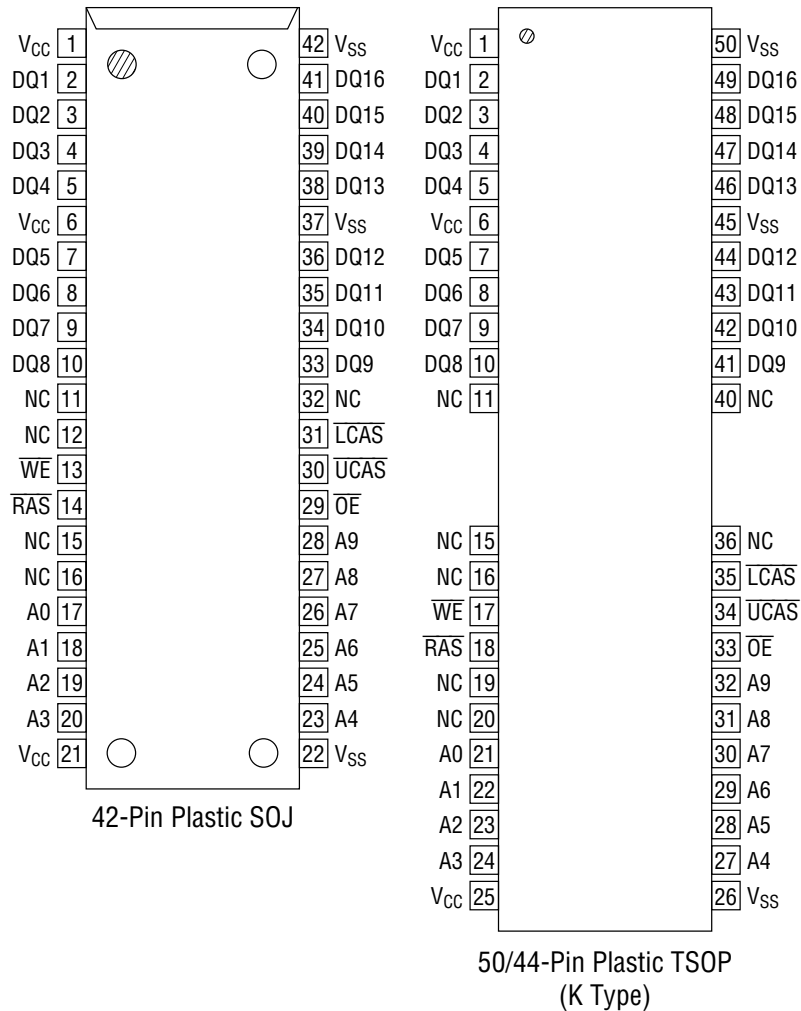
FEATURES

- 1,048,576-word × 16-bit configuration
 - Single 3.3 V power supply, ±0.3 V tolerance
 - Input : LVTTTL compatible, low input capacitance
 - Output : LVTTTL compatible, 3-state
 - Refresh : 1024 cycles/16 ms, 1024 cycles/128 ms (SL version)
 - Fast page mode, read modify write capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
 - Package options:
 - 42-pin 400 mil plastic SOJ (SOJ42-P-400-1.27) (Product : MSM51V18160B/BSL-xxJS)
 - 50/44-pin 400 mil plastic TSOP (TSOPII50/44-P-400-0.80-K) (Product : MSM51V18160B/BSL-xxTS-K)
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM51V18160B/BSL-50	50 ns	25 ns	13 ns	13 ns	90 ns	684 mW	1.8 mW/ 0.72 mW (SL version)
MSM51V18160B/BSL-60	60 ns	30 ns	15 ns	15 ns	110 ns	576 mW	
MSM51V18160B/BSL-70	70 ns	35 ns	20 ns	20 ns	130 ns	504 mW	

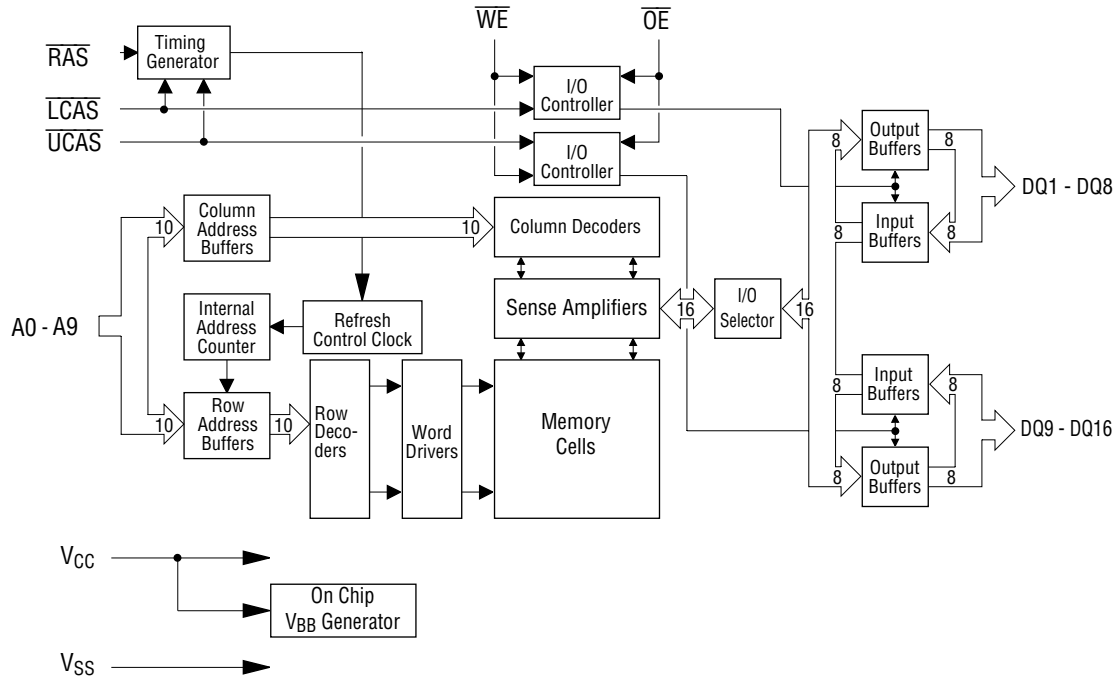
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A9	Address Input
\overline{RAS}	Row Address Strobe
\overline{LCAS}	Lower Byte Column Address Strobe
\overline{UCAS}	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V _{CC}	Power Supply (3.3 V)
V _{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D _{OUT}	Upper Byte Read
L	L	L	H	L	D _{OUT}	D _{OUT}	Word Read
L	L	H	L	H	D _{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-0.5 to 4.6	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

Capacitance(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C _{IN1}	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	C _{I/O}	—	7	pF

DC Characteristics

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V18160 B/BSL-50		MSM51V18160 B/BSL-60		MSM51V18160 B/BSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V _{OH}	I _{OH} = -2.0 mA	2.4	V _{CC}	2.4		
Output Low Voltage	V _{OL}	I _{OL} = 2.0 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0 V ≤ V _I ≤ V _{CC} + 0.3 V; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0 V ≤ V _O ≤ V _{CC}	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	190	—	160	—	140	mA	1, 2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V _{CC} - 0.2 V	—	0.5	—	0.5	—	0.5	μA	1, 5
			—	200	—	200	—	200	μA	
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, t _{RC} = Min.	—	190	—	160	—	140	mA	1, 2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	190	—	160	—	140	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, t _{PC} = Min.	—	120	—	100	—	90	mA	1, 3
Average Power Supply Current (Battery Backup)	I _{CC10}	t _{RC} = 125 μs, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, t _{RAS} ≤ 1 μs	—	300	—	300	—	300	μA	1, 4, 5
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	I _{CC8}	$\overline{\text{RAS}} \leq 0.2 \text{ V}$, $\overline{\text{CAS}} \leq 0.2 \text{ V}$	—	300	—	300	—	300	μA	1, 5

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. The address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
 4. V_{CC} - 0.2 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, -0.3 V ≤ V_{IL} ≤ 0.2 V.
 5. SL version.

AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51V18160 B/BSL-50		MSM51V18160 B/BSL-60		MSM51V18160 B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t _{RWC}	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t _{PC}	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	76	—	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4, 12
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	13	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	—	16	ms	
Refresh Period (SL version)	t _{REF}	—	128	—	128	—	128	ms	15
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	13	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	7	—	10	—	10	—	ns	14
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	13	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	—	35	—	40	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	17	37	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	12	25	15	30	15	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	11
Column Address Hold Time	t _{CAH}	7	—	10	—	15	—	ns	11
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	11
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	8, 11
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51V18160B/BSL-50		MSM51V18160B/BSL-60		MSM51V18160B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Write Command Set-up Time	t _{WCS}	0	—	0	—		
Write Command Hold Time	t _{WCH}	7	—	10	—	15	—	ns	11
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
\overline{OE} Command Hold Time	t _{OEH}	13	—	15	—	20	—	ns	
Write Command to \overline{RAS} Lead Time	t _{RWL}	13	—	15	—	20	—	ns	
Write Command to \overline{CAS} Lead Time	t _{CWL}	13	—	15	—	20	—	ns	13
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	10, 11
Data-in Hold Time	t _{DH}	7	—	10	—	15	—	ns	10, 11
\overline{OE} to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
\overline{CAS} to \overline{WE} Delay Time	t _{CWD}	36	—	40	—	50	—	ns	9
Column Address to \overline{WE} Delay Time	t _{AWD}	48	—	55	—	65	—	ns	9
\overline{RAS} to \overline{WE} Delay Time	t _{RWD}	73	—	85	—	100	—	ns	9
\overline{CAS} Precharge \overline{WE} Delay Time	t _{CPWD}	53	—	60	—	70	—	ns	9
\overline{CAS} Active Delay Time from \overline{RAS} Precharge	t _{RPC}	5	—	5	—	5	—	ns	11
\overline{RAS} to \overline{CAS} Set-up Time (\overline{CAS} before \overline{RAS})	t _{CSR}	10	—	10	—	10	—	ns	11
\overline{RAS} to \overline{CAS} Hold Time (\overline{CAS} before \overline{RAS})	t _{CHR}	10	—	10	—	10	—	ns	12
\overline{RAS} Pulse Width (\overline{CAS} before \overline{RAS} Self-Refresh)	t _{RASS}	100	—	100	—	100	—	μs	15
\overline{RAS} Precharge Time (\overline{CAS} before \overline{RAS} Self-Refresh)	t _{RPS}	90	—	110	—	130	—	ns	15
\overline{CAS} Hold Time (\overline{CAS} before \overline{RAS} Self-Refresh)	t _{CHS}	-50	—	-50	—	-50	—	ns	15

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles (RAS-only refresh or CAS before RAS refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. The output timing reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the \overline{UCAS} and \overline{LCAS} , leading edges in an early write cycle, and to the \overline{WE} leading edge in an \overline{OE} control write cycle, or a read modify write cycle.
 11. These parameters are determined by the falling edge of either \overline{UCAS} or \overline{LCAS} , whichever is earlier.
 12. These parameters are determined by the rising edge of either \overline{UCAS} or \overline{LCAS} , whichever is later.
 13. t_{CWL} should be satisfied by both \overline{UCAS} and \overline{LCAS} .
 14. t_{CP} is determined by the time both \overline{UCAS} and \overline{LCAS} are high.
 15. Only SL version.

See ADDENDUM P for AC Timing Waveforms