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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HCT137

3-to-8-line Decoder/Demultiplexer with Address Latch

ADE-205-546 (Z)
1st. Edition
Sep. 2000

Description

The HD74HCT137 implements a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G_1 and $\overline{G_2}$, control the state of the outputs independently of the select or latch-enable inputs.

All of the outputs are high unless G_1 is high and $\overline{G_2}$ is low. The HD74HCT137 is ideally suited for the implementation of glitchfree decoders in stored-address applications in bus oriented systems.

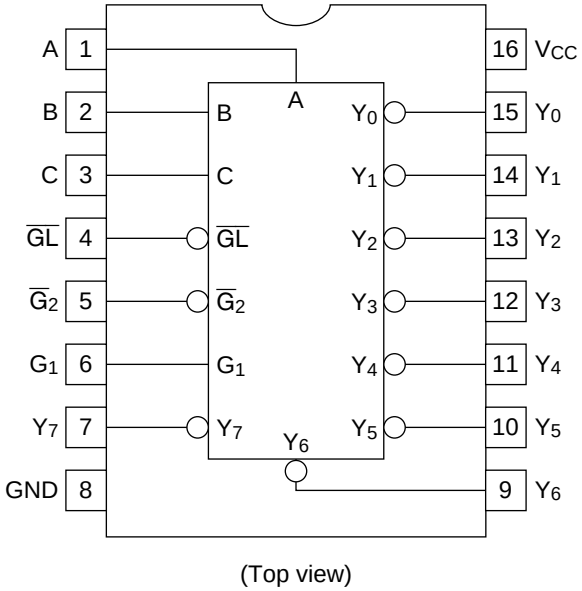
Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (A, B, C to Y) = 18 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 4.5 to 5.5 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max (Ta = 25°C)

Function Table

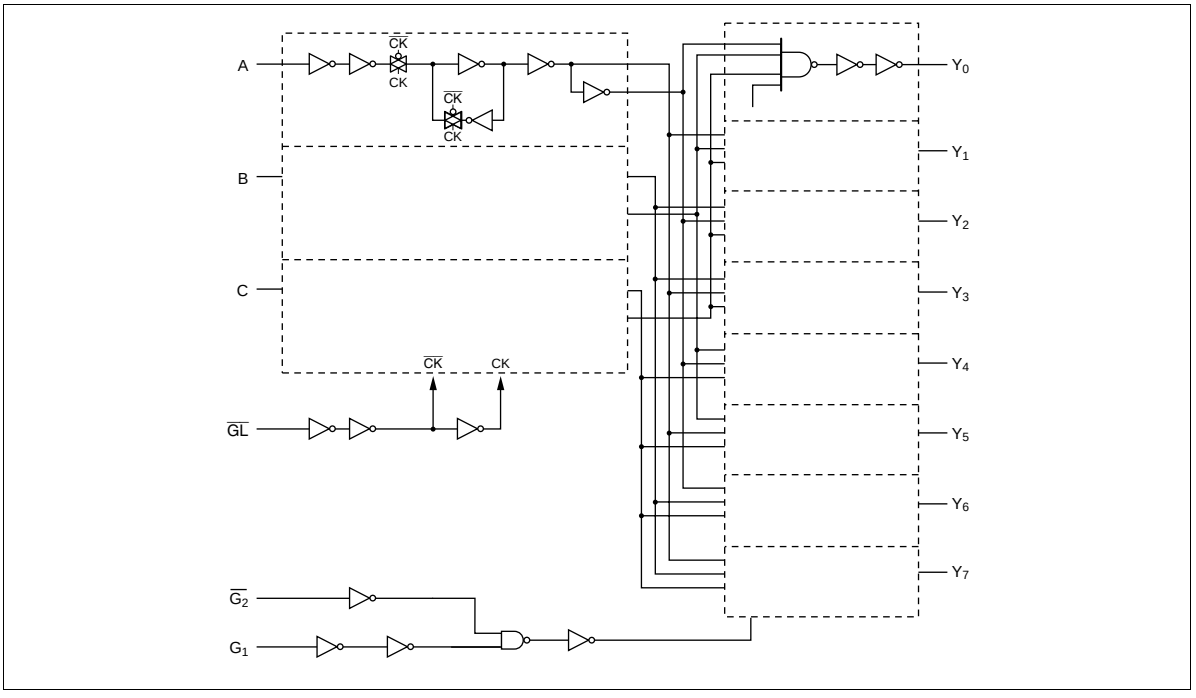
Inputs													
Enable			Select			Outputs							
$\overline{GL}$	G_1	$\overline{G_2}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output Corresponding to stored address L; all others H							

Pin Arrangement



(Top view)

Logic Diagram



DC Characteristics

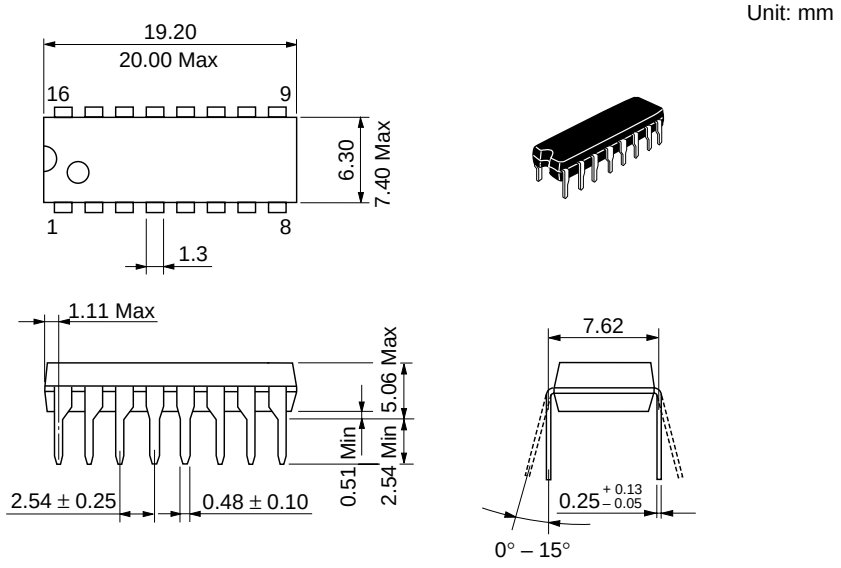
Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions V_{CC} (V)	
Input voltage	V_{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5	
	V_{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5	
Output voltage	V_{OH}	4.4	—	—	4.4	—	V	4.5	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.18	—	—	4.13	—		4.5	I_{OH} = –4 mA
	V_{OL}	—	—	0.1	—	0.1	V	4.5	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		—	—	0.26	—	0.33		4.5	I_{OL} = 4 mA
Input current	Iin	—	—	±0.1	—	±1.0	µA	5.5	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	—	—	4.0	—	40	µA	5.5	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

		Ta = 25°C			Ta = –40 to +85°C			Test Conditions	
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**V_{CC} (V)**	
Propagation delay time	t_{PLH}	—	14	34	—	43	ns	4.5	A, B or C to Y
	t_{PHL}	—	22	48	—	60		4.5	
	t_{PLH}	—	11	26	—	33	ns	4.5	$\overline{G}_2$ to Y
	t_{PHL}	—	23	39	—	49		4.5	
	t_{PLH}	—	13	30	—	38	ns	4.5	G_1 to Y
	t_{PHL}	—	17	39	—	49		4.5	
	t_{PLH}	—	16	35	—	44	ns	4.5	$\overline{GL}$ to Y
	t_{PHL}	—	23	50	—	63		4.5	
Pulse width	t_w	16	6	—	20	—	ns	4.5	
Setup time	t_{su}	20	3	—	25	—	ns	4.5	
Hold time	t_h	10	0	—	13	—	ns	4.5	
Output rise/fall time	t_{TLH} t_{THL}	—	5	15	—	19	ns	4.5	
Input capacitance	Cin	—	5	10	—	10	pF	—	

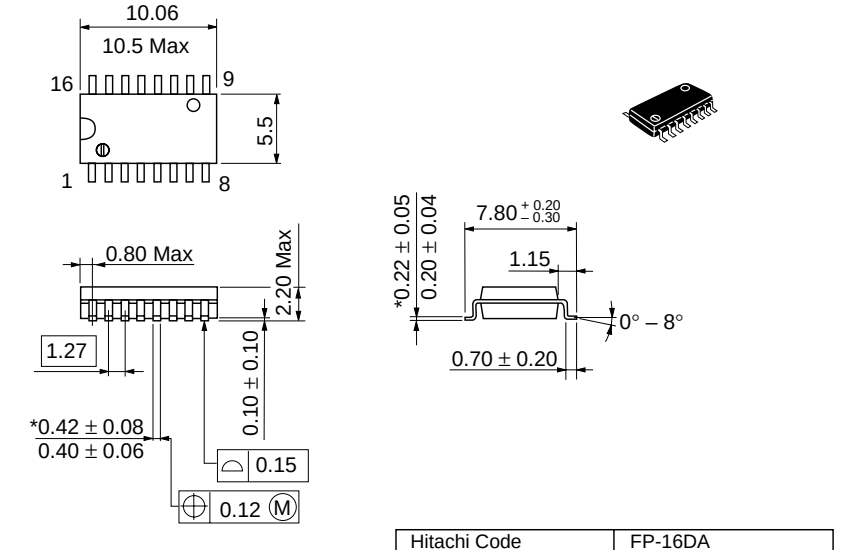
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

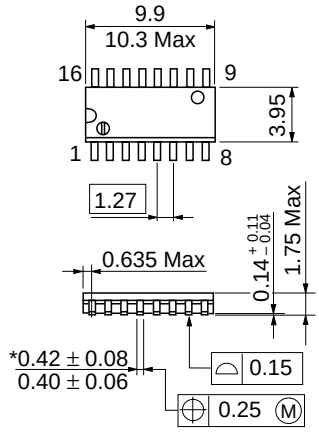
Unit: mm

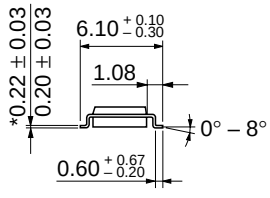


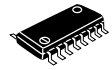
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http://semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straβe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://www.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : http://www.hitachi.com.hk

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