National Semiconductor

ADVANCE INFORMATION

74LVT125
3.3V ABT Quad Buffer with TRI-STATE® Outputs

General Description

The LVT125 contains four independent non-inverting buffers with TRI-STATE outputs.

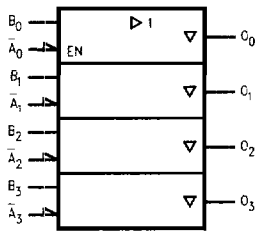
These buffers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/ + 64 mA
- Available in SOIC JEDEC, SOIC EIAJ, and TSSOP
- Functionally compatible with the 74 series 125

Logic Symbol

IEEE/IEC



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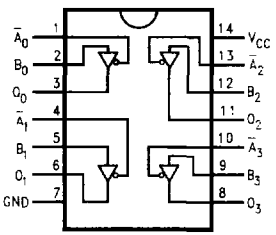
Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12011–2

Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	TRI-STATE Outputs

Truth Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVT125M 74LVT125MX	74LVT125SJ 74LVT125SJX	74LVT125MTC 74LVT125MTCX
See NS Package Number	M14A	M14D	MTC14

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