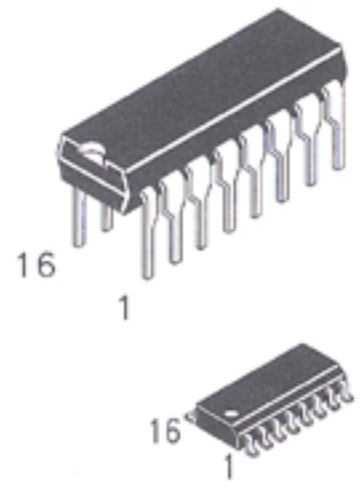
AVG *Semiconductors* DDi™

Technical Data

4-Bit Presettable Decade and Binary Synchronous Counters

DV74LS160A, DV74LS161A
DV74LS162A, DV74LS163A
DV74ALS160B, DV74ALS161B
DV74LS162B, DV74ALS163B

These devices are high-speed four-bit synchronous counters which are edge-triggered, synchronously presettable, and cascadable building blocks for counting, memory addressing frequency division and other applictions. The '161 and '163 count modulo 16 (binary). The '160 and '162 count modulo 10 (BCD). A Terminal Count (TC) output is included which decodes the highest count of the respective device for convenient expandibility.
The '160 and '161 have an asynchronous Master Reset (Clear) input that overrides, and is independent of the clock and all other control inputs. The '162 and '163 have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

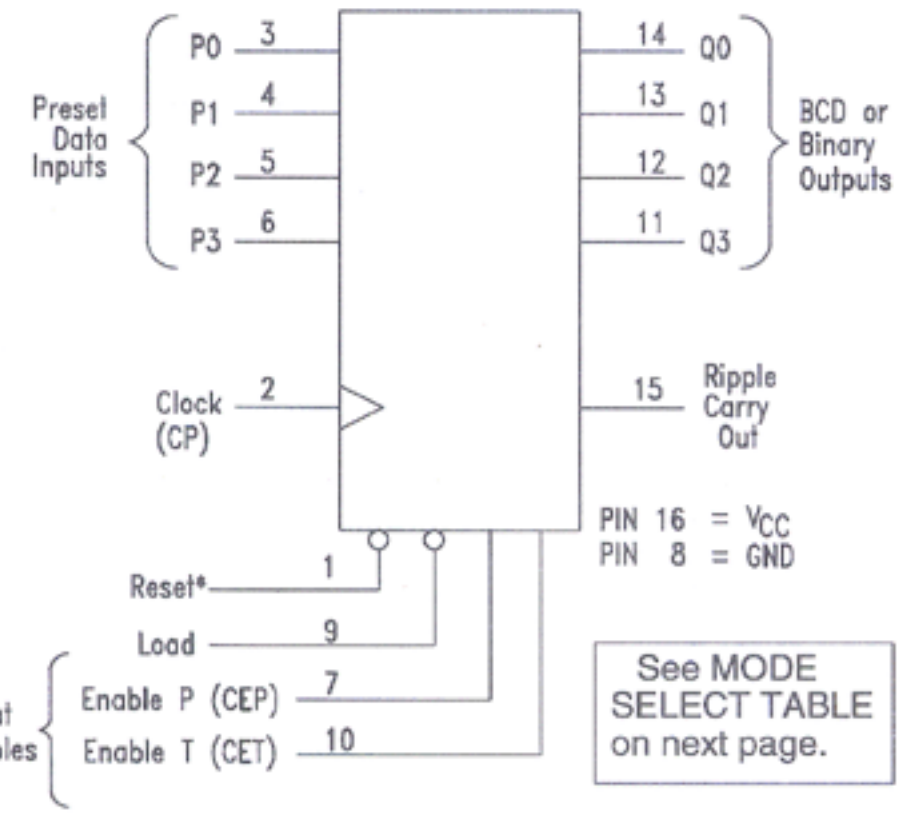


N Suffix
Plastic DIP
AVG-003 Case

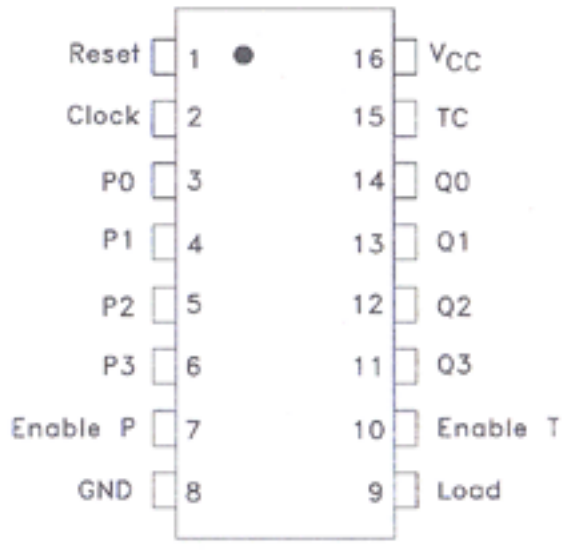
D Suffix
Plastic SOP
AVG-004 Case

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS 160A ALS160B	LS 161A ALS161B
Synchronous Reset	LS 162A ALS162B	LS163A ALS163B

- **AVG's LS operates over extended Vcc from 4.5 to 5.5 V**
- **AVG's LS and ALS both have guaranteed DC and AC specification over full temperature and Vcc range**
- **Switching specifications for ALS at 50 pF**
- **AVG's ALS has the lowest speed power product (4pJ per gate typical) of all logic series**



See MODE SELECT TABLE on next page.



LOGIC EQUATIONS

Count Enable=CEP·CET·$\overline{LOAD}$
TC for160 &162=CET·Q_0·$\overline{Q_1}$·$\overline{Q_2}$·Q_3
TC for $\overline{161 \text{ \& } 163}$=CET·$Q_0$·$Q_1$·$Q_2$·$Q_3$
Preset=$\overline{LOAD}$·CP↑(rising clock edge)
*Reset acts differently for these devices. See Pin Names.

NOTE:
The 160 and 162 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

PIN NAMES

Load	Parallel Enable (Active LOW) Input
P0-P3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
Reset	Count Reset Asynchronous Active low Reset for 160 & 161 Synchronous Active low Reset along with rising clock edge for 162 and 163
Q0-Q3	Parallel Outputs
TC	Terminal Count Output
Clock	Clock -Active high going edge

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	LS160A, 161A, 162A, 163A	ALS160, 161B, 162B, 163B	Unit
V_{CC}	Supply Voltage	7.0	7.0	V
V_{IN}	Input Voltage	–0.5 to +7.0	7.0	V
T_{STG}	Storage Temperature Range	–65 to +150	–65 to +150	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	LS160A, 161A, 162A, 163A		ALS160, 161B, 162B, 163B		Unit
		Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	2.0		2 .0		V
V_{IL}	Low Level Input Voltage		0.8		0.8	V
I_{OH}	High Level Output Current		-0.4		-0.4	mA
I_{OL}	Low Level Output Current		8.0		8.0	mA
T_A	Ambient Temperature Range	–10 to +70		–10 to +70		°C

DC ELECTRICAL CHARACTERISTICS over full operating range

Symbol	Parameter	Conditions	LS160A, 161A, 162A, 163A			ALS160, 161B, 162B, 163B			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = min, I_{IN} = –18 mA			–1.5			–1.5	V
V_{OH}	High Level Output Voltage	V_{CC}=min, I_{OH}= –0.4mA	Vcc-2	3.5		Vcc-2			V
		V_{CC}=min, I_{OH}=max							
V_{OL}	Low Level Output Voltage	V_{CC}=min; I_{OL} =4.0mA		0.25	0.4		0.2	0.4	V
		V_{CC}=min; I_{OL} =8.0 mA		0.35	0.5		0.3	0.5	V
I_{IH}	High Level Input Current Data, CEP, CP, MR CET, SR, LOAD	V_{CC}=max, V_{IH}=2.7V			 20 40			 20 20	µA
	Data, CEP, CP, MR CET, SR, LOAD	V_{CC}=max, V_{IH}=7.0V			0.1 0.2			0.1 0.1	mA
I_{IL}	Low Level Input Current Data, CEP, CP, MR CET, SR, LOAD	V_{CC}=max, V_{IN}=0.4V			 –0.4 –0.8			 –0.1 –0.1	mA
I_{OS}	Short Circuit Current	V_{CC}=max, V_O=2.25 V	–20			–30		–112	mA
I_{CC}	Supply Current	V_{CC}=max			32		12	21	mA

MODE SELECT TABLE

Reset*	'160, '161, '162, 163			Action on the Rising Clock Edge ↑
	LOAD	CET	CEP	
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD (Pn→Qn)
H	H	H	H	Count (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

H=High Logic Level L=Low Logic Level
X=Don't Care
↑= Low to High Transition
* 162 & 163 only, 160 & 161 reset asynchronously

AC CHARACTERISTICS over full operating conditions

Symbol	Parameter	LS160A, 161A, 162A, 163A 163A C_L=15pF		ALS160, 161B, 162B, 163B C_L= 50 pF R_L= 500Ω		Unit
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	25		40		MHz
t_{PLH}	Propagation Delay, Clock to Output Q		24	4	15	ns
t_{PHL}			27	6	20	
t_{PLH}	Propagation Delay, CET to TC Out		14	3	13	ns
t_{PHL}			14	3	13	
t_{PHL}	Reset to Output Q		28	8	24	ns
t_{PHL}	Reset to Ripple Carry Out (160-161 Only)		28	11	23	ns

AC SETUP REQUIREMENTS over full operating conditions

Symbol	Parameter	LS160A, 161A, 162A, 163A		ALS160, 161B, 162B, 163B		Unit
		Min	Max	Min	Max	
t_w	Pulse Width, Clock	25		12.5		ns
t_w	Pulse Width, Reset (160-161Only)	20		15		ns
t_s	Setup Time, Data, Enable P or Enable T	20		15		ns
t_s	Setup Time, SR, LOAD	25		15		ns
t_s	Setup Time, CEP, CET, DATA	25		15		ns
t_h	Hold Time	0		0		ns
t_{rec}	Recovery Time, Reset to Clock (160-161 Only)	15		10		ns

SWITCHING WAVEFORMS