GM76C8128A/AL/ALL

131,072 WORDS×8 BIT
CMOS STATIC RAM

Description

The GM76C8128A/AL/ALL is a 1,084,576 bits static random access memory organized as 131,072 words by 8 bits. Using a 0.8um advanced CMOS technology, it provides high speed operation with minimum cycle time of 70/85/100ns. The device is placed in a low power standby mode with $\overline{CS1}$ high or CS2 low and the output enable ($\overline{OE}$) allows fast memory access. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.
The GM76C8128A/AL/ALL is offered in a 32-pin DIP (600mil), SOP (525 mil) and TSOP I (0820).

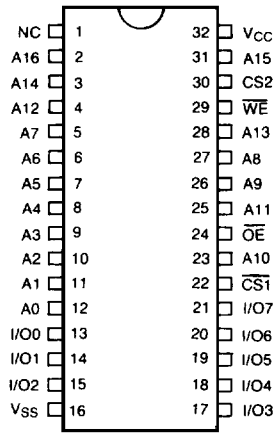
Features

- High Speed: Fast Access and Cycle Time 70/85/100ns Max.
- Low Power Standby and Low Power Operation.
  Standby: 5.5mW Max.
  Standby: 0.55mW Max. (Low Power Version)
  Standby: 0.275mW Max (Low Low Power Version)
  Operation: 385mW (Max)
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back up Operation
- Single +5V Operation (±10%)
- Standard 32 DIP, SOP and TSOP I

Pin Description

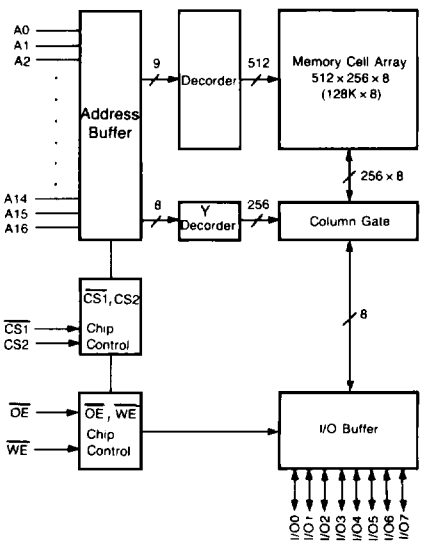
Pin	Function
A0 ~ A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O0 ~ I/O7	Data Inputs/Outputs
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.0	W

*: -3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{DR}	Data Retention Supply Voltage	2.0	—	5.5	V

Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A1 to A16	DATA I/O	Mode
L	H	L	H	stable	Output Data	Read
L	H	X	L	stable	Input Data	Write
L	H	H	H	stable	Hi-Z	Output Disable
H	X	X	X	—	Hi-Z	Standby
X	L	X	X	—	Hi-Z	

Note: X means don't care

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0 to V_{CC}	-1	—	+1	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} $\overline{OE}$ = V_{IH}, $V_{SS} \leq V_{OUT} \leq V_{CC}$	-1	—	+1	μA
I_{OH}	High Level Output Current	V_{OH} = 2.4V	-1.0	—	—	mA
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	—	—	2.1	mA
I_{CC}	Operating Supply Current	$\overline{CS1}$ = V_{IL} or CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA	—		45	mA
I_{CC1}	Average Operating Current	$\overline{CS1}$ = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0mA t_{cycle} = Min. cycle	—		70	mA
I_{CC2}		$\overline{CS1}$ = 0.2V, CS2 = V_{CC}-0.2V V_{IN} = V_{CC}-0.2V/0.2V I_{OUT} = 0mA t_{cycle} = 1μs	—	—	45	mA
I_{CCS1}	Standby Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	—	3	mA
I_{CCS2}		$\overline{CS1}$ = V_{CC}-0.2V, CS2 = 0.2V GM76C8128A GM76C8128AL GM76C8128ALL	— — —	— 2* 2*	1 100 50	mA μA μA

*TYP. Values are measured at 25°C, V_{CC} = 5V

AC Operating Characteristics ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Read Cycle

Symbol	Parameter	GM76C8128A-70		GM76C8128A-85		GM76C8128A-10		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	ns
t_{ACS1}	Chip Select 1 Access Time	—	70	—	85	—	100	ns
t_{ACS2}	Chip Select 2 Access Time	—	70	—	85	—	100	ns
t_{OE}	Output Enable Access Time	—	35	—	45	—	50	ns
t_{CHZ1}	Chip Select 1 Output Setup Time	5	—	10	—	10	—	ns
t_{CHZ1}	Chip Select 1 Output Floating	—	25	—	30	—	35	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	5	—	10	—	10	—	ns
t_{CHZ2}	Chip Select 2 Output Floating	—	25	—	30	—	35	ns
t_{OLZ}	Output Enable Output Setup Time	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable Output Floating Time	—	25	—	30	—	35	ns
t_{OH}	Output Hold Time	10	—	10	—	10	—	ns

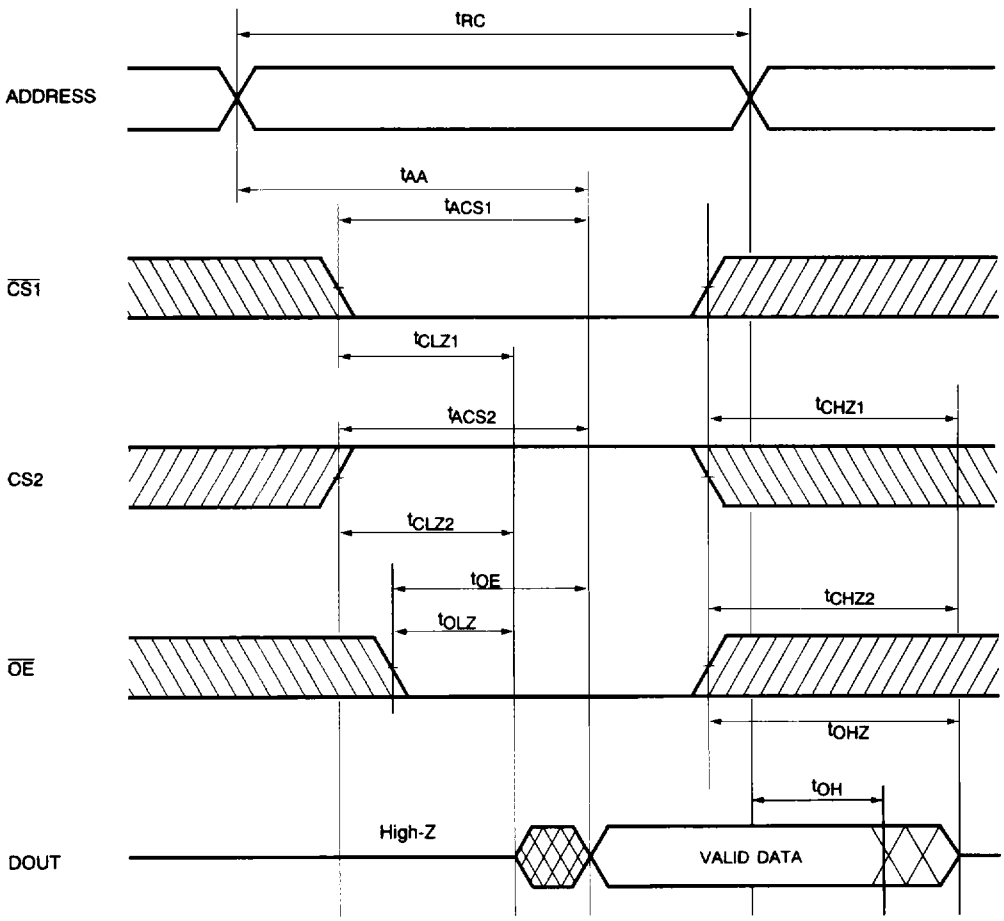
Write Cycle

Symbol	Parameter	GM76C8128A-70		GM76C8128A-85		GM76C8128A-10		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t_{CW1}	Chip Select Time 1	65	—	75	—	80	—	ns
t_{CW2}	Chip Select Time 2	65	—	75	—	80	—	ns
t_{AW}	Address Enable Time	60	—	70	—	80	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	50	—	60	—	60	—	ns
t_{WR}	Address Hold Time	0	—	0	—	0	—	ns
t_{DW}	Input Data Setup Time	30	—	35	—	40	—	ns
t_{DH}	Input Data Hold Time	0	—	0	—	0	—	ns
t_{WHZ}	R/W Output Floating	—	25	—	30	—	35	ns
t_{OW}	R/W Output Setup Time	0	—	0	—	0	—	ns

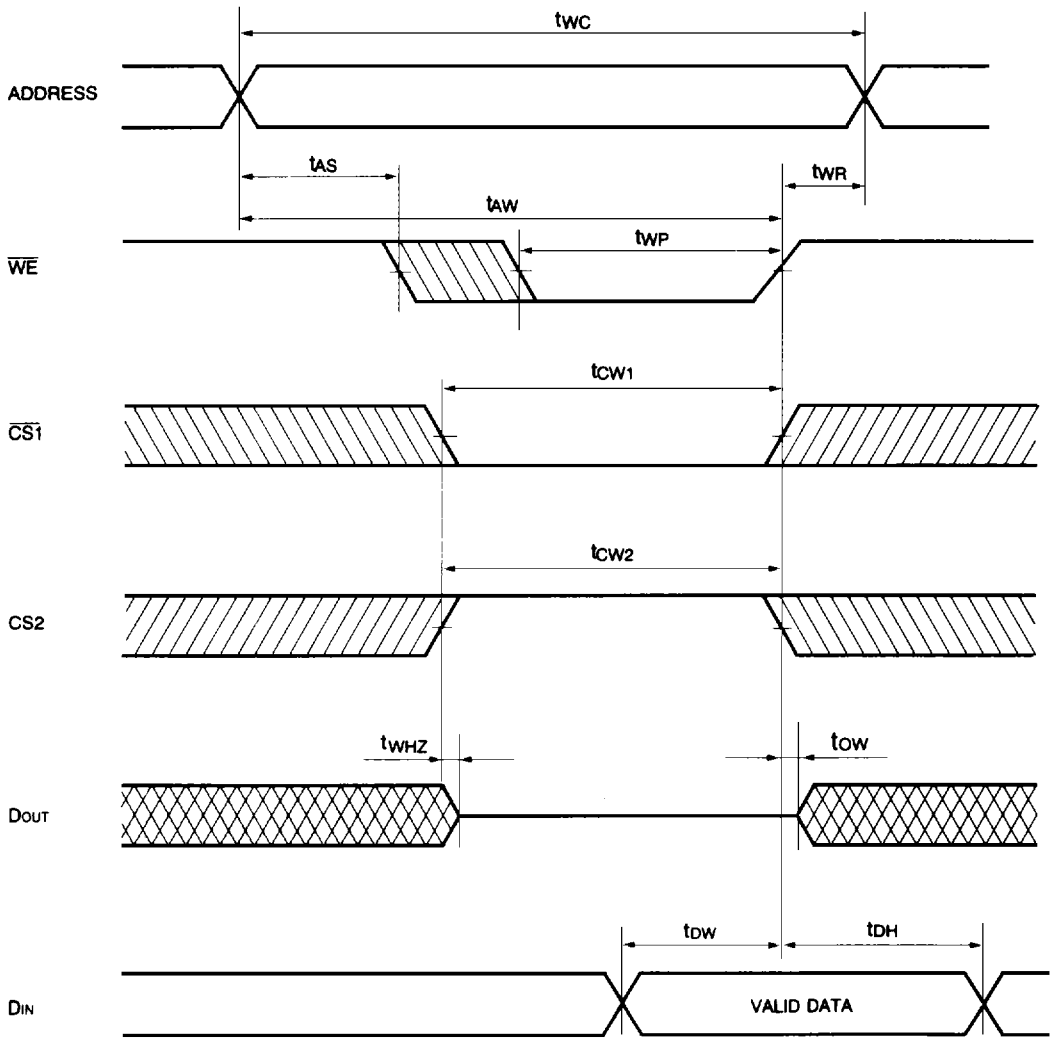
AC TEST CONDITIONS
- Output load: 100pF + 1TTL Gate
- Input pulse level: 0.6V to 2.4V
- Input and output timing reference levels 1.5V.
- $tr=t_f=5ns$

TIMING WAVEFORMS

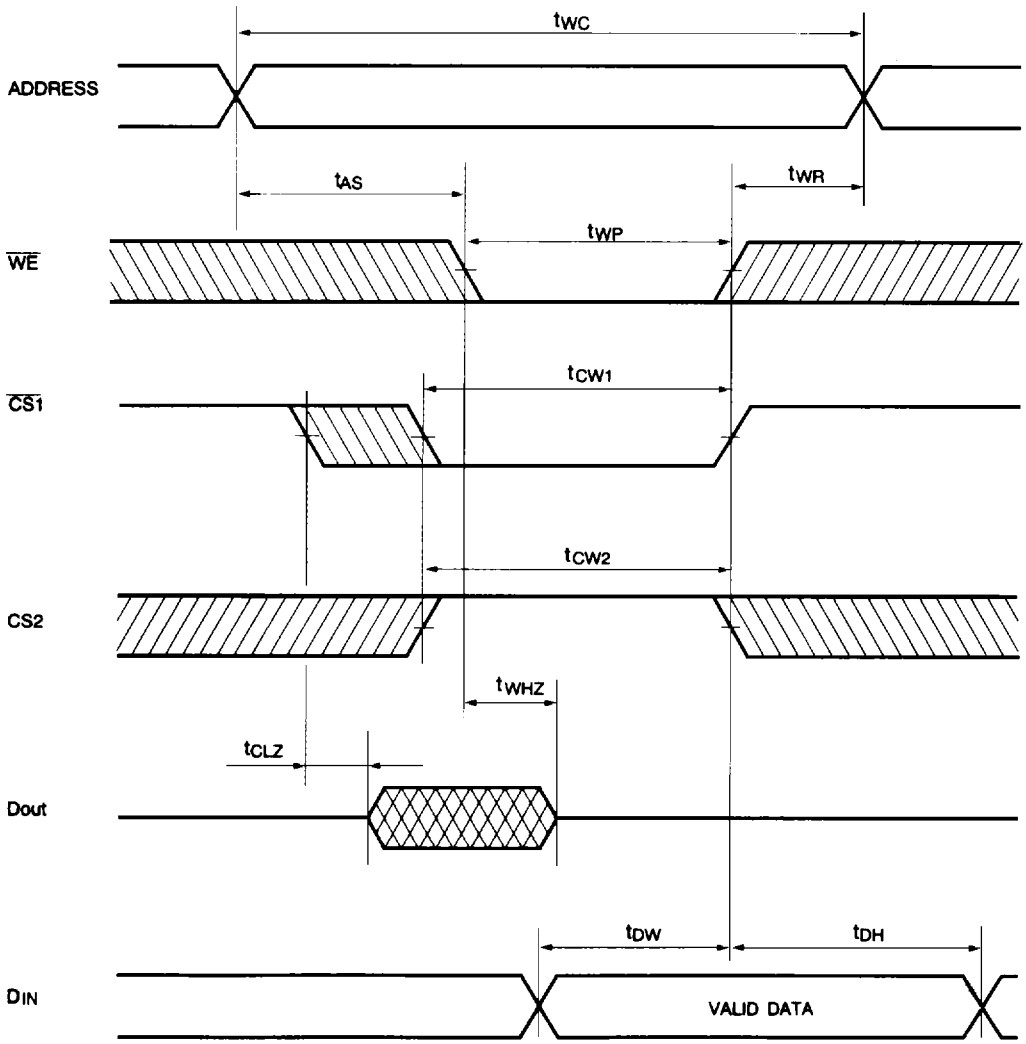
Read Cycle (Note 1)



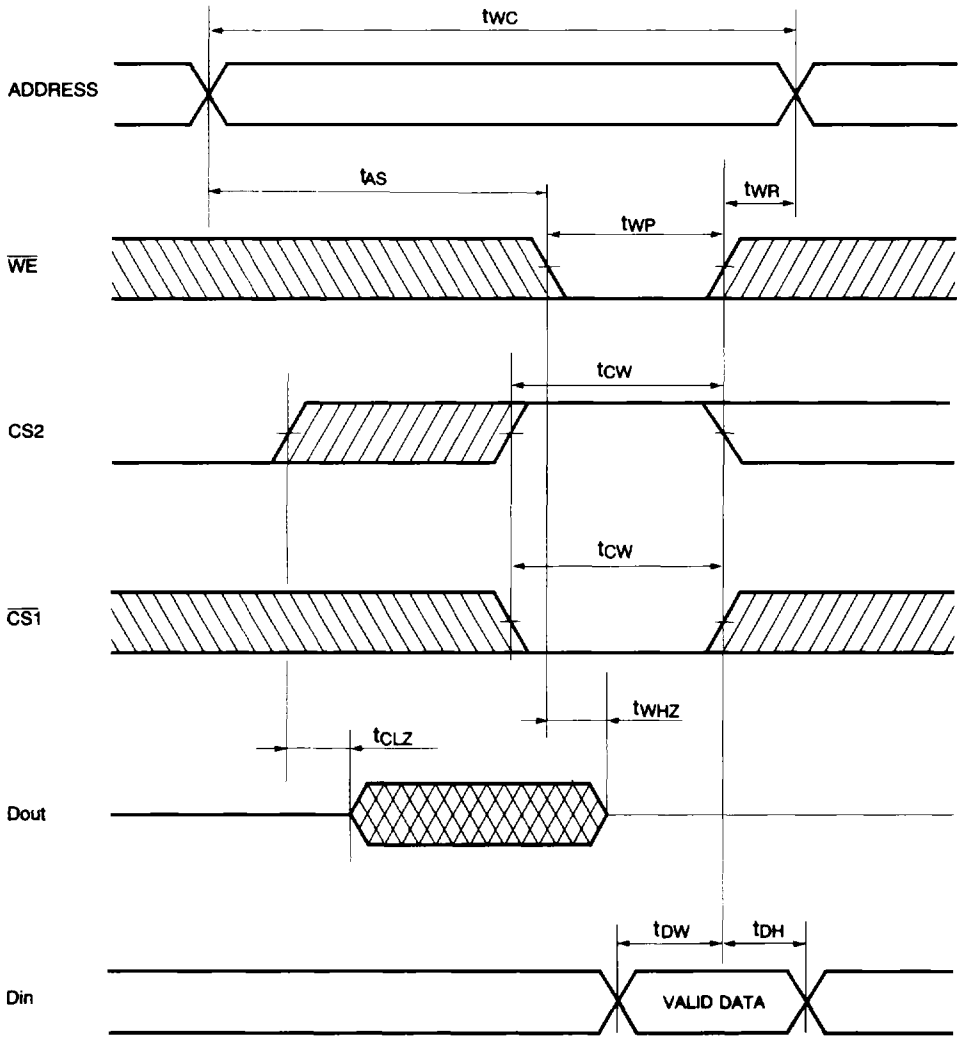
Write Cycle(1) ($\overline{WE}$ Controlled) (Notes 2,3,4)



Write Cycle (2) ($\overline{CS1}$ Controlled) (Note 4)



Write Cycle (3) (CS2 Controlled) (Note 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition. Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition. Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is high for write cycle. Outputs are in a high impedance state during this period.

Capacitance: (f = 1MHz, T_A = 25°C)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V	–	8	pF
C_{OUT}	Input Capacitance	V_O = 0V	–	8	pF

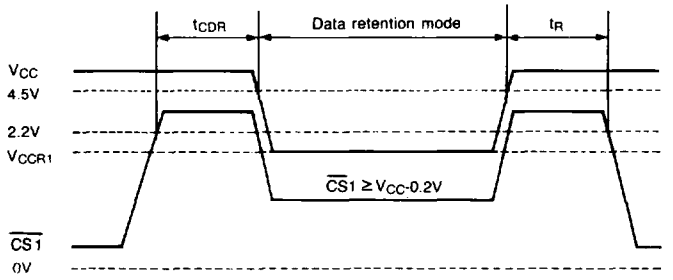
Note: This parameter is sampled and not 100% tested.

Data Retention Characteristics (T_A = 0 ~ 70°C)

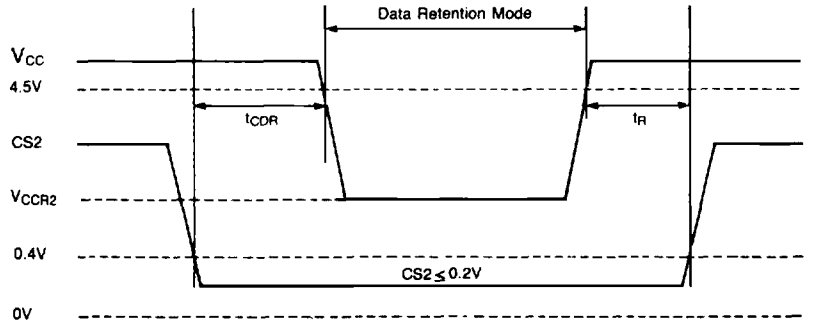
Symbol	Parameter			Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage			2.0	–	5.5	V
I_{CCR}	Data Retention Current	V_{CC} = 3.0V	L	–	1	50*	μA
			LL	–	1	25	
t_{CDR}	Chip Select to Data Retention Time			0	–	–	ns
t_R	Operation Recovery Time			5	–	–	ns

*20μA max at T_A = 0 ~ 40°...

• Low V_{CC} Data Retention Mode: (1) $\overline{CS1}$ Controlled



• Low V_{CC} Data Retention Mode: (2) CS2 Controlled

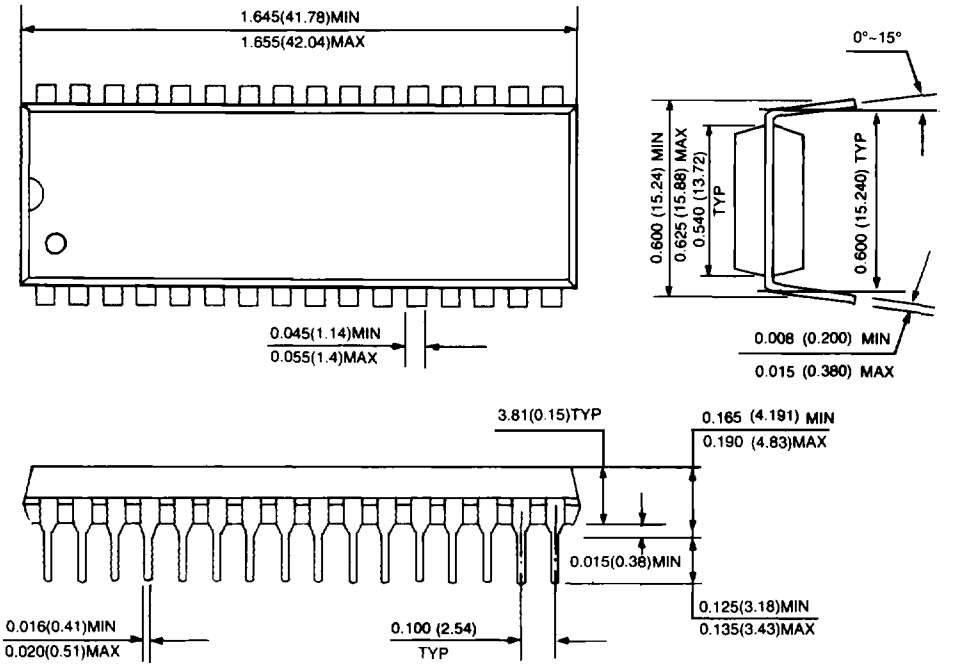


Note: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

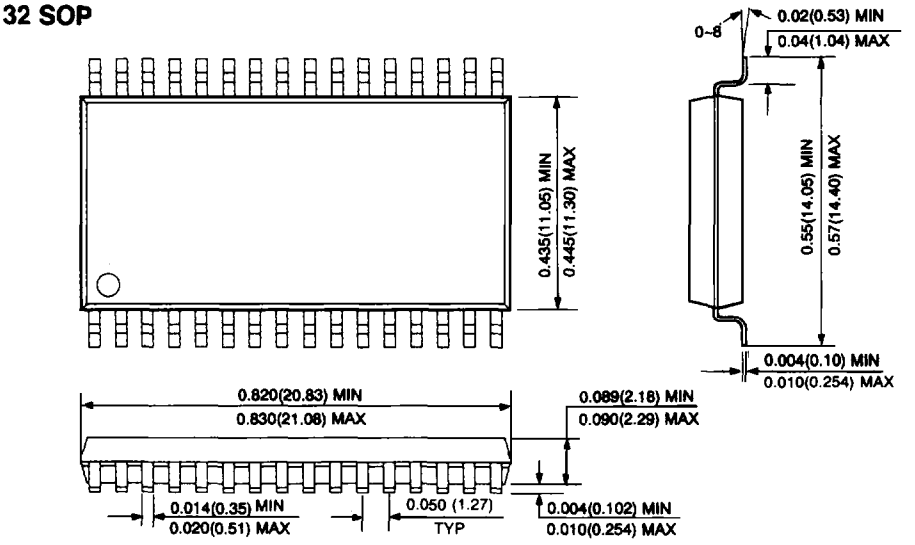
Package Dimensions

Unit: inches (mm)

32 DIP



32 SOP



32 TSOP I

Unit: inches (mm)