



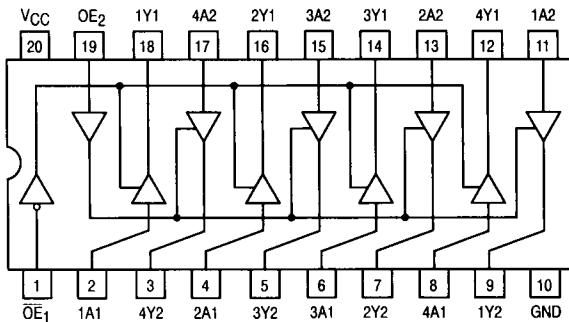
Octal Buffer With Active Low And Active High Enable 3-State Non-Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/33202

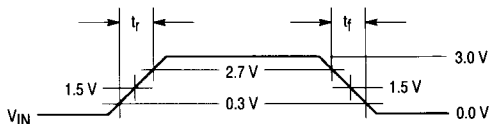
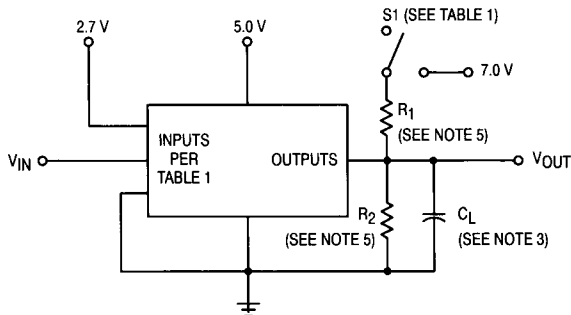
The F241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Register
- Outputs Sink 64 mA
- 15 mA Source Current
- Input Clamp Diodes Limit High Speed Termination Effects

LOGIC DIAGRAM



AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-107

Military 54F241



AVAILABLE AS:

- 1) JAN: JM38510/33202BXA
- 2) SMD: 5962-8687401
- 3) 883: 54F241/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
OE ₁	1	1	1	V _{CC}
1A1	2	2	2	V _{CC}
4Y2	3	3	3	OPEN
2A1	4	4	4	V _{CC}
3Y2	5	5	5	OPEN
3A1	6	6	6	V _{CC}
2Y2	7	7	7	OPEN
4A1	8	8	8	V _{CC}
1Y2	9	9	9	OPEN
GND	10	10	10	GND
1A2	11	11	11	V _{CC}
4Y1	12	12	12	OPEN
2A2	13	13	13	V _{CC}
3Y1	14	14	14	OPEN
3A2	15	15	15	V _{CC}
2Y1	16	16	16	OPEN
4A2	17	17	17	V _{CC}
1Y1	18	18	18	OPEN
OE ₂	19	19	19	V _{CC}
V _{CC}	20	20	20	V _{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs			Output
OE ₁	OE ₂	D	
L	H	L	L
L	H	H	H
H	L	X	Z

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = HIGH Impedance

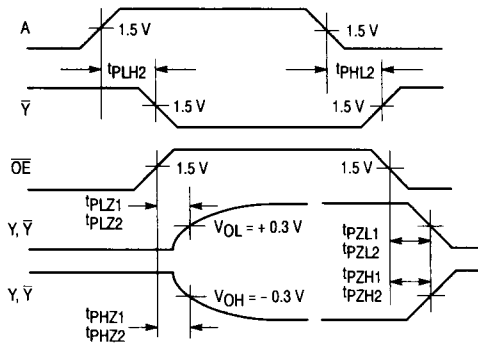
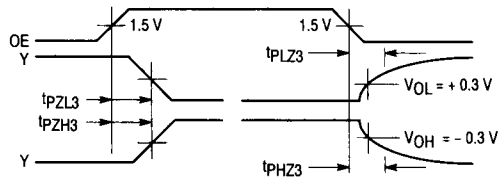
Table 1

Test Type	S1
t _{PLH}	open
t _{PHL}	open
t _{PHZ}	open
t _{PZH}	open
t _{PLZ}	closed
t _{PZL}	closed

NOTES:

1. Pulse generator has the following characteristics:
 $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, $Z_{OUT} = 50 \Omega$.
2. Inputs not under test are at 2.7 V, GND or open.
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2 = 500 \Omega \pm 5.0\%$.

WAVEFORMS



54F241

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = -3.0 mA, V _{IH} = 2.0 V, other input = 0.8 V.
V _{OL}	Logical "0" Output Voltage		0.55		0.55		0.55	V	V _{CC} = 4.5 V, I _{OL} = 48 mA, V _{IH} = 2.0 V, V _{IL} = 0.8 V (both inputs).
V _{IC}	Input Clamping Voltage		-1.2					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open.
I _{OD}	Diode Current	65		65		65		mA	V _{CC} = 4.5 V, V _{IN} = GND, OE ₂ = 4.5 V, other input = GND, V _{OUT} = 2.5 V.
I _{IL}	Logical "0" Input Current (OE)	-0.03	-1.6	-0.03	-1.6	-0.03	-1.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V, other inputs are open.
I _{IL}	Logical "0" Input Current (A)	-0.03	-1.0	-0.03	-1.0	-0.03	-1.0	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	-100	-325	-100	-325	-100	-325	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other input = 0 V, V _{OUT} = 0 V.
I _{IOZH}	Output Off Current High		50		50		50	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other input = 0 V, V _{OUT} = 2.4 V.
I _{IOZL}	Output Off Current Low		-50		-50		-50	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other input = 4.5 V, V _{OUT} = 0.5 V.
I _{CCH}	Power Supply Current		60		60		60	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other input = 0 V.
I _{CCL}	Power Supply Current		90		90		90	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
I _{CCZ}	Power Supply Current Off		90		90		90	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, OE ₂ = 0 V, other input is open.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.

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Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	- 55°C		
	Functional Tests	Subgroup 7		Subgroup 8A	Subgroup 8B	per Truth Table with $V_{CC} = 4.5\text{ V}$, (Repeat at), $V_{CC} = 5.5\text{ V}$, $V_{INL} = 0.55\text{ V}$, $V_{INH} = 2.4\text{ V}$.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
	Switching Parameters:	Min	Max	Min	Max	Min	Max		
t _{PHL2}	Propagation Delay /Data-Output Output High-Low	1.0	5.2	1.0	7.0	1.0	7.0	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PLH2}	Propagation Delay /Data-Output Output Low-High	1.0	5.2	1.0	6.5	1.0	6.5	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PLZ2}	Propagation Delay /Data-Output Output Low-High	2.0	6.0	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PHZ2}	Propagation Delay /Data-Output Output High-Low	2.0	6.0	2.0	7.0	2.0	7.0	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PZL2}	Propagation Delay /Data-Output Output Low-High	2.0	7.0	2.0	8.5	2.0	8.5	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PZH2}	Propagation Delay /Data-Output Output High-Low	2.0	5.7	2.0	7.0	2.0	7.0	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PHZ3}	Propagation Delay /Data-Output Output Low-High	2.0	6.0	2.0	7.0	2.0	7.0	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PZH3}	Propagation Delay /Data-Output Output High-Low	2.0	5.7	2.0	7.0	2.0	7.0	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PLZ3}	Propagation Delay /Data-Output Output Low-High	2.0	6.0	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.
t _{PZL3}	Propagation Delay /Data-Output Output Low-High	2.0	7.0	2.0	8.5	2.0	8.5	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = R_2 = 500\ \Omega$.