LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

Check for Samples: LM613

FEATURES

OP AMP

- **Low Operating Current (Op Amp): 300 μA**
- **Wide Supply Voltage Range: 4V to 36V**
- **Wide Common-Mode Range: V^- to (V^+ − 1.8V)**
- **Wide Differential Input Voltage: ±36V**
- **Available in Plastic Package Rated for Military Temp. Range Operation**

REFERENCE

- **Adjustable Output Voltage: 1.2V to 6.3V**
- **Tight Initial Tolerance Available: ±0.6%**
- **Wide Operating Current Range: 17 μA to 20 mA**
- **Tolerant of Load Capacitance**

APPLICATIONS

- **Transducer Bridge Driver**
- **Process and Mass Flow Control Systems**
- **Power Supply Voltage Monitor**
- **Buffered Voltage References for A/D's**

DESCRIPTION

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of TI's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Connection Diagrams

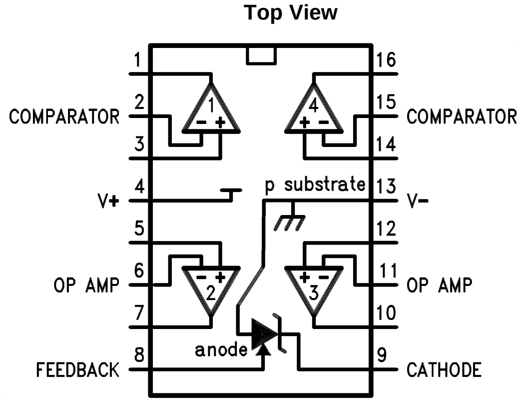


Figure 1. CDIP and SOIC Packages
See Package Numbers NFE0016A and DW0016B

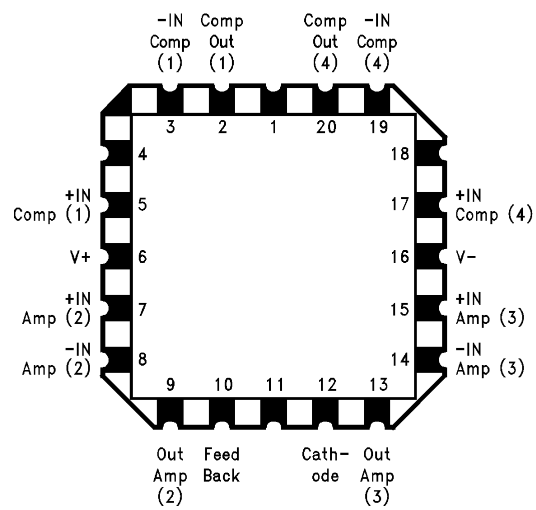
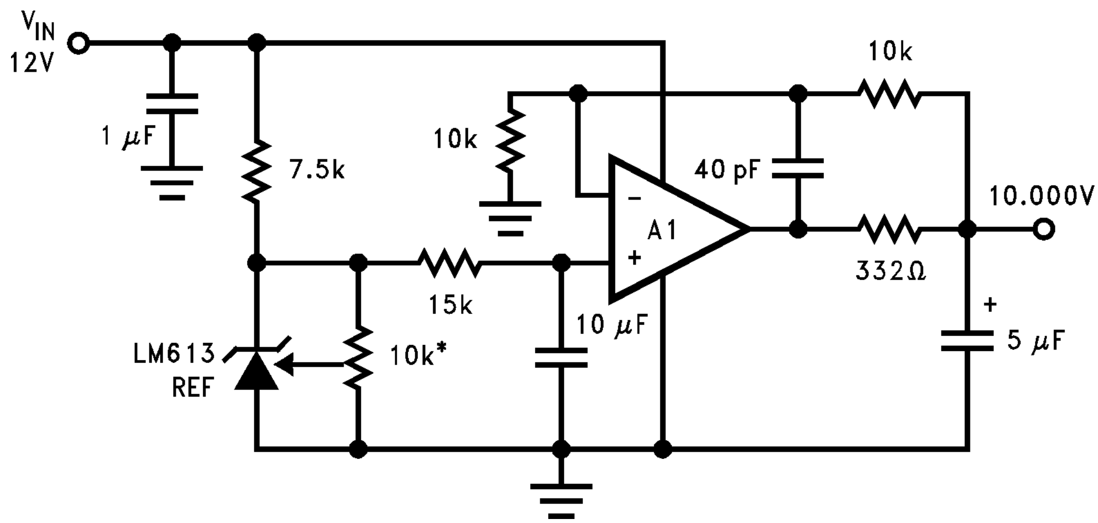


Figure 2. E Package Pinout



*10k must be low
t.c. trimpot

Figure 3. Ultra Low Noise, 10.00V Reference
Total Output Noise is Typically 14 μV_{RMS}

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

Voltage on Any Pin Except V_R (referred to V^- pin)	See [(3)]	36V (Max)
	See [(4)]	−0.3V (Min)
Current through Any Input Pin & V_R Pin		±20 mA
Differential Input Voltage	Military and Industrial	±36V
	Commercial	±32V
Storage Temperature Range		$-65°C \le T_J \le +150°C$
Maximum Junction Temperature[(5)]		150°C
Thermal Resistance, Junction-to-Ambient [(6)]	N Package	100°C/W
	DW0016B Package	150°C/W
Soldering Information (10 Sec.)	N Package	260°C
	DW0016B Package	220°C
ESD Tolerance[(7)]		±1 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.
(4) More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.
(5) Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.
(6) Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$.The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θJA is 90°C/W for the N package, and 135°C/W for the DW0016B package.
(7) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Temperature Range

LM613AI, LM613BI	−40°C to +85°C
LM613AM, LM613M	−55°C to +125°C
LM613C	$0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Parameter		Test Conditions	Typ (1)	LM613AM LM613AI Limits (2)	LM613M LM613I LM613C Limits (2)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM613C)	450 **550**	940 **1000**	1000 **1070**	µA (Max) µA (Max)
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V (Min) V (Min)
			46 **43**	36 **36**	32 **32**	V (Max) V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM613C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} =$ $(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	See (2)	**15**			µV/°C (Max)
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB (Min) dB (Min)
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/V_{OS})$	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV (Min)
SR	Slew Rate	$V^+ = 30V$ (3)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/µs
GBW	Gain Bandwidth	$C_L = 50\ pF$	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	$R_L = 10\ k\Omega$ to GND, $V^+ = 36V$ (32V for LM613C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	$R_L = 10\ k\Omega$ to V^+, $V^+ = 36V$ (32V for LM613C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V (Max) V (Max)
I_{OUT}	Output Source Current	$V_{OUT} = 2.5V$, $V^+_{IN} = 0V$, $V^-_{IN} = -0.3V$	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	$V_{OUT} = 1.6V$, $V^+_{IN} = 0V$, $V^-_{IN} = 0.3V$	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	$V_{OUT} = 0V$, $V^+_{IN} = 3V$, $V^-_{IN} = 2V$	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		$V_{OUT} = 5V$, $V^+_{IN} = 2V$, $V^-_{IN} = 3V$	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)

(1) Typical values in standard typeface are for $T_J = 25°C$; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.
(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.
(3) Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Electrical Characteristics (continued)

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Parameter		Test Conditions	Typ(1)	LM613AM LM613AI Limits(2)	LM613M LM613I LM613C Limits(2)	Units
COMPARATORS						
V_{OS}	Offset Voltage	$4V \le V^+ \le 36V$ (32V for LM613C), $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	$0V \le V_{CM} \le 36V$ $V^+ = 36V$, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			µV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V (32V for LM613C) $2V \le V_{OUT} \le 27V$	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	$V^+_{IN} = 1.4V$, V^-_{IN} = TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			µs µs
I_{SINK}	Output Sink Current	$V^+_{IN} = 0V$, $V^-_{IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)
I_{LEAK}	Output Leakage Current	$V^+_{IN} = 1V$, $V^-_{IN} = 0V$, $V_{OUT} = 36V$ (32V for LM613C)	0.1 **0.2**	10	10	µA (Max) µA (Max)
VOLTAGE REFERENCE						
V_R	Voltage Reference	See(4)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	See(5)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	See(6)	**3.2**			µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ See(7)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \to 0.1\ mA)}/9.9\ mA$ $\Delta V_{R(100 \to 17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V+}$	V_R Change with V_{ANODE} Change	$V_{R(V+ = 5V)} - V_{R(V+ = 36V)}$ ($V^+ = 32V$ for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V+ = 5V)} - V_{R(V+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \le V_{FB} \le 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)

(4) V_R is the Cathode-to-feedback voltage, nominally 1.244V.
(5) Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/(V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is ensured by design and sample testing.
(6) Hysteresis is the change in V_R caused by a change in T_J, after the reference has been “dehysterized”. To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.
(7) Low contact resistance is required for accurate measurement.

Electrical Characteristics (continued)

These specifications apply for V^{-} = GND = 0V, V^{+} = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Parameter		Test Conditions	Typ (1)	LM613AM LM613AI Limits (2)	LM613M LM613I LM613C Limits (2)	Units
e_n	V_R Noise	10 Hz to 10 kHz, V_{RO} = V_R	30			µV_{RMS}

Simplified Schematic Diagrams

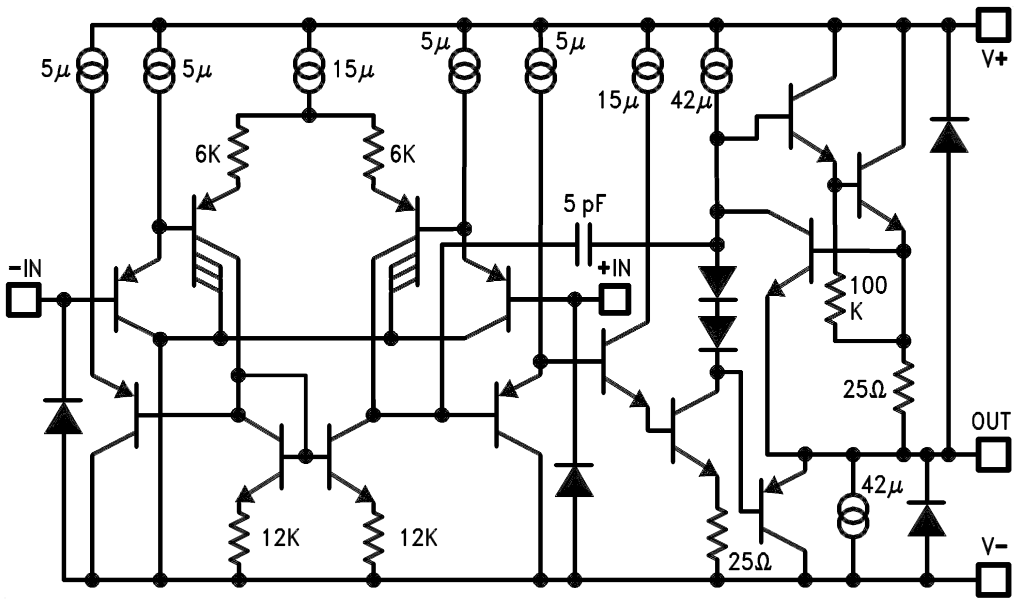


Figure 4. Op Amp

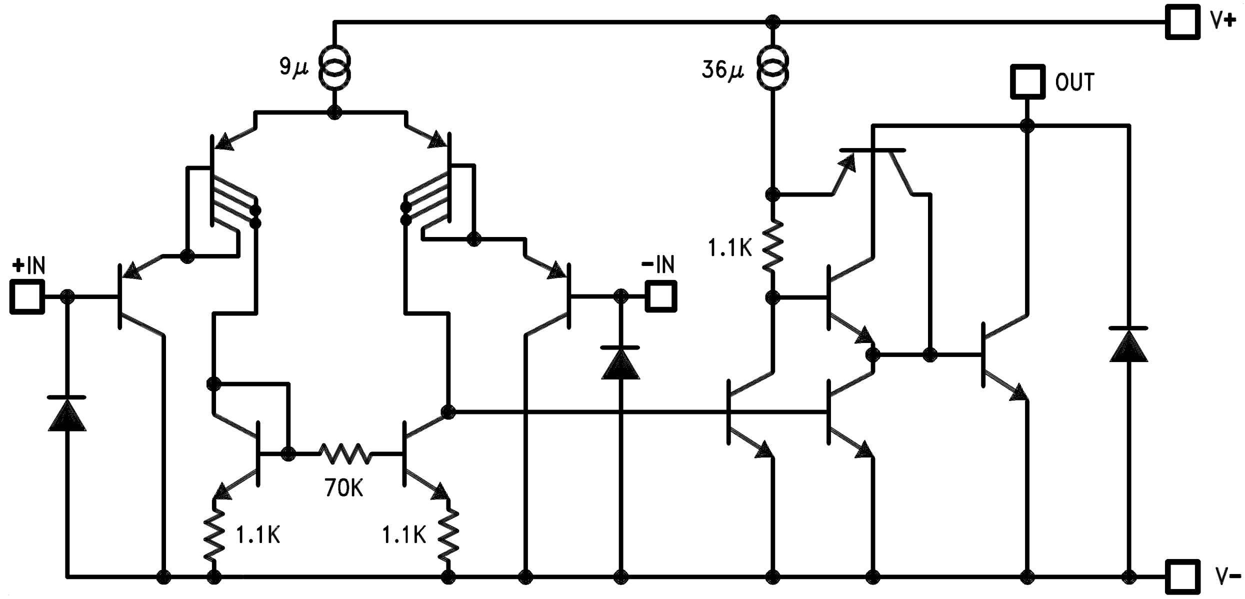


Figure 5. Comparator

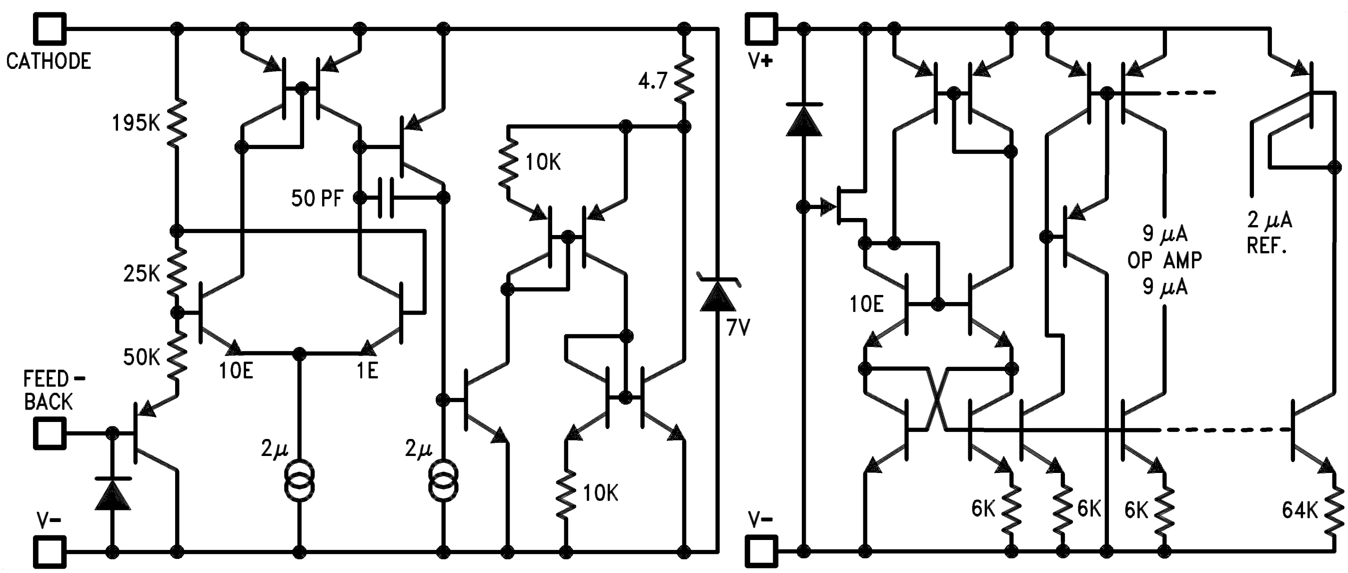


Figure 6. Reference/Bias

TYPICAL PERFORMANCE CHARACTERISTICS (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Voltage vs Temp.

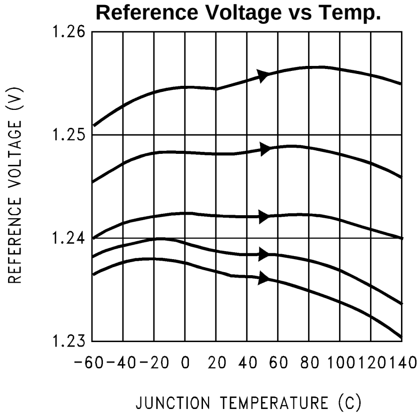


Figure 7.

Reference Voltage Drift

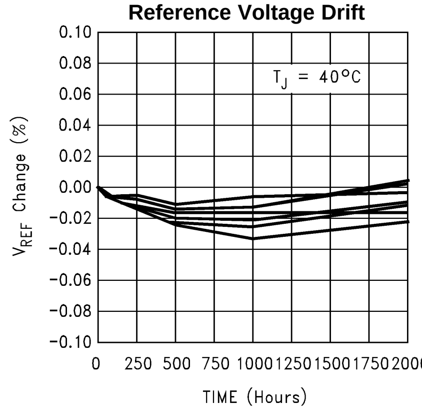


Figure 8.

Accelerated Reference Voltage Drift vs Time

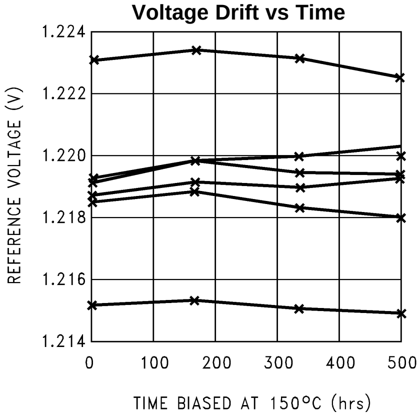


Figure 9.

Reference Voltage vs Current and Temperature

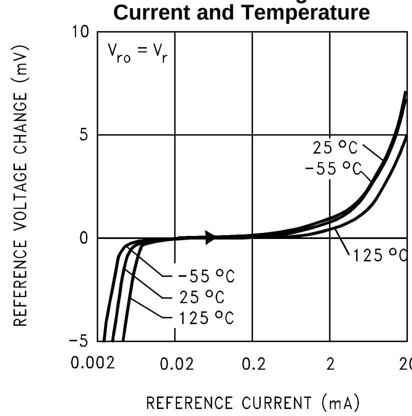


Figure 10.

Reference Voltage vs Current and Temperature

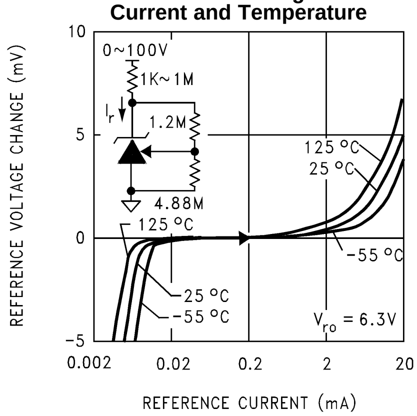


Figure 11.

Reference Voltage vs Reference Current

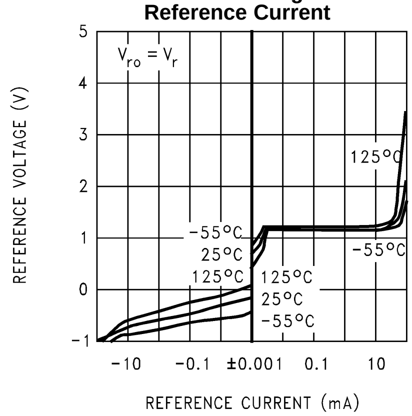


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Voltage vs Reference Current

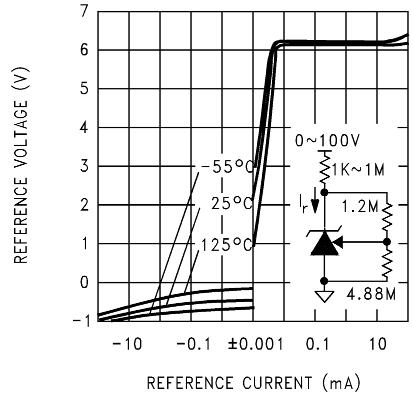


Figure 13.

Reference AC Stability Range

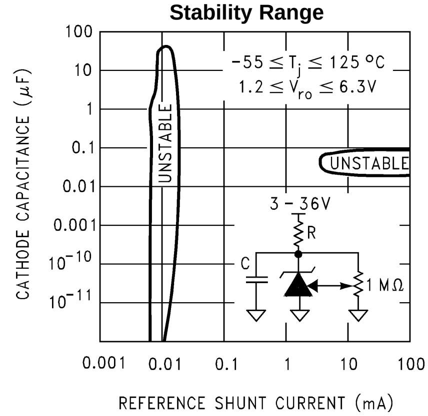


Figure 14.

FEEDBACK Current vs FEEDBACK-to-Anode Voltage

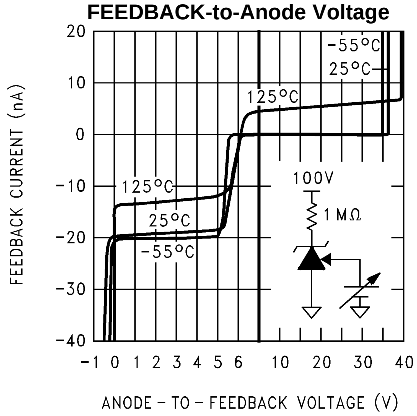


Figure 15.

FEEDBACK Current vs FEEDBACK-to-Anode Voltage

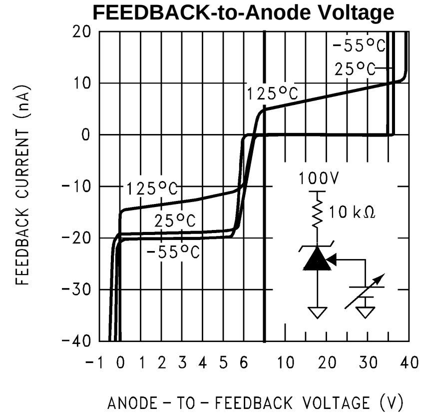


Figure 16.

Reference Noise Voltage vs Frequency

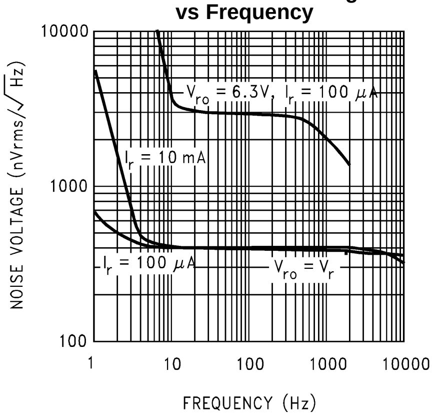


Figure 17.

Reference Small-Signal Resistance vs Frequency

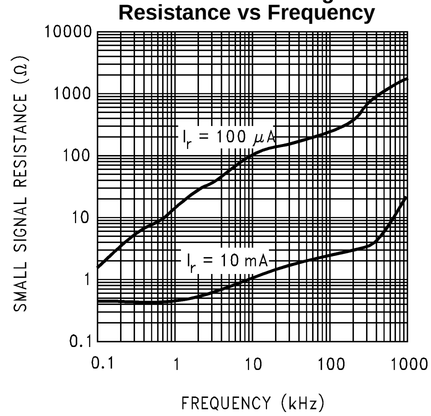


Figure 18.

TYPICAL PERFORMANCE CHARACTERISTICS (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Power-Up Time

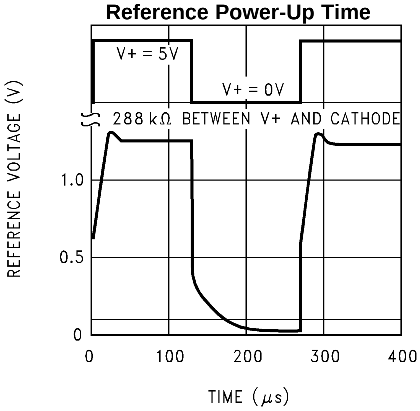


Figure 19.

Reference Voltage with FEEDBACK Voltage Step

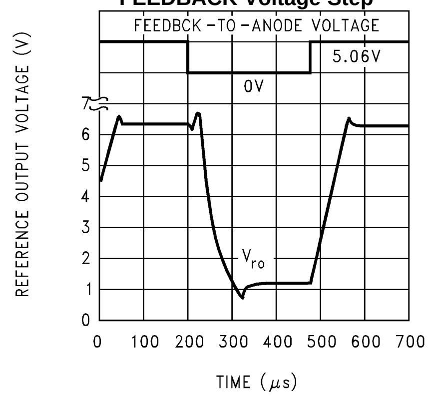


Figure 20.

Reference Voltage with 100 ~ 12 μA Current Step

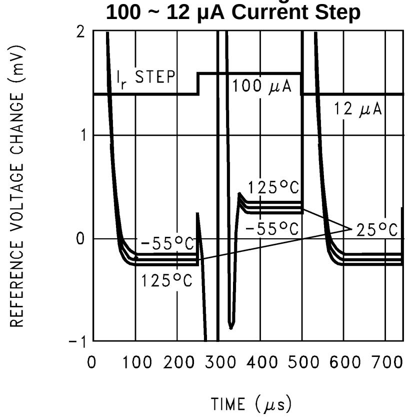


Figure 21.

Reference Step Response for 100 μA ~ 10 mA Current Step

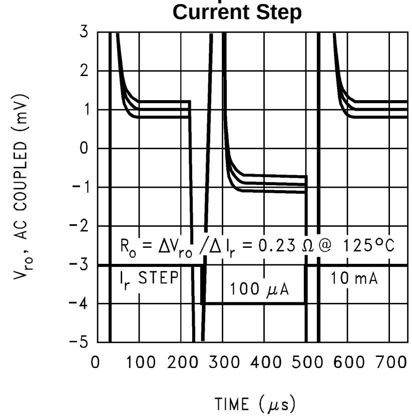


Figure 22.

Reference Voltage Change with Supply Voltage Step

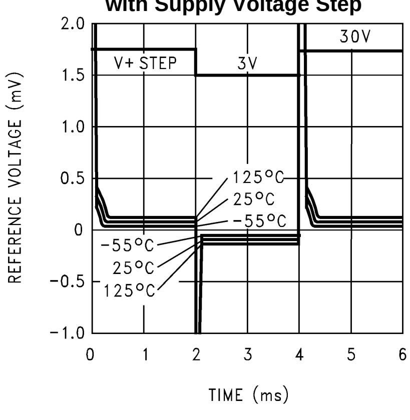


Figure 23.

Reference Change vs Common-Mode Voltage

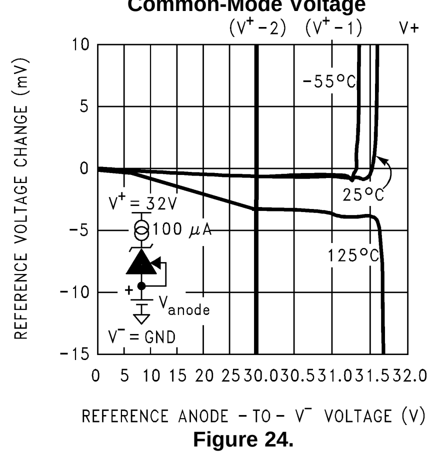


Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Input Common-Mode Voltage Range vs Temperature

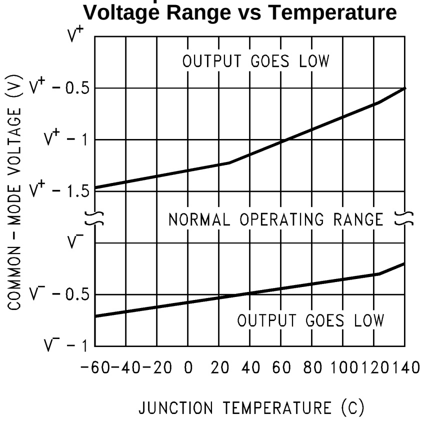


Figure 25.

V_{OS} vs Junction Temperature

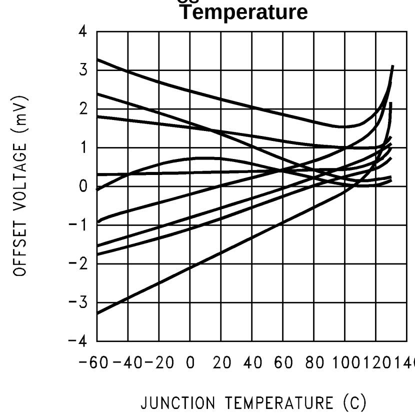


Figure 26.

Input Bias Current vs Common-Mode Voltage

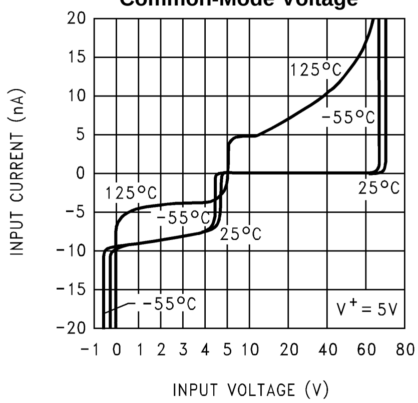


Figure 27.

Large-Signal Step Response

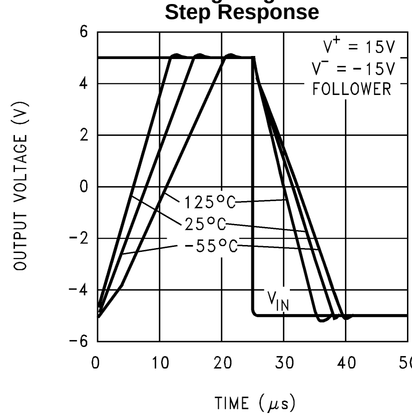


Figure 28.

Output Voltage Swing vs Temp. and Current

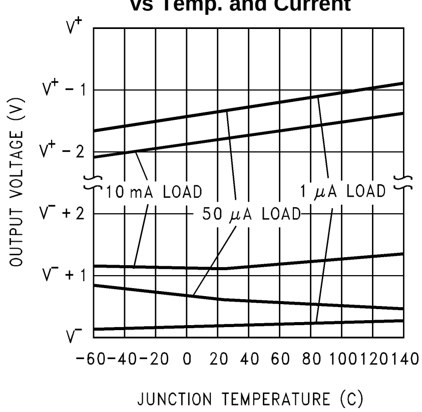


Figure 29.

Output Source Current vs Output Voltage and Temp.

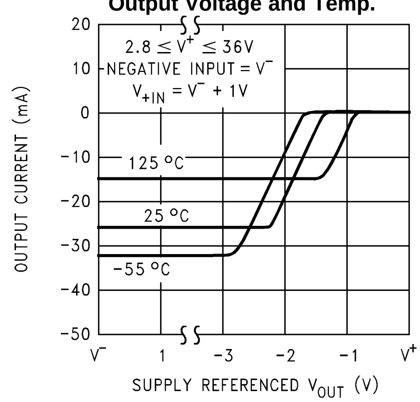


Figure 30.

TYPICAL PERFORMANCE CHARACTERISTICS (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = V^+/2, V_{OUT} = V^+/2, T_J = 25°C, unless otherwise noted

Output Sink Current vs Output Voltage

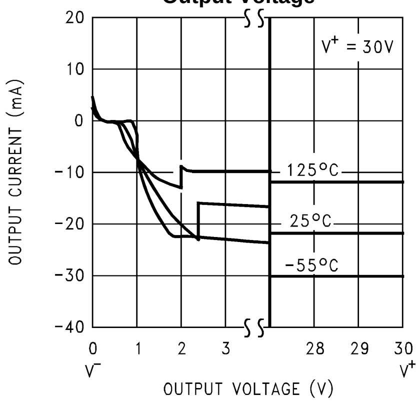


Figure 31.

Output Swing, Large Signal

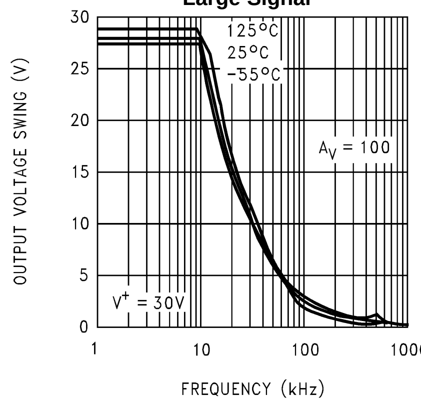


Figure 32.

Output Impedance vs Frequency and Gain

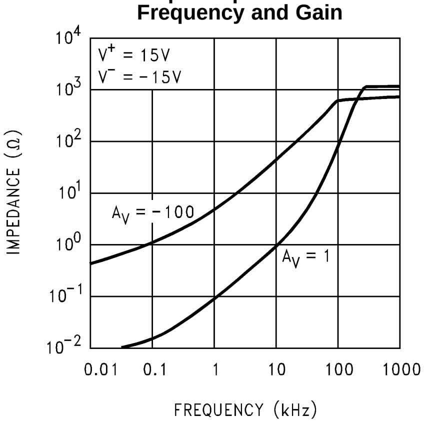


Figure 33.

Small Signal Pulse Response vs Temp.

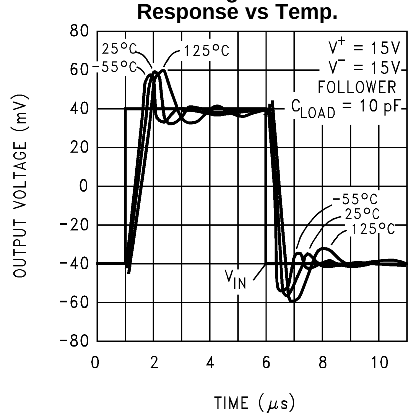


Figure 34.

Small-Signal Pulse Response vs Load

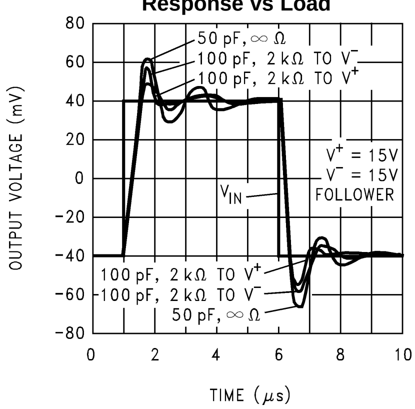


Figure 35.

Op Amp Voltage Noise vs Frequency

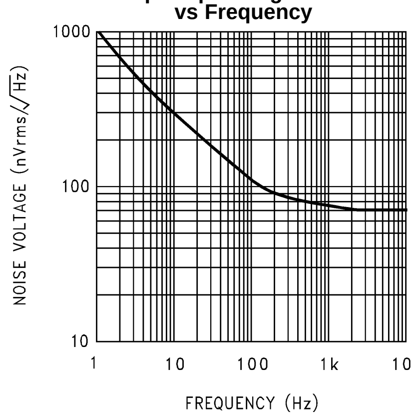


Figure 36.

TYPICAL PERFORMANCE CHARACTERISTICS (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

Op Amp Current Noise vs Frequency

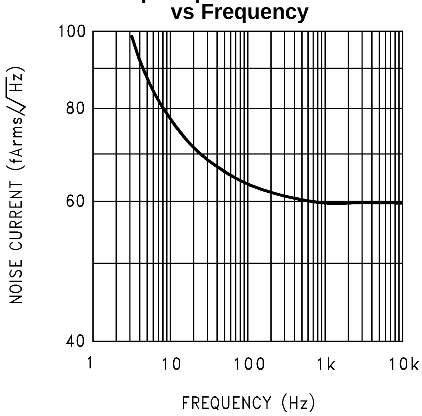


Figure 37.

Small-Signal Voltage Gain vs Frequency and Temperature

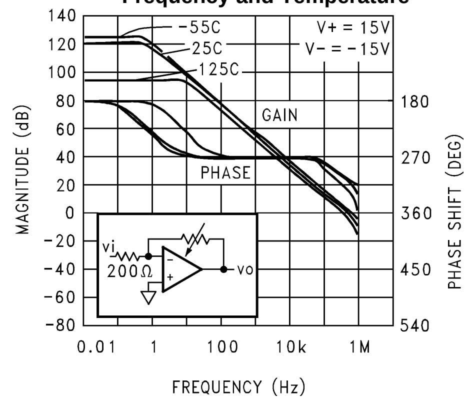


Figure 38.

Small-Signal Voltage Gain vs Frequency and Load

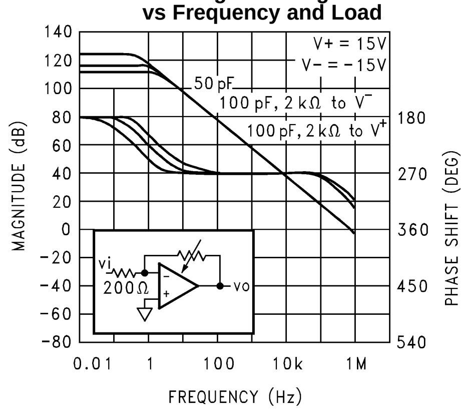


Figure 39.

Follower Small-Signal Frequency Response

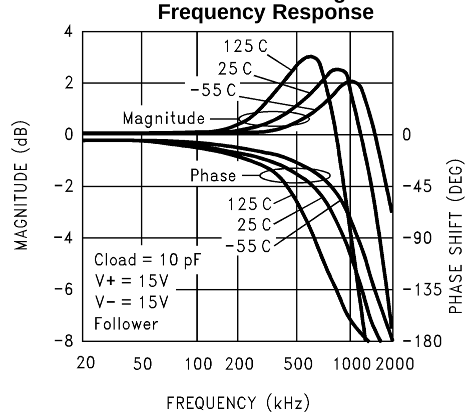


Figure 40.

Common-Mode Input Voltage Rejection Ratio

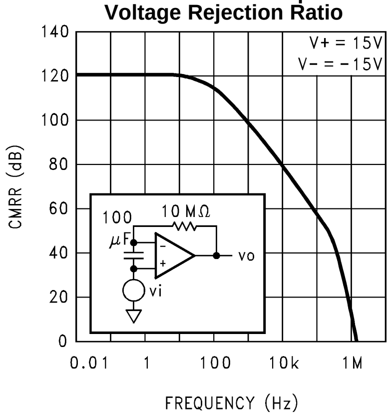


Figure 41.

Power Supply Current vs Power Supply Voltage

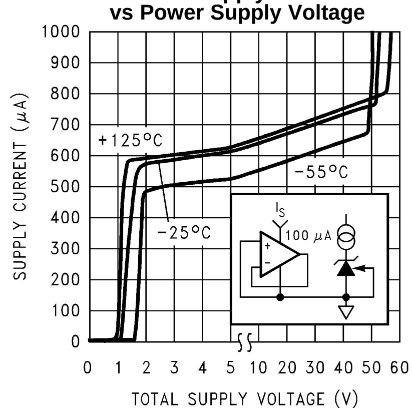


Figure 42.

TYPICAL PERFORMANCE CHARACTERISTICS (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

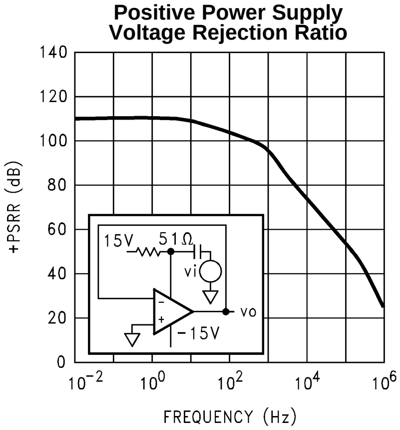


Figure 43.

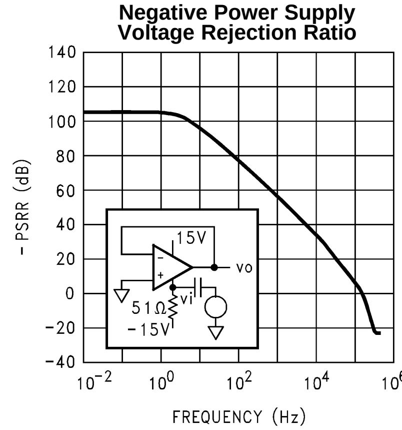


Figure 44.

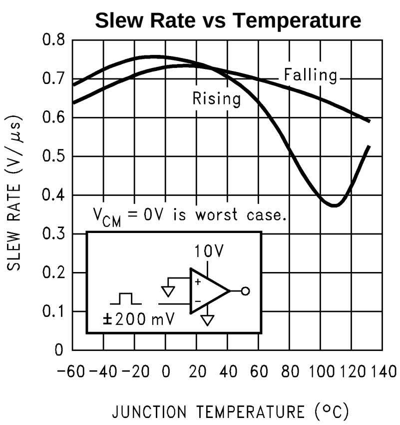


Figure 45.

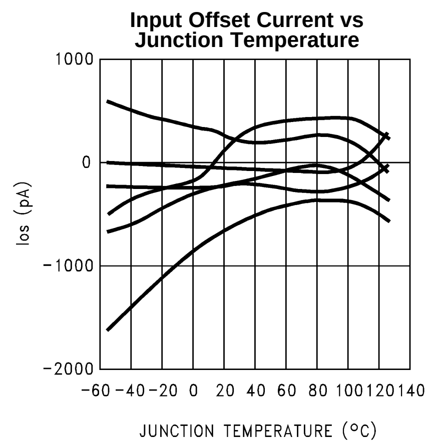


Figure 46.

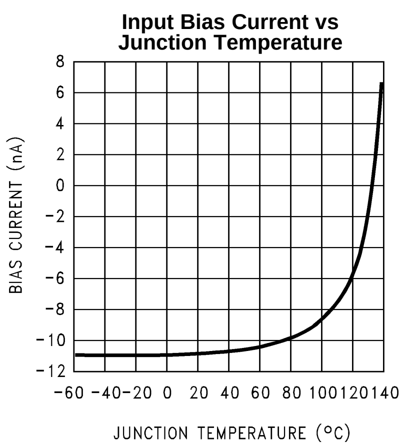


Figure 47.

TYPICAL PERFORMANCE CHARACTERISTICS (Comparators)

Output Sink Current

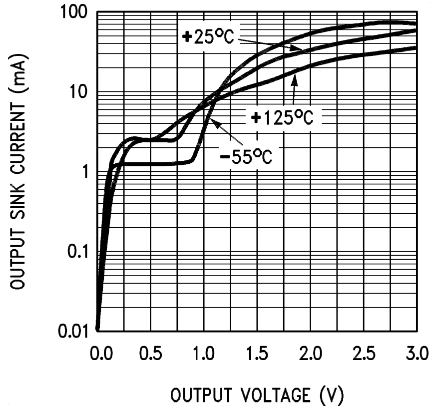


Figure 48.

Input Bias Current vs Common-Mode Voltage

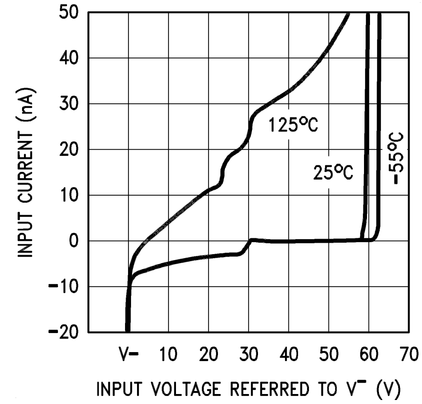


Figure 49.

Comparator Response Times— Inverting Input, Positive Transition

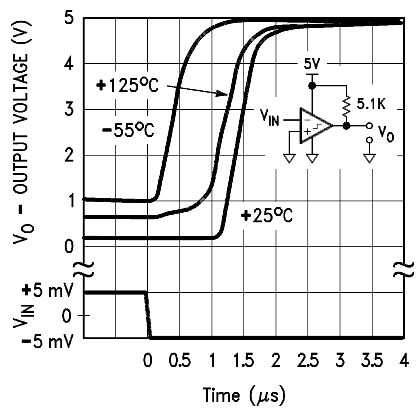


Figure 50.

Comparator Response Times— Inverting Input, Negative Transition

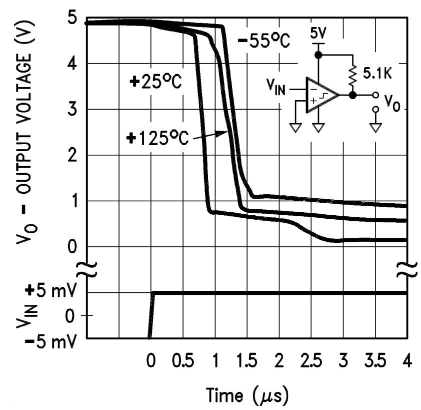


Figure 51.

Comparator Response Times— Non-Inverting Input, Positive Transition

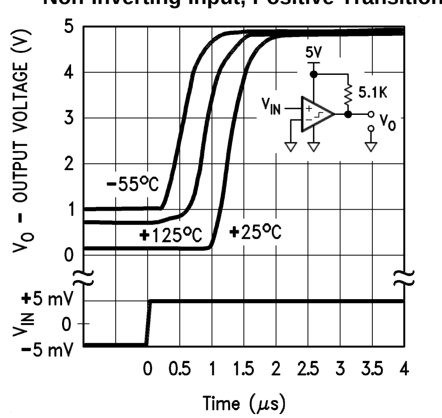


Figure 52.

Comparator Response Times— Non-Inverting Input, Negative Transition

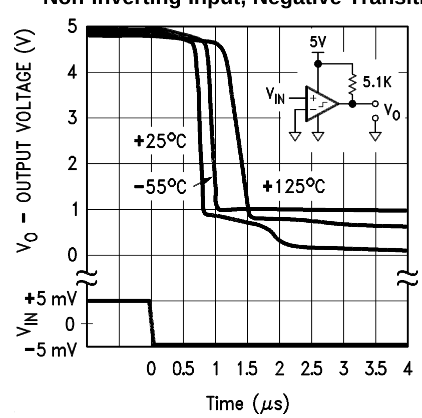


Figure 53.

TYPICAL PERFORMANCE CHARACTERISTICS (Comparators) (continued)

Comparator Response Times— Inverting Input, Positive Transition

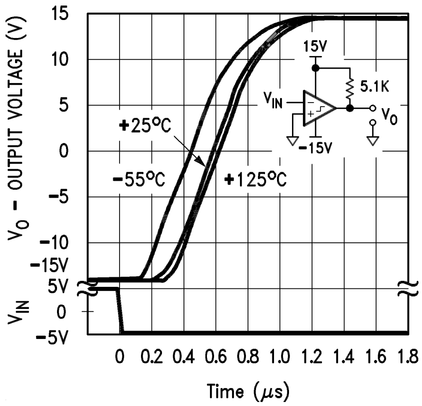


Figure 54.

Comparator Response Times— Inverting Input, Negative Transition

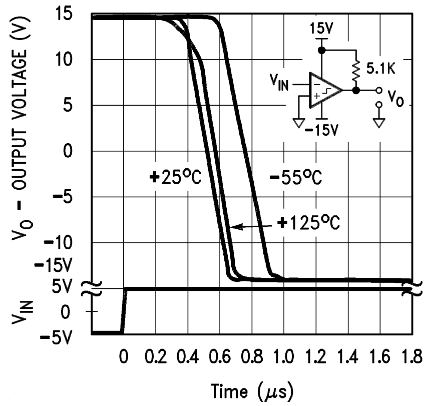


Figure 55.

Comparator Response Times— Non-Inverting Input, Positive Transition

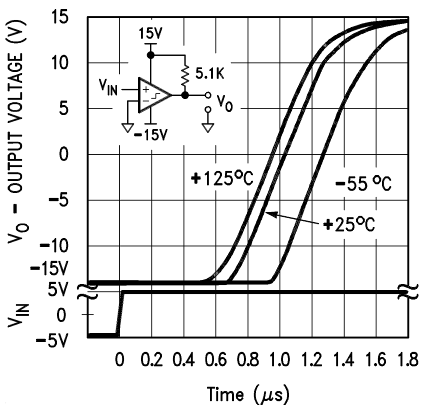


Figure .

Comparator Response Times— Non-Inverting Input, Negative Transition

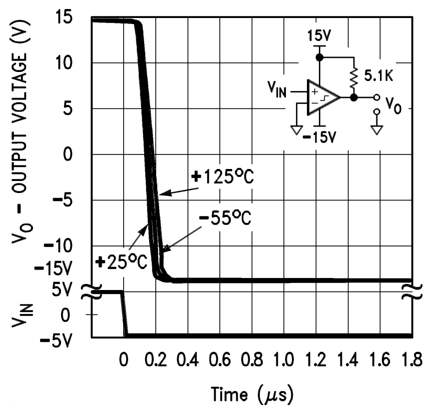


Figure 56.

TYPICAL PERFORMANCE DISTRIBUTIONS

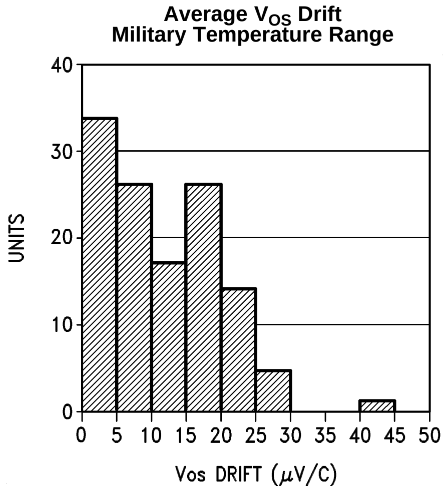


Figure 57.

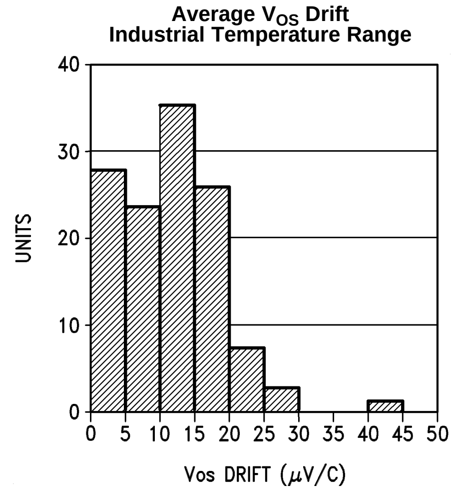


Figure 58.

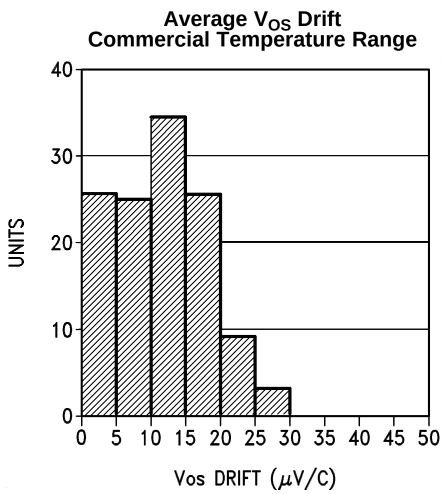


Figure 59.

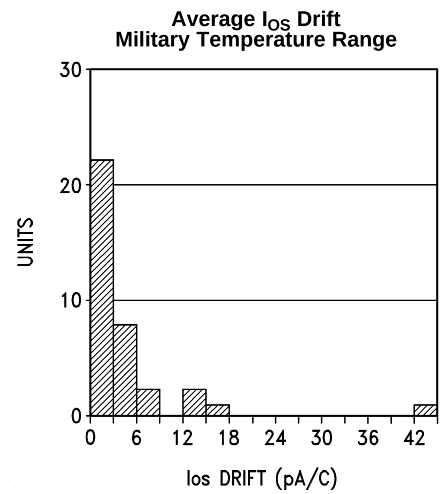


Figure 60.

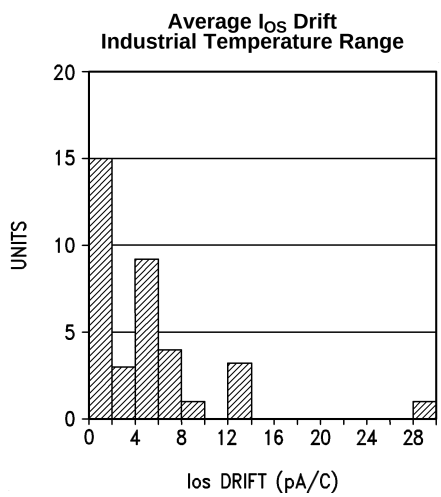


Figure 61.

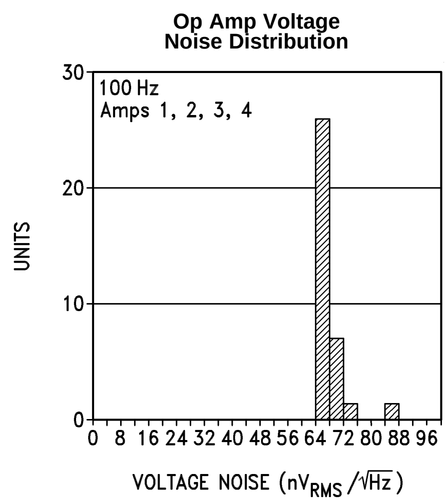


Figure 62.

TYPICAL PERFORMANCE DISTRIBUTIONS (continued)

Average I_{OS} Drift Commercial Temperature Range

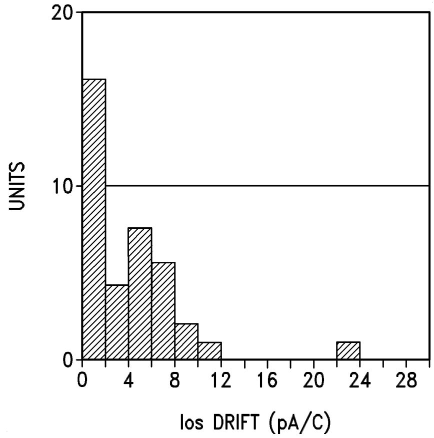


Figure 63.

Op Amp Current Noise Distribution

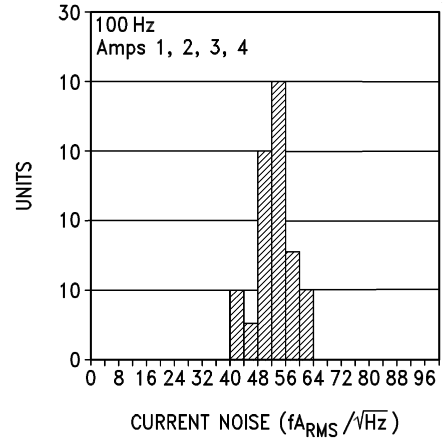


Figure 64.

Voltage Reference Broad-Band Noise Distribution

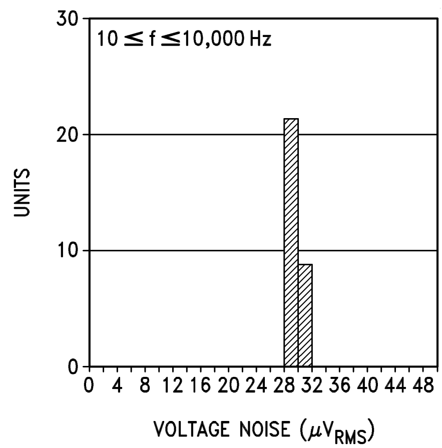


Figure 65.

APPLICATION INFORMATION

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.

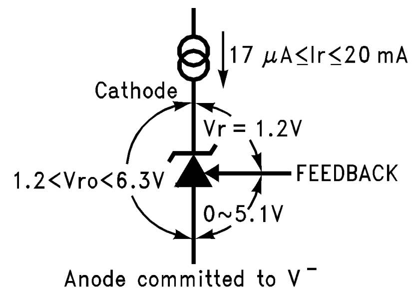


Figure 66. Voltage Associated with Reference (current source I_r is external)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

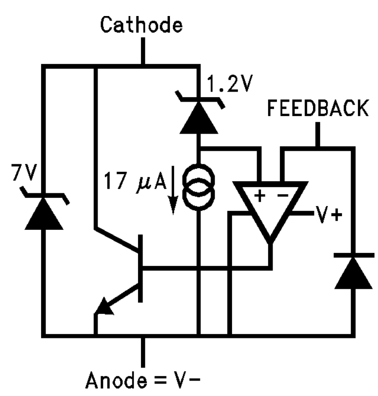


Figure 67. Reference Equivalent Circuit

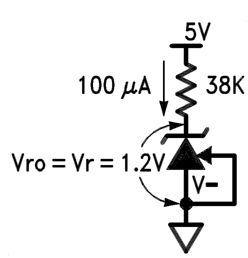


Figure 68. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then V_{ro} = V_r = 1.24V. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constant V_r generates a current I=R1/V_r flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2=3.76/I. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 μA for the military grade over the military temperature range (I≥5.5 μA for a 1% untrimmed error for a commercial part).

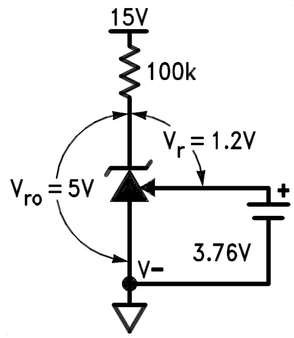
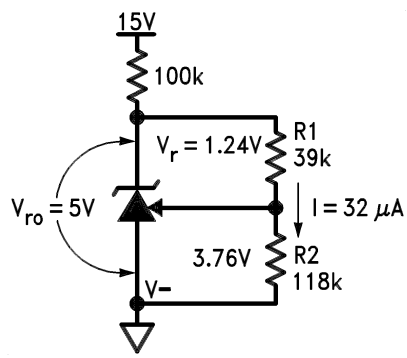


Figure 69. Thevenin Equivalent of Reference with 5V Output



R1 = Vr/I = 1.24/32μ = 39k
R2 = R1 {(Vro/Vr) − 1} = 39k {(5/1.24) − 1)} = 118k

Figure 70. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

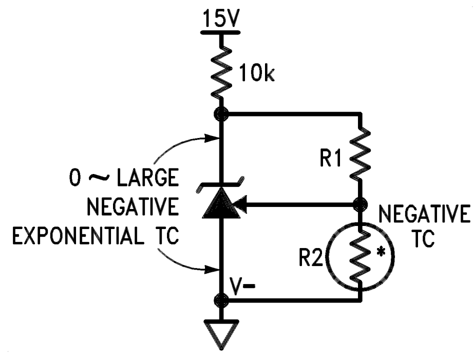


Figure 71. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

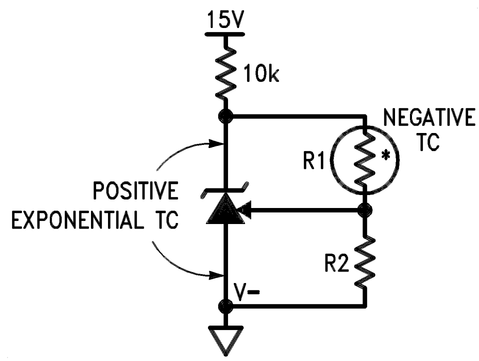


Figure 72. Output Voltage has Positive TC if R1 has Negative TC

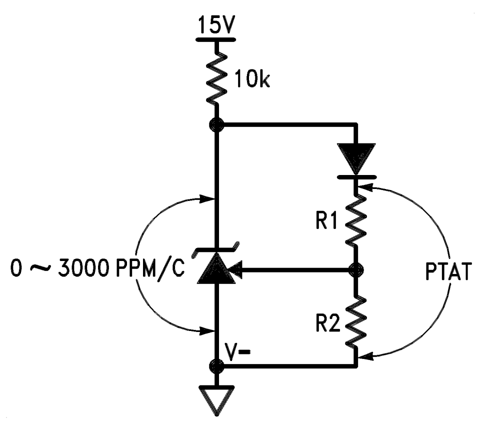
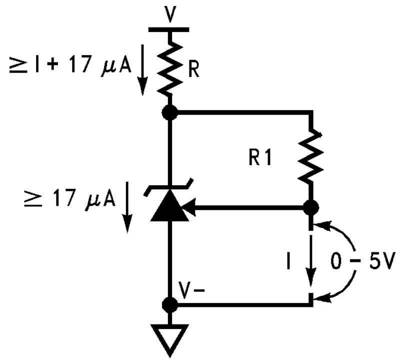


Figure 73. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



I = Vr/R1 = 1.24/R1

Figure 74. Current Source is Programmed by R1

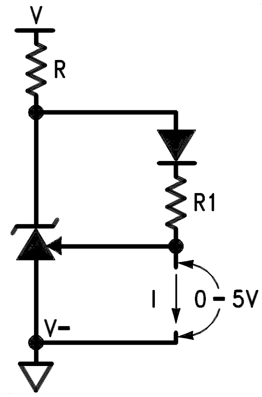


Figure 75. Proportional-to-Absolute-Temperature Current Source

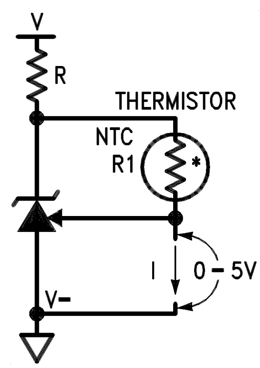


Figure 76. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary— always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts, see [1] in Electrical Characteristics. For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1. Output Swing: Unloaded, the 42 µA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 µA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2. Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3. Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 µA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 µA.

Op Amp and Comparator Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Typical Applications

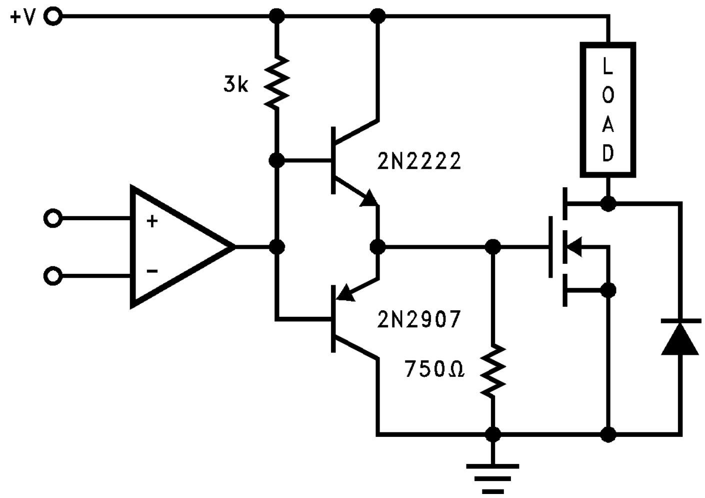


Figure 77. High Current, High Voltage Switch

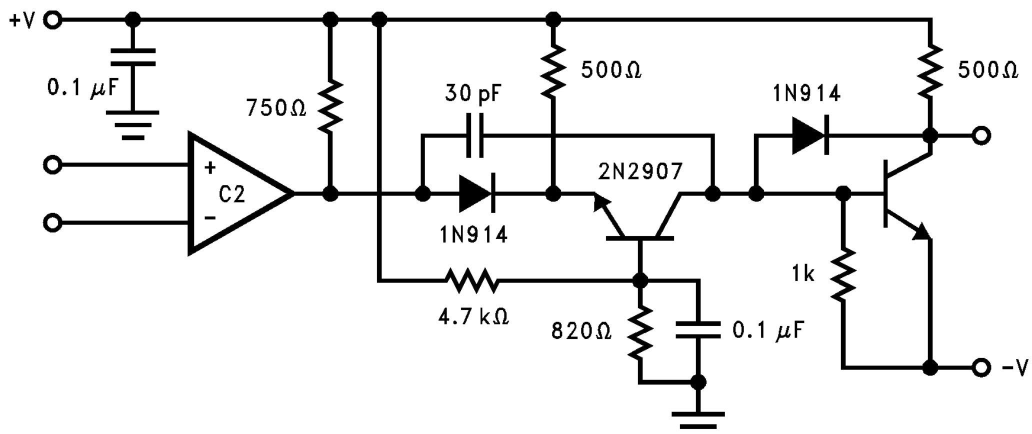
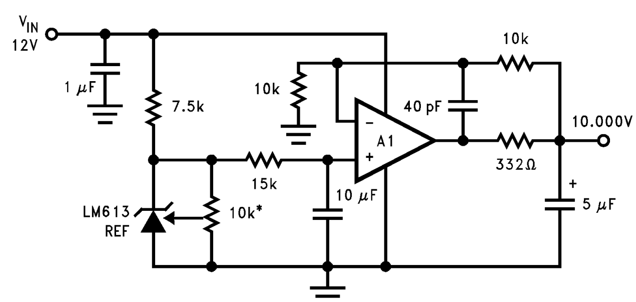


Figure 78. High Speed Level Shifter. Response Time is Approximately 1.5 µs, Where Output is Either Approximately +V or −V.



*10k must be low t.c. trimpot

Figure 79. Ultra Low Noise, 10.00V Reference. Total Output Noise is Typically 14 μV_{RMS}.

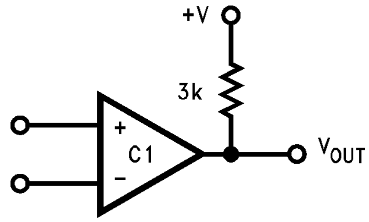


Figure 80. Basic Comparator

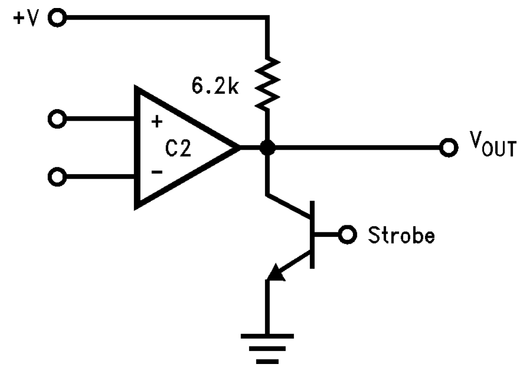


Figure 81. Basic Comparator with External Strobe

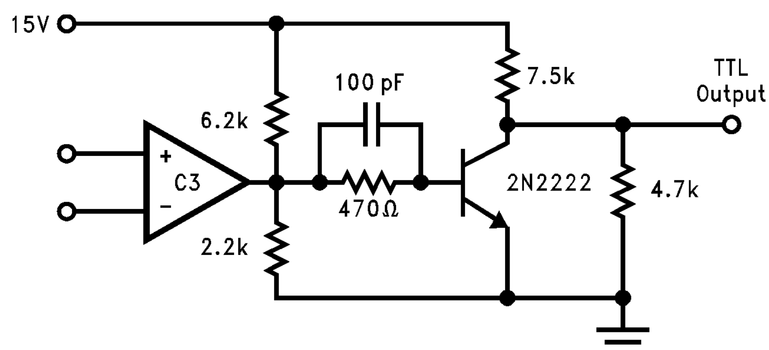


Figure 82. Wide-Input Range Comparator with TTL Output

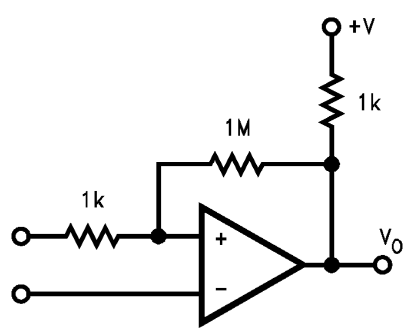


Figure 83. Comparator with Hysteresis (ΔV_H = $^+$V(1k/1M))

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM613IWM	LIFEBUY	SOIC	DW	16	45	TBD	Call TI	Call TI	-40 to 85	LM613IWM	
LM613IWM/NOPB	LIFEBUY	SOIC	DW	16	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LM613IWM	
LM613IWMX	LIFEBUY	SOIC	DW	16	1000	TBD	Call TI	Call TI	-40 to 85	LM613IWM	
LM613IWMX/NOPB	LIFEBUY	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LM613IWM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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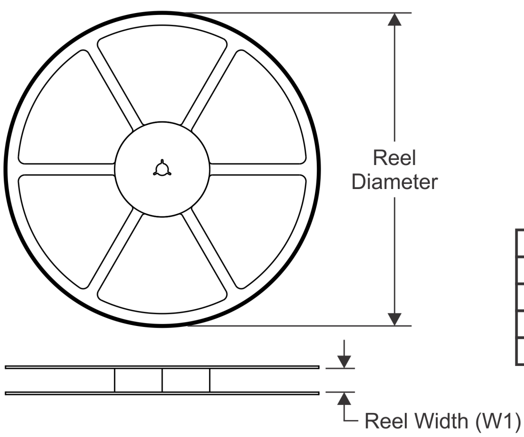
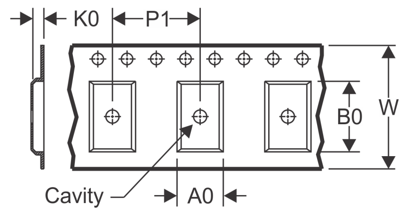
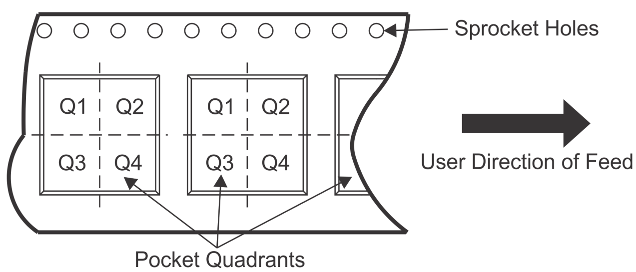
TAPE AND REEL INFORMATION





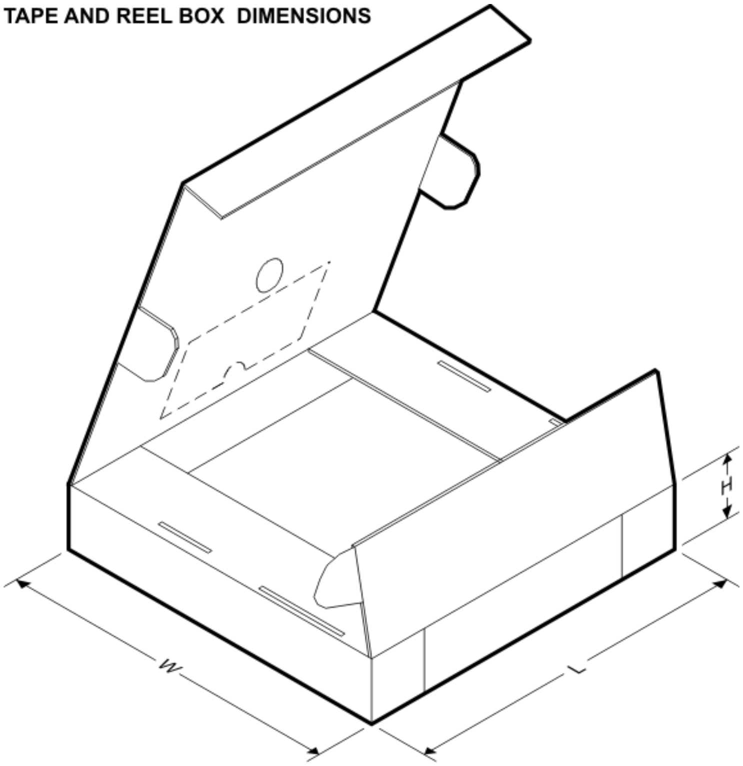
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM613IWMX	SOIC	DW	16	1000	330.0	16.4	10.9	10.7	3.2	12.0	16.0	Q1
LM613IWMX/NOPB	SOIC	DW	16	1000	330.0	16.4	10.9	10.7	3.2	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

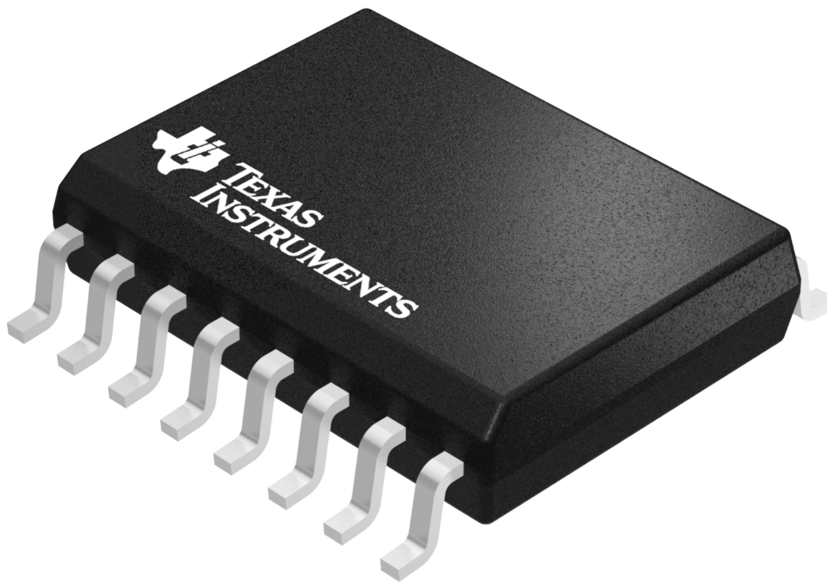


*All dimensions are nominal

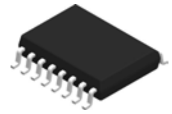
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM613IWMX	SOIC	DW	16	1000	367.0	367.0	38.0
LM613IWMX/NOPB	SOIC	DW	16	1000	367.0	367.0	38.0

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

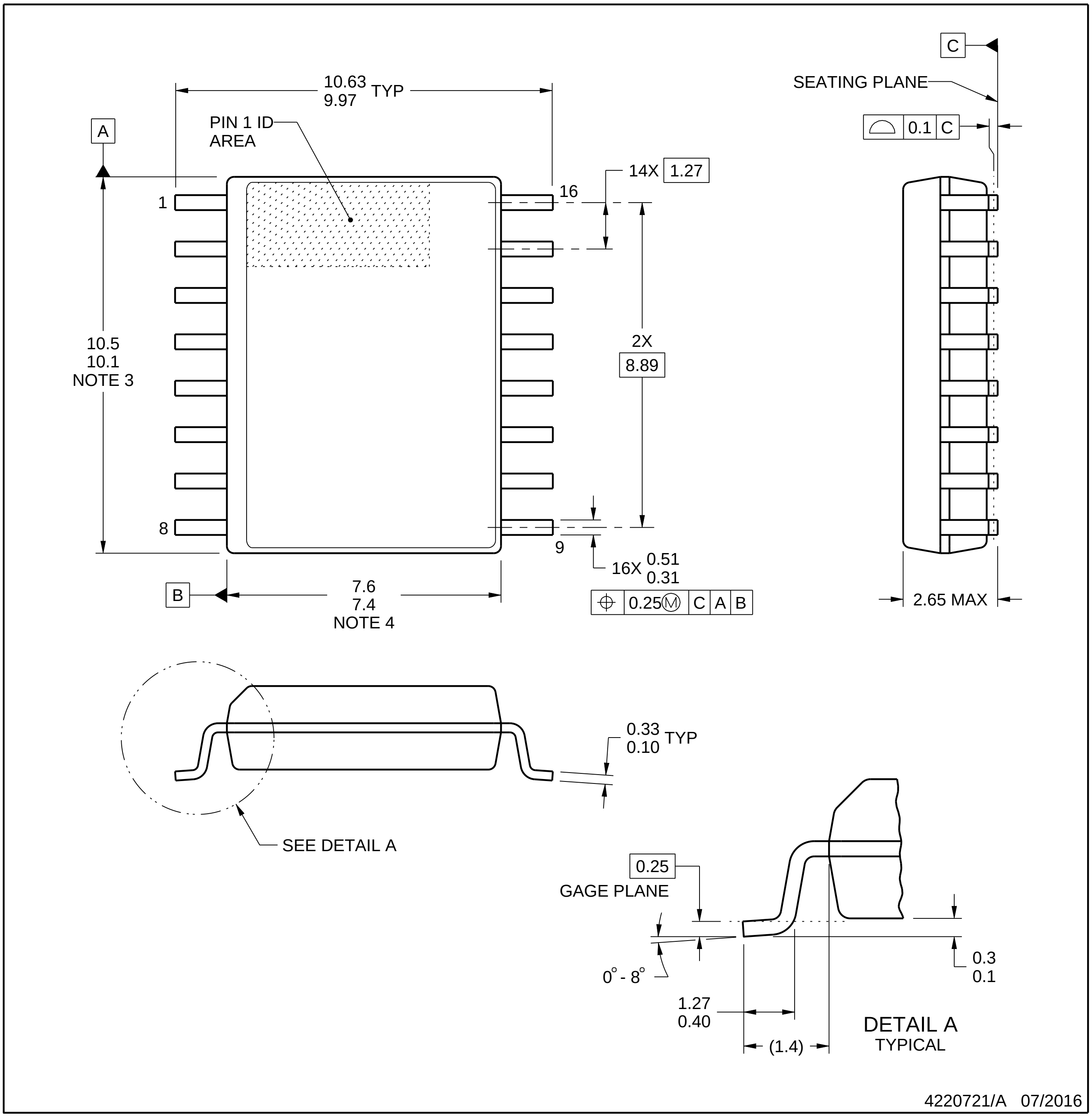


PACKAGE OUTLINE

DW0016A

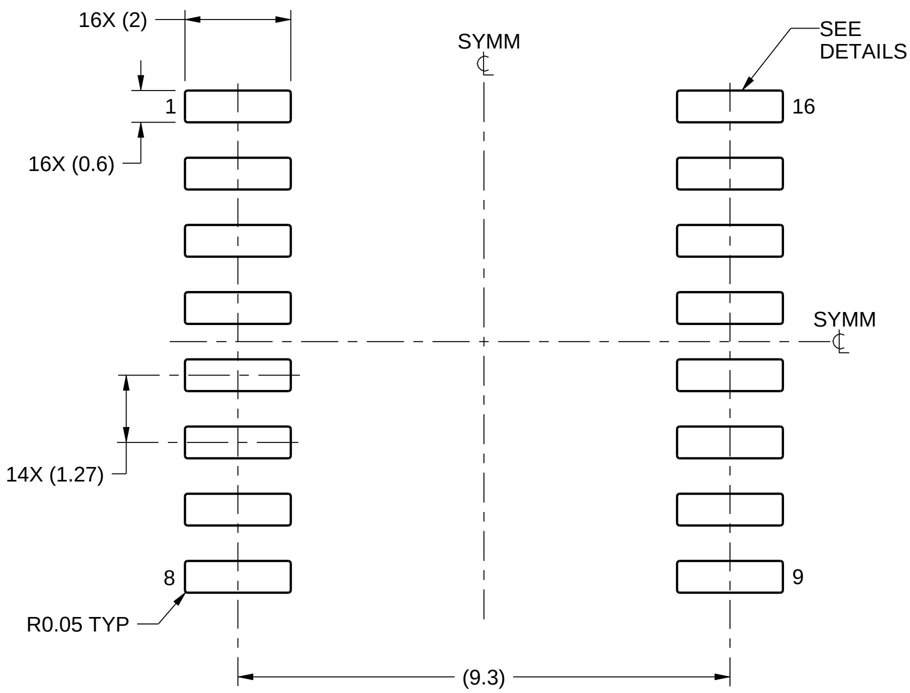
SOIC - 2.65 mm max height

SOIC

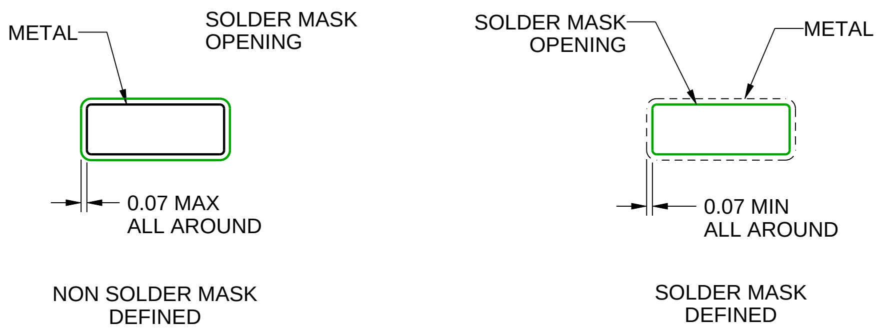


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

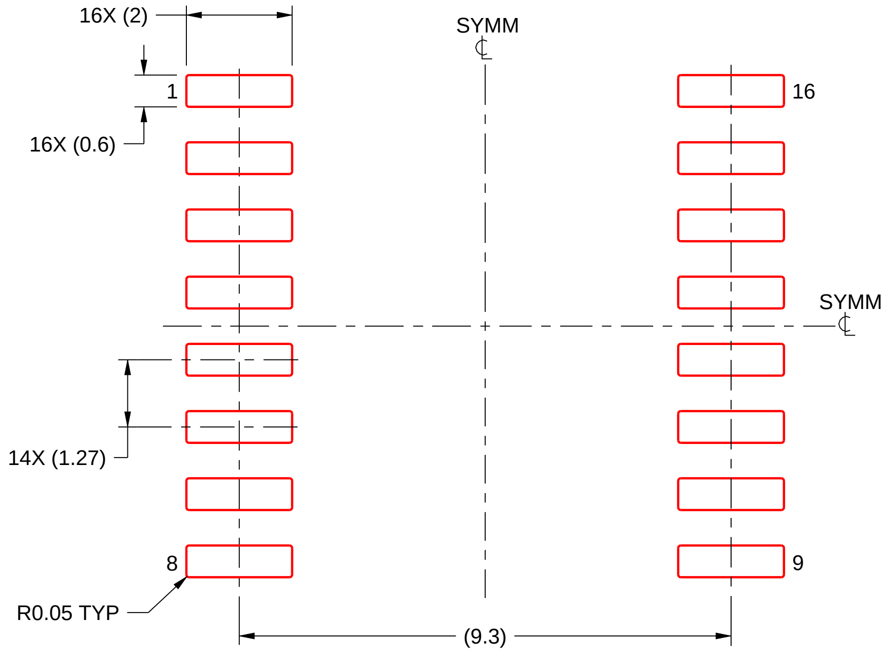


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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