MOTOROLA

Dual 1-of-4 Decoder/ Demultiplexer

ELECTRICALLY TESTED PER:
MIL-M-38510/32601

The 54LS155 is a high-speed Dual 1-of-4 Decode/Demultiplexer. The device has two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs.

The 'LS155 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process For High-Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diode Limits High-Speed Termination Effects

LOGIC DIAGRAM

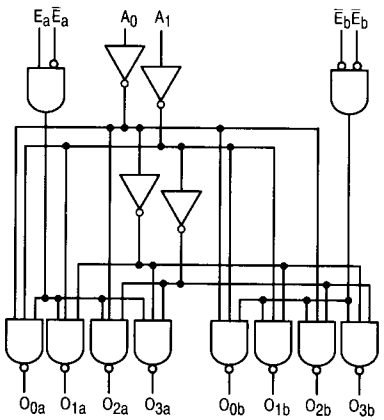
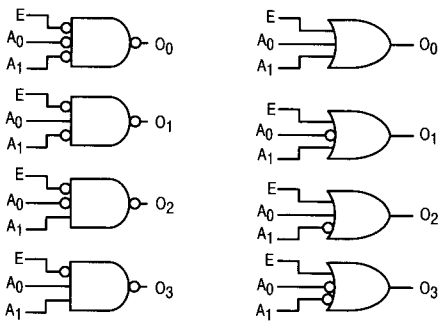


Figure a



Military 54LS155

AVAILABLE AS:

1) JAN: JM38510/32601BXA
2) SMD: N/A
3) 883: 54LS155/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
E_a	1	1	2	GND
$\bar{E}_a$	2	2	3	V_{CC}
A_1	3	3	4	V_{CC}
O_{3a}	4	4	5	V_{CC}
O_{2a}	5	5	7	V_{CC}
O_{1a}	6	6	8	V_{CC}
O_{0a}	7	7	9	V_{CC}
GND	8	8	10	GND
O_{0b}	9	9	12	V_{CC}
O_{1b}	10	10	13	V_{CC}
O_{2b}	11	11	14	V_{CC}
O_{3b}	12	12	15	V_{CC}
A_0	13	13	17	V_{CC}
$\bar{E}_b$	14	14	18	V_{CC}
$\bar{E}_b$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

Pin Names		Loading (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\bar{E}_a$, $\bar{E}_b$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\bar{O}_0$, $\bar{O}_3$	Active Low Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

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FUNCTIONAL DESCRIPTION

The 'LS155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \bullet \overline{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \bullet \overline{E}_b$). The 'LS155 can be used as a 1-of-8 Decoder/Demultiplexer by tying $\overline{E}_a$ to E_b and relabeling the common connection as (A_2). The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

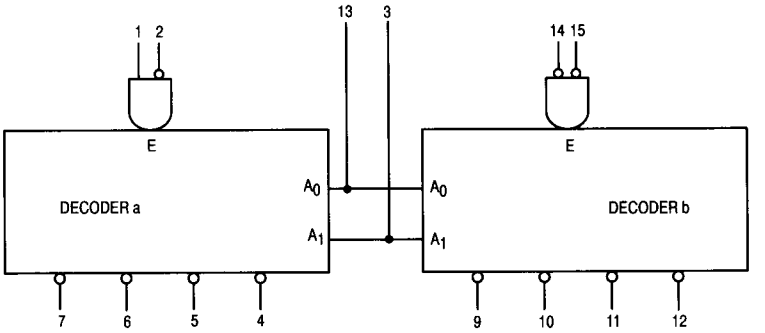
The LS155 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Figure a.

TRUTH TABLE

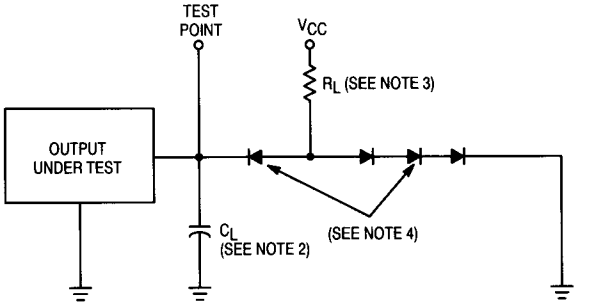
Address		Enable "a"		Output "a"				Enable "b"		Output "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	E_b	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC SYMBOL

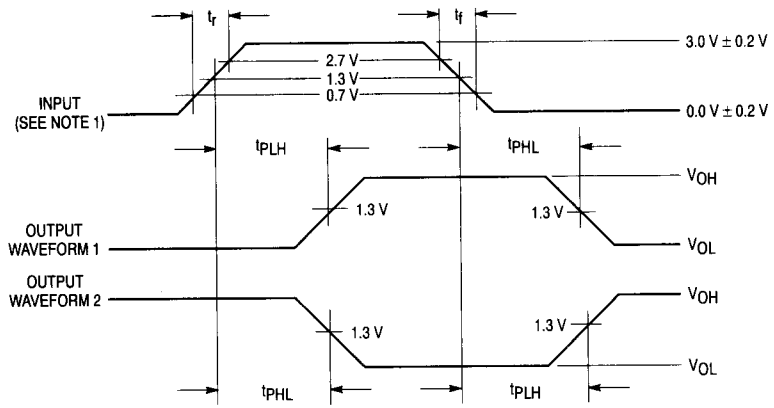


LOAD FOR OUTPUT UNDER TEST



REFERENCE NOTES ON PAGE 5-165

WAVEFORMS



Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −400 µA, V_{IH} = 2.0 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, $V_{IN(\overline{E}_b)}$ = 0.7 V, $\overline{E}_a$ = 2.0 V, $\overline{E}_a$ = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.12	−0.36	−0.12	−0.36	−0.12	−0.36	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, $V_{IN(\overline{E}_a)}$ = 5.5 V, all other inputs are open, V_{OUT} = GND.
I_{CC}	Power Supply Current		10		10		10	mA	V_{CC} = 5.5 V, $V_{IN(A_0,A_1,E_a)}$ = 4.5 V, other inputs = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:
1. The pulse generator has the following characteristics: PRR ≤ 1.0 MHz, t_r = 15 ns, t_f ≤ 6.0 ns.
2. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance without package in test fixture.
3. R_L = 2.0 kΩ ± 5.0%.
4. All diodes are 1N3064 or equivalent.
5. The limits specified for C_L = 15 pF are guaranteed but not tested.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output A_0 to Output	2.0 —	35 30	2.0 —	46 41	2.0 —	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output A_0 to Output	2.0 —	20 15	2.0 —	26 21	2.0 —	26 21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output A_1 to Output	2.0 —	35 30	2.0 —	46 41	2.0 —	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output A_1 to Output	2.0 —	20 15	2.0 —	26 21	2.0 —	26 21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL3} t_{PHL3}	Propagation Delay /Data-Output $\overline{E}_a$ to Output	2.0 —	35 30	2.0 —	46 41	2.0 —	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH3} t_{PLH3}	Propagation Delay /Data-Output $\overline{E}_a$ to Output	2.0 —	20 15	2.0 —	26 21	2.0 —	26 21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL4}	Propagation Delay /Data-Output $\overline{E}_b$ to Output	2.0	35	2.0	46	2.0	46	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH4}	Propagation Delay /Data-Output $\overline{E}_b$ to Output	2.0	20	2.0	26	2.0	26	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL5}	Propagation Delay /Data-Output $\overline{E}_b$ to Output	2.0	35	2.0	46	2.0	46	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH5}	Propagation Delay /Data-Output $\overline{E}_b$ to Output	2.0	20	2.0	26	2.0	26	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL6}	Propagation Delay /Data-Output A_1 to Output	2.0	35	2.0	46	2.0	46	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH6}	Propagation Delay /Data-Output A_1 to Output	2.0	31	2.0	40	2.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL7}	Propagation Delay /Data-Output A_0 to Output	2.0	35	2.0	46	2.0	46	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH7}	Propagation Delay /Data-Output A_0 to Output	2.0	31	2.0	40	2.0	40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL8}	Propagation Delay /Data-Output E_a to Output	2.0	33	2.0	43	2.0	43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH8}	Propagation Delay /Data-Output E_a to Output	2.0	32	2.0	42	2.0	42	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.