Integrated Circuit Systems, Inc.

ICS950818

Frequency Generator with 200MHz Differential CPU Clocks

Recommended Application:

CK-408 clock for Brookdale/Odem/Montara-GM for P4/Banias processor.

Output Features:

- 2 - Differential CPU Clock Pairs @ 3.3V
- 8 - PCI (3.3V) @ 33.3MHz including 2 1x/2x selectable PCI clocks
- 3 - PCI_F/PCI selectable (3.3V) @ 33.3MHz
- 1 - USB (3.3V) @ 48MHz, 1 DOT (3.3V) @ 48MHz
- 1 - REF (3.3V) @ 14.318MHz
- 4 - 3V66 (3.3V) @ 66.6MHz
- 1 - VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

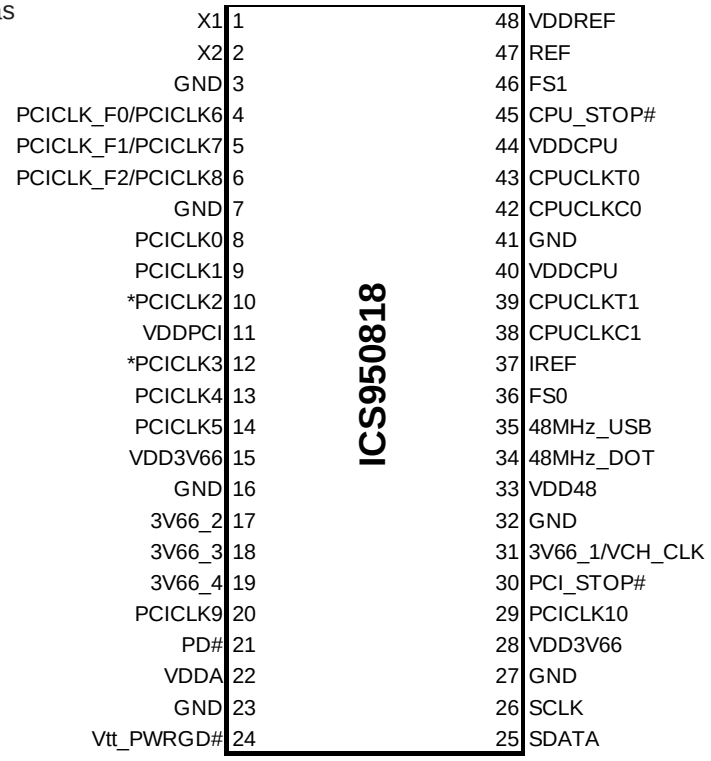
Features:

- Selectable 1X or 2X strength for REF and PCI via SMBus interface
- Programmable group to group skew
- Linear programmable frequency and spreading %
- Efficient power management scheme through PD#, CPU_STOP# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through SMBus interface.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

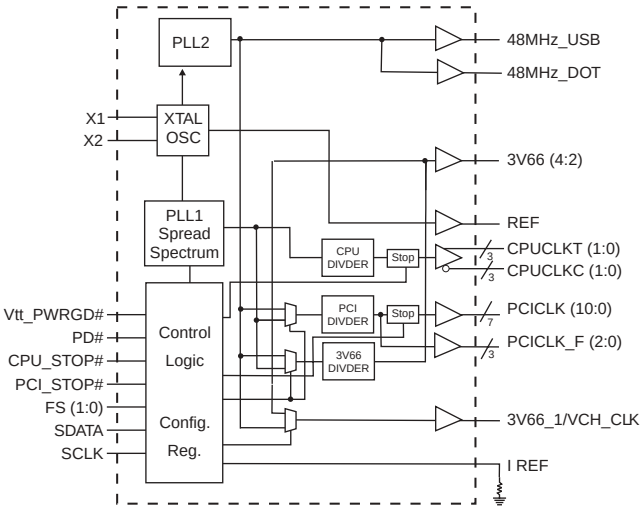
Pin Configuration



48-Pin 6.10 mm. Body, 0.50 mm. pitch TSSOP

*These outputs have selectable 1X/2X strength via SMBus

Block Diagram



Frequency Select Table 1

Freq Sel		CPU MHz	3V66(4:1) MHz	PCI MHz	REF MHz	USB/DOT MHz
FS 1	FS 0					
0	0	100.00	66.66	33.33	14.318	48.008
0	1	166.67	66.66	33.33	14.318	48.008
1	0	133.33	66.66	33.33	14.318	48.008
1	1	200.00	66.66	33.33	14.318	48.008

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	X1	IN	Crystal input, Nominally 14.318MHz.
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	GND	PWR	Ground pin.
4	PCICLK_F0/PCICLK6	OUT	Free running/Non-Free running PCI clock selected by SMBus.
5	PCICLK_F1/PCICLK7	OUT	Free running/Non-Free running PCI clock selected by SMBus.
6	PCICLK_F2/PCICLK8	OUT	Free running/Non-Free running PCI clock selected by SMBus.
7	GND	PWR	Ground pin.
8	PCICLK0	OUT	PCI clock output.
9	PCICLK1	OUT	PCI clock output.
10	*PCICLK2	OUT	PCI clock output.
11	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
12	*PCICLK3	I/O	PCI clock output.
13	PCICLK4	OUT	PCI clock output.
14	PCICLK5	OUT	PCI clock output.
15	VDD3V66	PWR	Power pin for the 3V66 clocks.
16	GND	PWR	Ground pin.
17	3V66_2	OUT	3.3V 66.66MHz clock output
18	3V66_3	OUT	3.3V 66.66MHz clock output
19	3V66_4	OUT	3.3V 66.66MHz clock output
20	PCICLK9	OUT	PCI clock output.
21	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped.
22	VDDA	PWR	3.3V power for the PLL core.
23	GND	PWR	Ground pin.
24	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input.

Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
26	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
27	GND	PWR	Ground pin.
28	VDD3V66	PWR	Power pin for the 3V66 clocks.
29	PCICLK10	OUT	PCI clock output.
30	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
31	3V66_1/VCH_CLK	OUT	3.3V 66.66MHz clock output / 48MHz VCH clock output.
32	GND	PWR	Ground pin.
33	VDD48	PWR	Power pin for the 48MHz output.3.3V
34	48MHz_DOT	OUT	48MHz clock output.
35	48MHz_USB	OUT	48MHz clock output.
36	FS0	IN	Frequency select pin.
37	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
38	CPUCLKC1	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
39	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
41	GND	PWR	Ground pin.
42	CPUCLKC0	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
45	CPU_STOP#	IN	Stops all CPUCLK besides the free running clocks
46	FS1	IN	Frequency select pin.
47	REF	OUT	14.318 MHz reference clock.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V

Power Supply

Pin Number		Description
VDD	GND	
48	3	Xtal, Ref
11	7	PCICLK outputs
15, 28	16, 27	3V66
22	23	Master clock, CPU Analog
33	32	48MHz, Fix Digital, Fix Analog
	41	Inputs
40, 44	41	CPUCLK clocks

Default Setup of Byte 11-17

CPU (MHz)	SS%	Bytes						
		11	12	13	14	15	16	17
100.00	0	8E	B7	F8	17	94	95	0F
100.00	0 to -0.5%	8D	9A	F2	17	94	95	0F
100.00	0 to -1%	90	ED	EE	17	94	95	0F
100.00	+/- 0.25%	8E	B7	0A	18	94	95	0F
100.00	+/- 0.50%	8E	B7	06	18	94	95	0F
100.00	+/- 1.0%	8E	B7	15	18	94	95	0F

CPU (MHz)	SS%	Bytes						
		11	12	13	14	15	16	17
166.66	0	87	9B	F8	27	A4	A6	0F
166.66	0 to -0.5%	87	9A	EE	27	A4	A6	0F
166.66	0 to -1%	86	6B	E5	27	A4	A6	0F
166.66	+/- 0.25%	87	9B	15	28	A4	A6	0F
166.66	+/- 0.50%	87	9B	10	28	A4	A6	0F
166.66	+/- 1.0%	87	9B	28	28	A4	A6	0F

CPU (MHz)	SS%	Bytes						
		11	12	13	14	15	16	17
133.33	0	86	22	F9	1F	C4	C8	0F
133.33	0 to -0.5%	8B	DB	F0	1F	C4	C8	0F
133.33	0 to -1%	87	46	EB	1F	C4	C8	0F
133.33	+/- 0.25%	86	22	10	20	C4	C8	0F
133.33	+/- 0.50%	86	22	0C	20	C4	C8	0F
133.33	+/- 1.0%	86	22	1F	20	C4	C8	0F

CPU (MHz)	SS%	Bytes						
		11	12	13	14	15	16	17
200.00	0	86	B7	FB	2F	D4	D9	0F
200.00	0 to -0.5%	86	B6	F0	2F	D4	D9	0F
200.00	0 to -1%	84	46	E4	2F	D4	D9	0F
200.00	+/- 0.25%	86	B7	1D	30	D4	D9	0F
200.00	+/- 0.50%	86	B7	17	30	D4	D9	0F
200.00	+/- 1.0%	86	B7	34	30	D4	D9	0F

BYTE 0	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	Spread Enabled	Spread Spectrum Control	RW	OFF	ON	0
Bit 6	-	CPUCLKT(1:0)	Power down mode output level 0= CPU driven in power down 1= undriven	RW	x2 IREF	Hi-Z	0
Bit 5	31	3V66_1/VCH_CLK	VCH/66.66 Select	RW	66.66	48.00	0
Bit 4	44	CPU_STOP#	Reflects value of pin	R	Stop	Active	X
Bit 3	30	PCI_STOP#	Reflects value of pin at power up. Also can be set.	RW	Stop	Active	X
Bit 2	-	-	(Reserved)	R	-	-	X
Bit 1	46	FS1	Frequency Selection	R	-	-	X
Bit 0	36	FS0	Frequency Selection	R	-	-	X

Note: For PCI_STOP# function, refer to table 2.

BYTE 1	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(Reserved)	R	-	-	X
Bit 6	-	CPUCLKT(1:0)	CPU_Stop mode output level 0= CPU driven when stopped 1 = undriven	RW	x2 IREF	Hi-Z	0
Bit 5	39, 38	CPUCLKT1, CPUCLKC1 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 4	43, 42	CPUCLKT0, CPUCLKC0 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 3	-	-	(Reserved)	R	-	-	X
Bit 2	39, 38	CPUCLKT1, CPUCLKC1	Output control	RW	Disable	Enable	1
Bit 1	43, 42	CPUCLKT0, CPUCLKC0	Output control	RW	Disable	Enable	1
Bit 0	-	-	(Reserved)	R	-	-	X

Note: CPUCLK(1:0) can be turned on/off by CPU_STOP#. Refer to table 3.

BYTE 2	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	47	REF	1X or 0.5X Strength control	RW	1X	0.5X	0
Bit 6	14	PCICLK5	Output control	RW	Disable	Enable	1
Bit 5	13	PCICLK4	Output control	RW	Disable	Enable	1
Bit 4	12	*PCICLK3	Output control	RW	Disable	Enable	1
Bit 3	-	-	Reserved	X	-	-	1
Bit 2	10	*PCICLK2	Output control	RW	Disable	Enable	1
Bit 1	9	PCICLK1	Output control	RW	Disable	Enable	1
Bit 0	8	PCICLK0	Output control	RW	Disable	Enable	1

Note: PCICLK(5:0) can be turned on/off by PCI_STOP#. Refer to table 2.

BYTE 3	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	34	48MHz_DOT	Output control	RW	Disable	Enable	1
Bit 6	35	48MHz_USB	Output control	RW	Disable	Enable	1
Bit 5	6	PCICLK_F2/PCICLK8 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 4	5	PCICLK_F1/PCICLK7 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 3	4	PCICLK_F0/PCICLK6 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 2	6	PCICLK_F2/PCICLK8	Output control	RW	Disable	Enable	1
Bit 1	5	PCICLK_F1/PCICLK7	Output control	RW	Disable	Enable	1
Bit 0	4	PCICLK_F0/PCICLK6	Output control	RW	Disable	Enable	1

Note: PCICLK_F(2:0) can be turned on/off by PCI_STOP#. Refer to table 4.

BYTE 4	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	10	*PCICLK2	Output strength (1X/2X)	R/W	2X	1X	1
Bit 6	12	*PCICLK3	Output strength (1X/2X)	R/W	2X	1X	1
Bit 5	29	PCICLK10	Output control	RW	Disable	Enable	1
Bit 4	31	3V66_1/VCH_CLK	Output control	RW	Disable	Enable	1
Bit 3	20	PCICLK9	Output control	RW	Disable	Enable	1
Bit 2	19	3V66_4	Output control	RW	Disable	Enable	1
Bit 1	18	3V66_3	Output control	RW	Disable	Enable	1
Bit 0	17	3V66_2	Output control	RW	Disable	Enable	1

BYTE 5	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	PD Mode Iref Mirror Enable	Allow Iref Mirror to be ON during Power Down Mode	RW	OFF	ON	0
Bit 6	X	Reserved	Reserved	X	-	-	0
Bit 5	X	3V66(4:2) (See table 6)	Allow control of output with assertion of CPU_STOP#.	X	Freerun	Not Freerun	0
Bit 4	X	3V66(1) (See table 7)	Allow control of output with assertion of CPU_STOP#.	X	Freerun	Not Freerun	0
Bit 3	34	48MHz_DOT Slew Control	00 = Medium (default), 01 = Low, 11,10 =High	RW	-	-	0
Bit 2				RW	-	-	0
Bit 1	35	48MHz_USB Slew Control	00 = Medium (default), 01 = Low, 11,10 =High	RW	-	-	0
Bit 0				RW	-	-	0

Note: Functions in Byte 5 of CK408 were intended as a test and debug byte only.

BYTE 6	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	Revision ID Bit 3	Revision ID Value Based on Device Revision	R	-	-	0
Bit 6	X	Revision ID Bit 2		R	-	-	0
Bit 5	X	Revision ID Bit 1		R	-	-	0
Bit 4	X	Revision ID Bit 0		R	-	-	0
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	0
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	0
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	0
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

BYTE 7	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	X	-	-	0
Bit 6	X	-	(Reserved)	X	-	-	0
Bit 5	X	-	(Reserved)	X	-	-	0
Bit 4	X	-	(Reserved)	X	-	-	0
Bit 3	X	-	(Reserved)	X	-	-	1
Bit 2	X	-	(Reserved)	X	-	-	1
Bit 1	X	-	(Reserved)	X	-	-	1
Bit 0	X	-	(Reserved)	X	-	-	0

BYTE 8	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	X	-	-	0
Bit 6	X	-	(Reserved)	X	-	-	0
Bit 5	X	-	(Reserved)	X	-	-	0
Bit 4	X	-	(Reserved)	X	-	-	0
Bit 3	X	-	Readback Byte Count	R	-	-	1
Bit 2	X	-		R	-	-	1
Bit 1	X	-		R	-	-	1
Bit 0	X	-		R	-	-	1

Note: Byte 8 is for ICS test only. Do not write as system damage may occur. Bit(3:0) contain the readback Byte count.

BYTE 9	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	X	-	-	0
Bit 6	X	-	(Reserved)	X	-	-	0
Bit 5	X	-	(Reserved)	X	-	-	0
Bit 4	X	-	(Reserved)	X	-	-	0
Bit 3	X	-	(Reserved)	X	-	-	0
Bit 2	X	-	(Reserved)	X	-	-	0
Bit 1	X	-	(Reserved)	X	-	-	0
Bit 0	X	-	(Reserved)	X	-	-	0

BYTE 10	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	M/N Enable (Enable access to Byte 11 - 14)	RW	HW/B0	Byte (11-14)	0
Bit 6	X	-	(Reserved)	X	-	-	0
Bit 5	X	-	(Reserved)	X	-	-	1
Bit 4	X	-	(Reserved)	X	-	-	1
Bit 3	X	-	(Reserved)	X	-	-	1
Bit 2	X	-	(Reserved)	X	-	-	1
Bit 1	X	-	(Reserved)	X	-	-	1
Bit 0	X	-	(Reserved)	X	-	-	0

BYTE 11	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	VCO Divider Bit8	RW	-	-	X
Bit 6	X	-	REF Divider Bit6	RW	-	-	X
Bit 5	X	-	REF Divider Bit5	RW	-	-	X
Bit 4	X	-	REF Divider Bit4	RW	-	-	X
Bit 3	X	-	REF Divider Bit3	RW	-	-	X
Bit 2	X	-	REF Divider Bit2	RW	-	-	X
Bit 1	X	-	REF Divider Bit1	RW	-	-	X
Bit 0	X	-	REF Divider Bit0	RW	-	-	X

Note: The decimal representation of these 7 bits (Byte 11 bit[6:0]) + 2 is equal to the REF divider value.

BYTE 12	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	VCO Divider Bit7	RW	-	-	X
Bit 6	X	-	VCO Divider Bit6	RW	-	-	X
Bit 5	X	-	VCO Divider Bit5	RW	-	-	X
Bit 4	X	-	VCO Divider Bit4	RW	-	-	X
Bit 3	X	-	VCO Divider Bit3	RW	-	-	X
Bit 2	X	-	VCO Divider Bit2	RW	-	-	X
Bit 1	X	-	VCO Divider Bit1	RW	-	-	X
Bit 0	X	-	VCO Divider Bit0	RW	-	-	X

Note: The decimal representation of these 9 bits (Byte 12 bit[7:0]) and Byte 11 bit [7]) + 8 is equal to the VCO divider value.

BYTE 13	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	Spread Spectrum Bit7	RW	-	-	X
Bit 6	X	-	Spread Spectrum Bit6	RW	-	-	X
Bit 5	X	-	Spread Spectrum Bit5	RW	-	-	X
Bit 4	X	-	Spread Spectrum Bit4	RW	-	-	X
Bit 3	X	-	Spread Spectrum Bit3	RW	-	-	X
Bit 2	X	-	Spread Spectrum Bit2	RW	-	-	X
Bit 1	X	-	Spread Spectrum Bit1	RW	-	-	X
Bit 0	X	-	Spread Spectrum Bit0	RW	-	-	X

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

BYTE 14	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	RW	-	-	X
Bit 6	X	-	(Reserved)	RW	-	-	X
Bit 5	X	-	Spread Spectrum Bit13	RW	-	-	X
Bit 4	X	-	Spread Spectrum Bit12	RW	-	-	X
Bit 3	X	-	Spread Spectrum Bit11	RW	-	-	X
Bit 2	X	-	Spread Spectrum Bit10	RW	-	-	X
Bit 1	X	-	Spread Spectrum Bit9	RW	-	-	X
Bit 0	X	-	Spread Spectrum Bit8	RW	-	-	X

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Table 2
PCI_STOP# SMBus Control Table-Byte 0, Bit 3

PCI_STOP# (Pin 30)	Byte 0 Bit 3 Write Bit	Byte 0, Bit 3 Read Bit (Internal Status)
0	0	0
0	1	0
1	0	0
1	1	1`

Note: When this Byte 0, Bit 3 is low (0), all PCI clocks are stopped.

Table 3
CPUCLKT/C (1:0) Outputs SMBus Control Table

CPU_STOP# (Pin 45)	Byte 1 Bit 4, 5	CPUCLKT/C (1:0) Outputs
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Note: Individual CPUCLK outputs are controlled by Byte 1, Bit 4, and 5.

Table 4
PCICLK_F (2:0) Outputs SMBus Control Table

PCI_STOP# (Pin 30)	Byte 3 Bit 3, 4, 5	PCICLK (2:0) Outputs
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Note: Individual PCICLK outputs are controlled by Byte 3, Bit 3, 4, and 5.

Table 5
3V66 (4:2) SMBus Control Table

CPU_STOP# (Pin 45)	Byte 5 Bit 5	3V66 (4:2)
0	0	Running
0	1	Stopped
1	0	Running
1	1	Running

Note: Activating Byte 5, Bit 5 will allow CPU_STOP# to control stop of pins 17, 18, and 19

Table 6
3V66 (1) SMBus Control Table

CPU_STOP# (Pin 45)	Byte 5 Bit 4	3V66 (1)
0	0	Running
0	1	Stopped
1	0	Running
1	1	Running

Note: Activating Byte 5, Bit 4 will allow CPU_STOP# to control stop of pins 31.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +90°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 90°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}; Inputs with no pull-down resistors			5.75	mA
	I_{IH}	V_{IN} = V_{DD}; Inputs with pull-down resistors			200	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5.75			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz		182	280	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz		189	280	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=5 mA		14	52	mA
	$I_{DD3.3PDHIz}$			9	0.5	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.32		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.			2.1	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		12	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		12	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

Electrical Characteristics - CPU (0.7V Select) 100MHz

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000	-		Ω
Average Period	T_{PERIOD}	Fig. 1	10.00	10.02	10.20	ns
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	757.1	850	mV
Voltage Low	VLow		-150	9.067	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		774.7	1150	mV
Min Voltage	Vuds		-450	3		
Crossing Voltage (abs)	Vcross(abs)	Fig. 3	250	386.1	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges (Fig. 4)		41.57	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V (Fig. 3)	175	552.8	810	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V (Fig. 3)	175	558.7	810	ps
Rise Time Variation	d-t_r			34.25	125	ps
Fall Time Variation	d-t_f			45.5	125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom (Fig 1)	45	50.58	55	%
Skew	t_{sk3}	V_T = 50%		60.5	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50% (Fig. 1)		65.25	175	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU (0.7V Select) 133.33MHz

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000	-		Ω
Average Period	T_{PERIOD}	Fig. 1	7.50	7.58	7.65	ns
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	757	850	mV
Voltage Low	VLow		-150	9	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		775	1150	mV
Min Voltage	Vuds		-450	3		
Crossing Voltage (abs)	Vcross(abs)	Fig. 3	250	386	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges (Fig. 4)		42	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V (Fig. 3)	175	553	810	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V (Fig. 3)	175	559	810	ps
Rise Time Variation	d-t_r			34	125	ps
Fall Time Variation	d-t_f			46	125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom (Fig 1)	45	51	55	%
Skew	t_{sk3}	V_T = 50%		61	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50% (Fig. 1)		65	175	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	64.50	65	Ω
Average Period	T_{PERIOD}	Fig. 8	15.00	15.01	15.30	ns
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05	3.24		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.06	0.65	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V		-90	-33	mA
		V_{OH} = 3.135 V	-33	-14		
Output Low Current	I_{OL}[1]	V_{OL} = 1.95 V	26	35		
		V_{OL} = 0.4 V		103	38	
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.74	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.45	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	52.05	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		13.50	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		158.75	290	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}	Fig. 8		48.008		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	52.50	70	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05	3.24		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.06	0.5	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V		-53	-29	mA
		V_{OH} = 3.135 V	-20	-7		
Output Low Current	I_{OL}[1]	V_{OL} = 0.4 V		21	27	mA
		V_{OL} 1.95 V	25	60		
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	0.86	1.15	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	0.86	1.15	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	1	1.37	2.3	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	1	1.37	2.3	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	51.10	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	52.80	55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		182.63	410	ps
USB to DOT Skew	t_{sk1}[1]	V_T = 1.5 V (0 OR 180 degrees)		0.13	1	ns
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		153.25	410	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F, PCICLK 1X

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	52.50	65	Ω
Average Period	T_{PERIOD}	Fig. 8	30.00	30.03		ns
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05	3.24		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.06	0.65	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V		-90	-33	mA
		V_{OH} = 3.135 V	-33	-14		
Output Low Current	I_{OL}[1]	V_{OL} = 1.95 V	26	35		
		V_{OL} = 0.4 V		103	38	
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.79	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.82	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	51.57	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		136.00	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		151.5	290	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK (3:2) 2X

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$		52.5		Ω
Average Period	T_{PERIOD}	Fig. 8		30.03		ns
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA		3.24	2.7	V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA	0.4	0.06		V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V		-100	-60	mA
		V_{OH} = 3.135 V	-28	-17		
Output Low Current	I_{OL}[1]	V_{OL} = 1.95 V		44	60	
		V_{OL} = 0.4 V	26	100		
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.75	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.80	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	51.95	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		136	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		151.5	290	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF (1X select)

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}	Fig. 8		14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	52.50	70	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05	3.24		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.06	0.45	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V		-70	-29	mA
		V_{OH} = 3.135 V	-25	-12		
Output Low Current	I_{OL}[1]	V_{OL} = 0.4 V		30	38	
		V_{OL} 1.95 V	26	60		
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	1	-	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	1	1.98	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.50	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		242	1200	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF (2X select)

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 20-40 pF (unless otherwise specified)

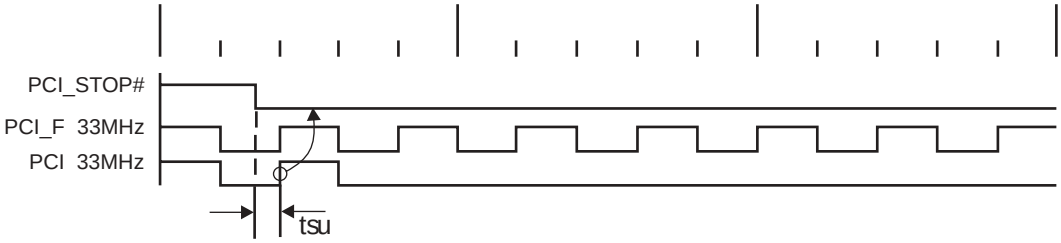
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}	Fig. 8		14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$		52.5		Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.7	3.24		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.06	0.4	V
Output High Current	I_{OH}[1]	V_{OH} = 1.0 V		-100	-60	mA
		V_{OH} = 3.135 V	-28	-17		
Output Low Current	I_{OL}[1]	V_{OL} = 0.4 V		44	60	
		V_{OL} 1.95 V	26	100		
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	1	-	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	1	1.98	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.70	55	%
Jitter	$t_{icyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		242	1200	ps

[1]Guaranteed by design, not 100% tested in production.

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[10:0] and stoppable PCI_F clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

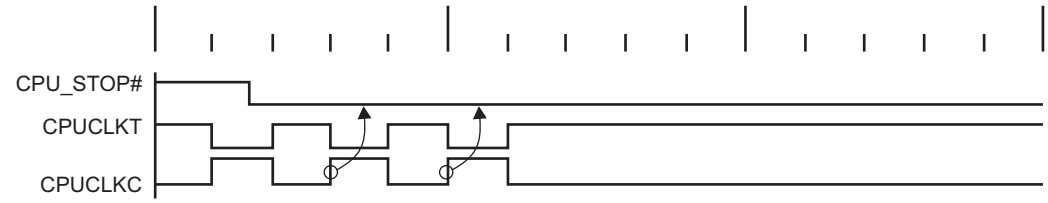
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the SMBus configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition. When the SMBus Bit 6 of Byte 1 is programmed to '0' the final state of the stopped CPU signals is CPU = High and CPU# = Low. There is to be no change to the output drive current values. The CPU will be driven high with a current value equal to (Mult 0 'select') x (Iref), the CPU# signal will not be driven . When the SMBus Bit 6 of Byte 1 is programmed to '1' then final state of the stopped CPU signals is Low, both CPU and CPU# outputs will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float

Group to Group Skews at Common Transition Edges: Unbuffered Mode

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66 to PCI[1,2]	$S_{3V66-PCI}$	3V66 (4:1) leads 33MHz PCI	1.5	2.765	3.5	ns

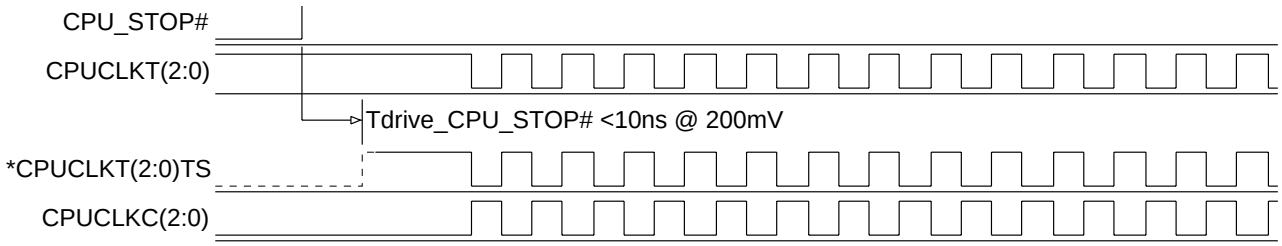
[1]Guaranteed by design, not 100% tested in production.

[2]500ps Tolerance

CPU_STOP# - De-assertion (transition from logic "0" to logic "1")

All CPU outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is to be defined to be between 2 - 6 CPU clock periods (2 clocks are shown). If the SMBus Bit 6 of Byte 1 is programmed to "1" then the stopped CPU outputs will be driven High within 10 nS of CPU_Stop# de-assertion.

De-assertion of CPU_STOP# Waveforms

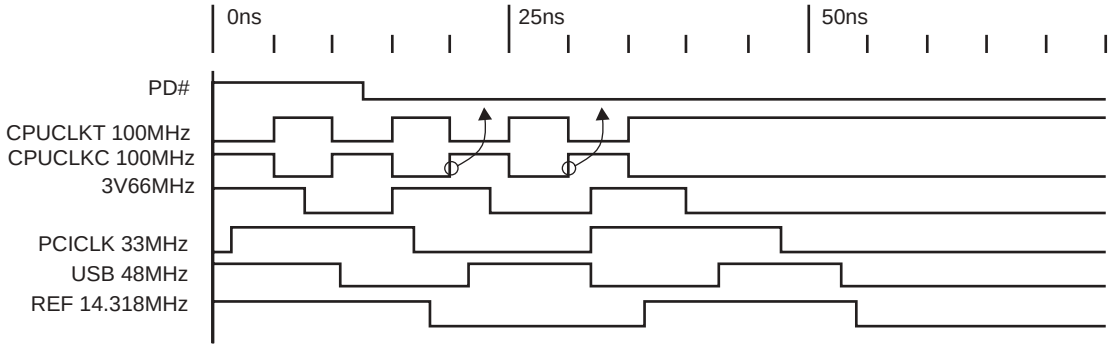


*Signal TS is CPUCLKT in Tri-State mode

PD# - Assertion (transition from logic "1" to logic "0")

When PWRDWN# is sampled low by two consecutive rising edges of CPU clock, then all clock outputs except CPU clocks must be held low on their next high to low transitions. When the SMBUS Bit 6 of Byte 0 is programmed to '0' CPU clocks must be held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# undriven. If Bit 6 of Byte 0 is '1' then both CPU and CPU# are undriven. Note the example below shows CPU = 133 MHz and Bit 6 of Byte 0 = '0', this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200 MHz.
Due to the state if the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms

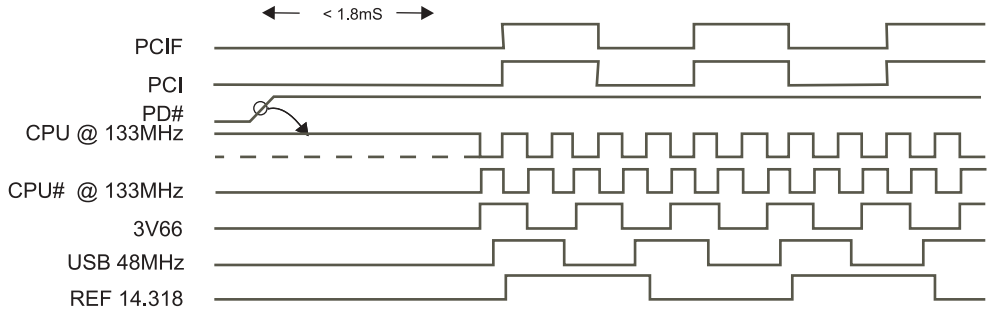


PD# Functionality

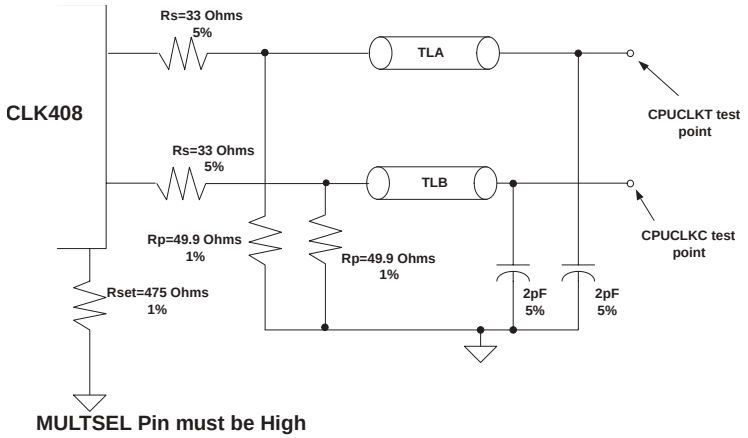
PD#	CPUCLKT	CPUCLKC	3V66	PCICLK_F PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	33MHz	48MHz
0	iref * Mult	Float	Low	Low	Low

Power Down De-Assertion Mode

The power-up latency needs to be less than 1.8mS. this is the time from the de-asseration of the powerdown of the ramping of the power supply until the time that stable clocks are output from the clock chip. If the SMBus Bit 6 of Byte 0 is programmed to "1" then the stopped CPU outputs will be driven high within 3 nS of PD# de-asseration.



Test Configuration Diagram



CPU 0.7V Configuration test load board termination

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

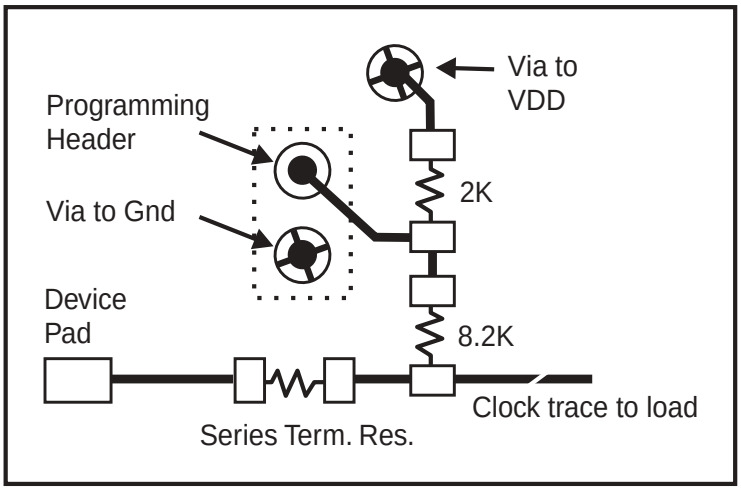
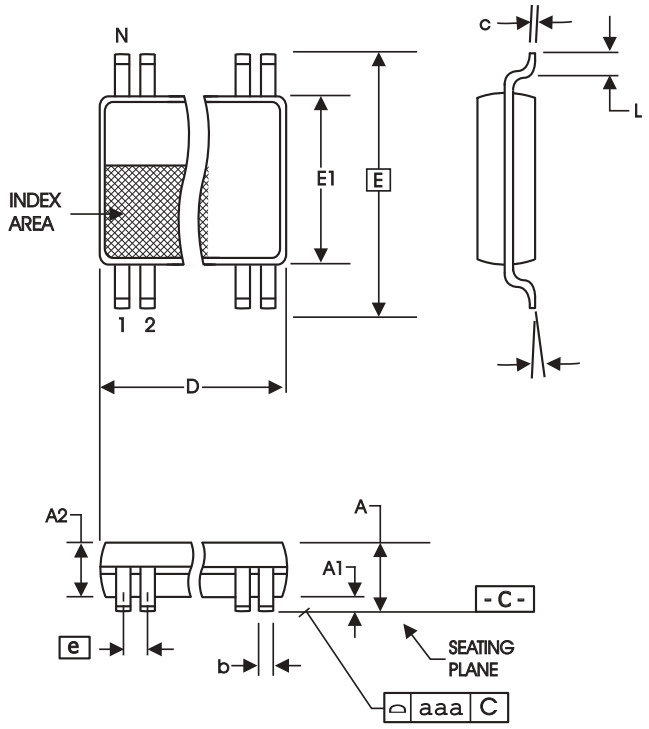


Fig. 1



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS950818yGT

Example:

ICS95 XXXX y G - T

Designation for tape and reel packaging

Package Type
G=TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS, AV = Standard Device

0825F—11/19/03