Ultra Low Power/High Speed CMOS SRAM
256K X 16 bit
BS616LV4016

n FEATURES

- Wide V_{CC} operation voltage : 2.4V ~ 3.6V
- Very low power consumption :
  - V_{CC} = 3.0V C-grade : 25mA(@55ns) operating current
  - I-grade : 27mA(@55ns) operating current
  - C-grade : 17mA(@70ns) operating current
  - I-grade : 18mA(@70ns) operating current
  - 0.45uA (Typ.) CMOS standby current
- High speed access time :
  - -55 55ns (Max.) at V_{CC}=2.7~3.6V/85^{O}C
  - -70 70ns (Max.) at V_{CC}=2.4~3.6V/85^{O}C
- Automatic power down when chip is deselected
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options
- I/O Configuration x8/x16 selectable by $\overline{LB}$ and $\overline{UB}$ pin.
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V

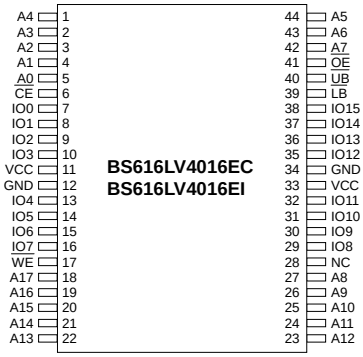
n DESCRIPTION

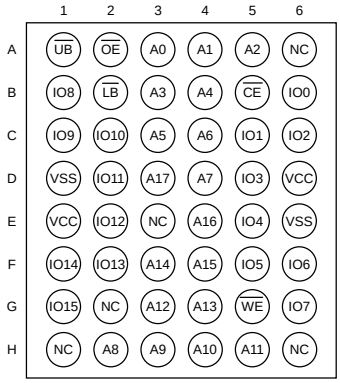
The BS616LV4016 is a high performance, very low power CMOS Static Random Access Memory organized as 262,144 words by 16 bits and operates form a wide range of 2.4V to 3.6V supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical CMOS standby current of 0.45uA at 3.0V/25^{O}C and maximum access time of 55ns at 2.7V/85^{O}C.
Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state output drivers.
The BS616LV4016 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The BS616LV4016 is available in DICE form, JEDEC standard 44-pin TSOP Type II and 48-ball BGA package.

n PRODUCT FAMILY

PRODUCT FAMILY	OPERATING TEMPERATURE	V_{CC} RANGE	SPEED (ns)	POWER DISSIPATION			PKG TYPE
				STANDBY (I_{CCSB1}, Max)	Operating (I_{CC}, Max)		
			55ns : 2.7~3.6V 70ns : 2.4~3.6V	V_{CC}=3.0V	V_{CC}=3.0V		
					55ns	70ns	
BS616LV4016DC	+0^{O}C to +70^{O}C	2.4V ~ 3.6V	55/70	6.0uA	25mA	17mA	DICE
BS616LV4016EC							TSOP2-44
BS616LV4016AC							BGA-48-0608
BS616LV4016DI	-40^{O}C to +85^{O}C	2.4V ~ 3.6V	55/70	8.0uA	27mA	18mA	DICE
BS616LV4016EI							TSOP2-44
BS616LV4016AI							BGA-48-0608

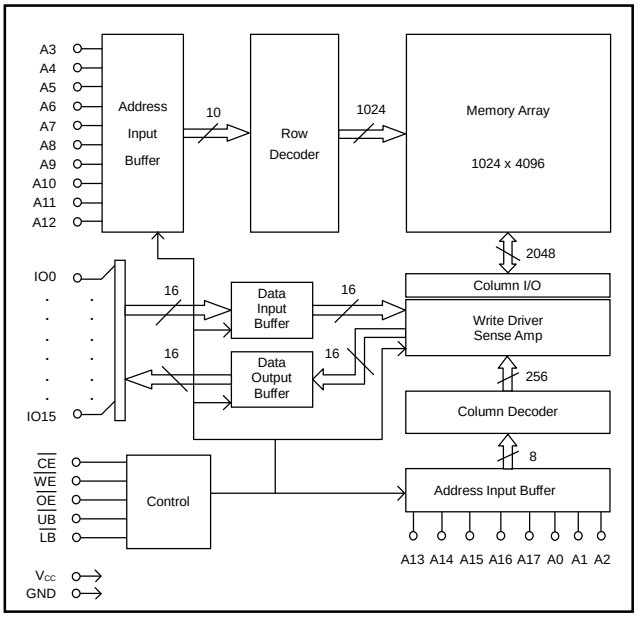
n PIN CONFIGURATIONS





48-ball BGA top view

n BLOCK DIAGRAM



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n PIN DESCRIPTIONS

Name	Function
A0-A17 Address Input	These 18 address inputs select one of the 262,144 x 16-bit words in the RAM
$\overline{CE}$ Chip Enable 1 Input	$\overline{CE}$ is active LOW. Chip enable must be active when data read form or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The IO pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the IO pins; when $\overline{WE}$ is LOW, the data present on the IO pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the IO pins and they will be enabled. The IO pins will be in the high impendence state when $\overline{OE}$ is inactive.
$\overline{LB}$ and $\overline{UB}$ Data Byte Control Input	Lower byte and upper byte data input/output control pins.
IO0-IO15 Data Input/Output Ports	There 8 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power Supply
GND	Ground

n TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	IO0~IO7	IO8~IO15	V_{CC} CURRENT
Not selected (Power Down)	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	X	X	X	H	H	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	L	X	High Z	High Z	I_{CC}
	L	H	H	X	L	High Z	High Z	I_{CC}
Read	L	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
				H	L	High Z	D_{OUT}	I_{CC}
				L	H	D_{OUT}	High Z	I_{CC}
Write	L	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
				H	L	X	D_{IN}	I_{CC}
				L	H	D_{IN}	X	I_{CC}

n ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +85	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	MA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

n OPERATING RANGE

RANG	AMBIENT TEMPERATURE	Vcc
Commercial	0^{O}C to + 70^{O}C	2.4V ~ 3.6V
Industrial	-40^{O}C to + 85^{O}C	2.4V ~ 3.6V

n CAPACITANCE (1) (T_A = 25^{O}C, f = 1.0MHz)

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{IO}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

n DC ELECTRICAL CHARACTERISTICS (T_A = -40^{O}C to +85^{O}C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS			MIN.	TYP.(1)	MAX.	UNITS
V_{CC}	Power Supply				2.4	--	3.6	V
V_{IL}	Guaranteed Input Low Voltage(2)				-0.3(2)	--	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)				2.0	--	V_{CC}+0.3(3)	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}			--	--	1	uA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$= V_{IH}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}			--	--	1	uA
V_{OL}	Output Low Voltage	V_{CC} = Max, I_{OL} = 2.0mA			--	--	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1.0mA			2.4	--	--	V
I_{CC}(5)	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{IO} = 0mA, f = F_{MAX}(3)	V_{CC}=3.0V	55ns	--	--	27	mA
				70ns			18	
I_{CCSB}	Standby Current – TTL	$\overline{CE}$ = V_{IH}, I_{IO} = 0mA		V_{CC}=3.0V	--	--	1.0	mA
I_{CCSB1}(4)	Standby Current – CMOS	$\overline{CE}$ ≧ V_{CC}-0.2V V_{IN} ≧ V_{CC}-0.2V or V_{IN} ≦ 0.2V		V_{CC}=3.0V	--	0.45	8.0	uA

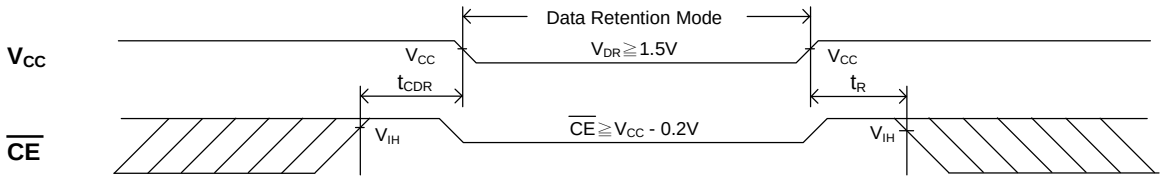
1. Typical characteristics are at T_A=25^{O}C.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: VCC+1.0V in case of pulse width less than 20 ns.
4. F_{MAX}=1/t_{RC}.
5. $I_{CCSB1\_MAX.}$ is 6.0uA at V_{CC}=3.0V and T_A=70^{O}C.
6. $I_{CC\_MAX.}$ is 25mA(@55ns)/17mA(@70nS) at V_{CC}=3.0V and T_A=70^{O}C.

n DATA RETENTION CHARACTERISTICS (T_A = -40^{O}C to +85^{O}C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{CE}$ ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN} ≦ 0.2V	1.5	--	--	V
I_{CCDR}(3)	Data Retention Current	$\overline{CE}$ ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN} ≦ 0.2V	--	0.15	1.7	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		t_{RC} (2)	--	--	ns

1. V_{CC}=1.5V, T_A=25^{O}C.
2. t_{RC} = Read Cycle Time.
3. $I_{CCRD\_Max.}$ is 1.2uA at T_A=70^{O}C.

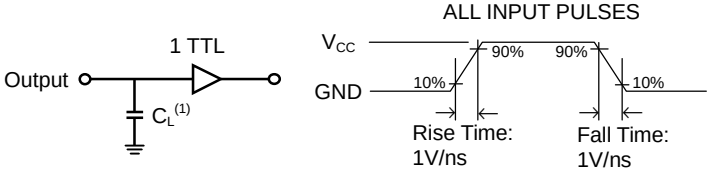
n LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE}$ Controlled)



n AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels		Vcc / 0V
Input Rise and Fall Times		1V/ns
Input and Output Timing Reference Level		0.5Vcc
Output Load	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}	C_L = 5pF+1TTL
	Others	C_L = 30pF+1TTL



n KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOW
	DOES NOT APPLY	CENTER LINE IS HIGH INPEDANCE "OFF" STATE

1. Including jig and scope capacitance.

n AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

READ CYCLE

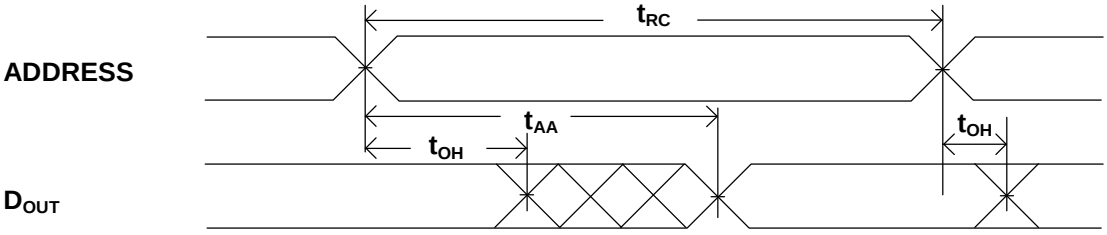
JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 55ns (V_{CC}=2.7~3.6V) MIN.	TYP.	MAX.	CYCLE TIME : 70ns (V_{CC}=2.4~3.6V) MIN.	TYP.	MAX.	UNITS
t_{AVAX}	t_{RC}	Read Cycle Time	55	--	--	70	--	--	ns
t_{AVQX}	t_{AA}	Address Access Time	--	--	55	--	--	70	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time ($\overline{CE}$)	--	--	55	--	--	70	ns
t_{BLQV}	t_{BA} (1)	Data Byte Control Access Time ($\overline{LB}$, $\overline{UB}$)	--	--	30	--	--	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	30	--	--	35	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z ($\overline{CE}$)	10	--	--	10	--	--	ns
t_{BLQX}	t_{BE}	Data Byte Control to Output Low Z ($\overline{LB}$, $\overline{UB}$)	10	--	--	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	5	--	--	5	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Select to Output High Z ($\overline{CE}$)	--	--	30	--	--	35	ns
t_{BHQZ}	t_{BDO}	Data Byte Control to Output High Z ($\overline{LB}$, $\overline{UB}$)	--	--	30	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Enable to Output High Z	--	--	25	--	--	30	ns
t_{AVQX}	t_{OH}	Data Hold from Address Change	10	--	--	10	--	--	ns

NOTE :

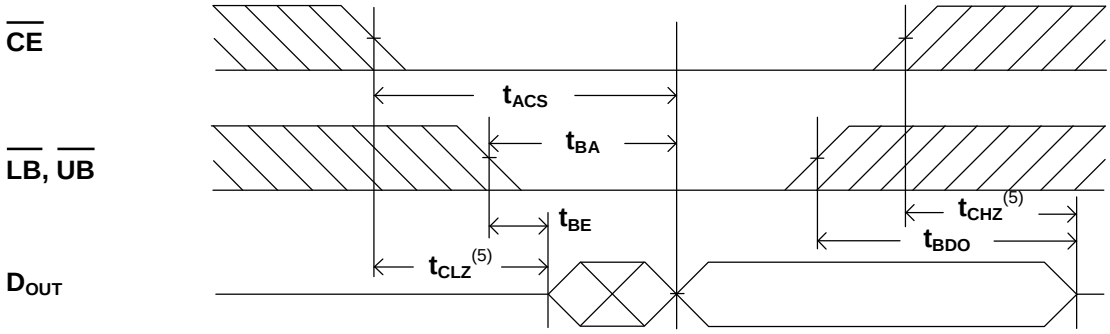
1. t_{BA} is 30ns/35ns(@speed=55ns/70ns) with address toggle; t_{BA} is 55ns/70ns(@speed=55ns/70ns) without address toggle

n SWITCHING WAVEFORMS (READ CYCLE)

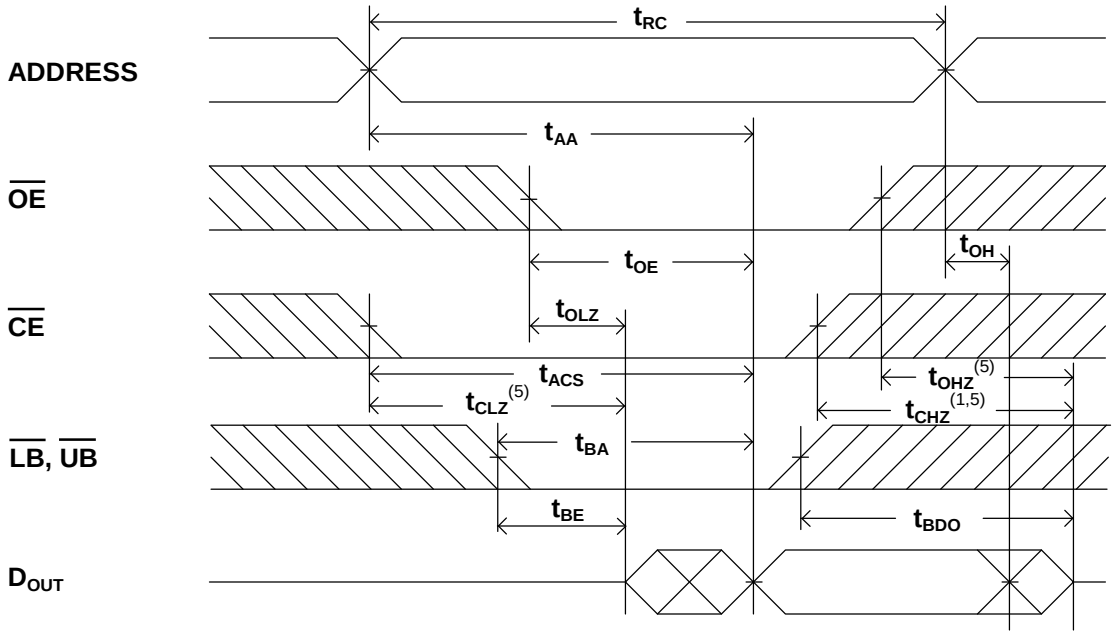
READ CYCLE 1 (1,2,4)



READ CYCLE 2 (1,3,4)



READ CYCLE 3 (1, 4)



NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ± 500mV from steady state with C_L = 5pF.
   The parameter is guaranteed but not 100% tested.

n AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

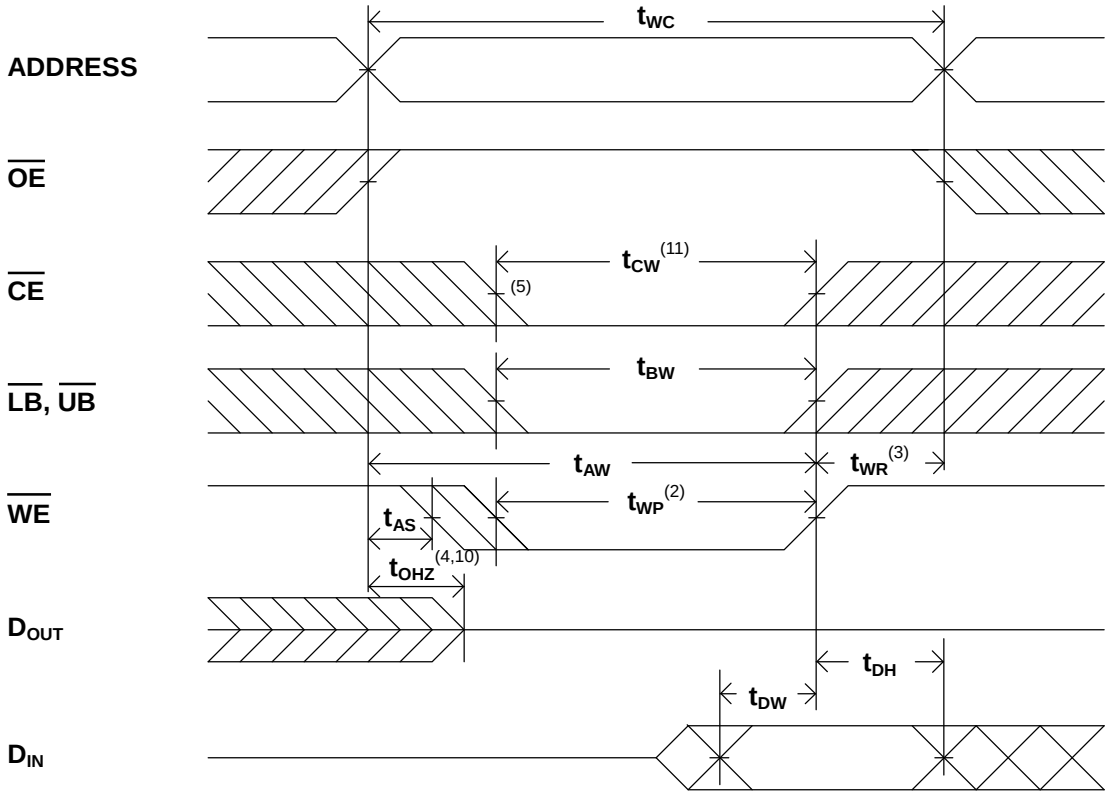
WRITE CYCLE

JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 55ns (V_{CC}=2.7~3.6V) MIN.	TYP.	MAX.	CYCLE TIME : 70ns (V_{CC}=2.4~3.6V) MIN.	TYP.	MAX.	UNITS
t_{AVAX}	t_{WC}	Write Cycle Time	55	--	--	70	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55	--	--	70	--	--	ns
t_{ELWH}	t_{CW}	Chip Select to End of Write ($\overline{CE}$)	55	--	--	70	--	--	ns
t_{BLWH}	t_{BW}(1)	Data Byte Control to End of Write ($\overline{LB}$, $\overline{UB}$)	25	--	--	30	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	30	--	--	35	--	--	ns
t_{WHAX}	t_{WR}	Write Recovery Time ($\overline{CE}$, $\overline{WE}$)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output High Z	--	--	25	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	--	--	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	5	--	--	ns

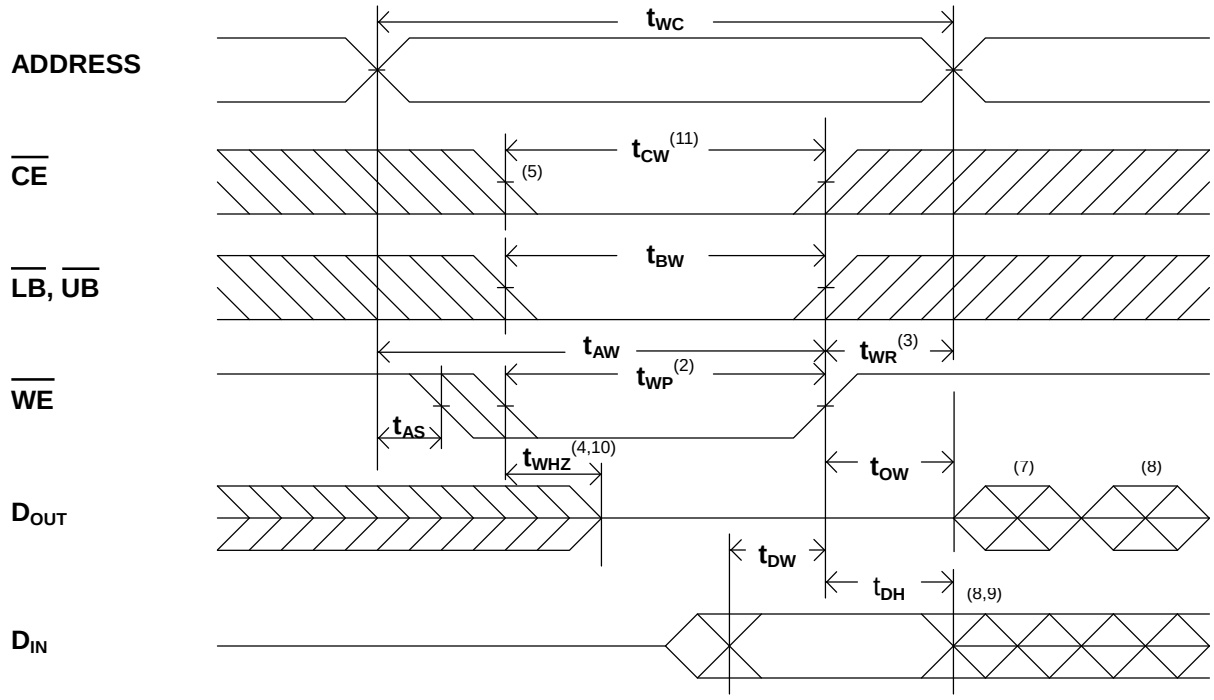
NOTE:
1. t_{BW} is 25ns/30ns (@speed=55ns/70ns) with address toggle; t_{BW} is 55ns/70ns (@speed=55ns/70ns) without address toggle.

n SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



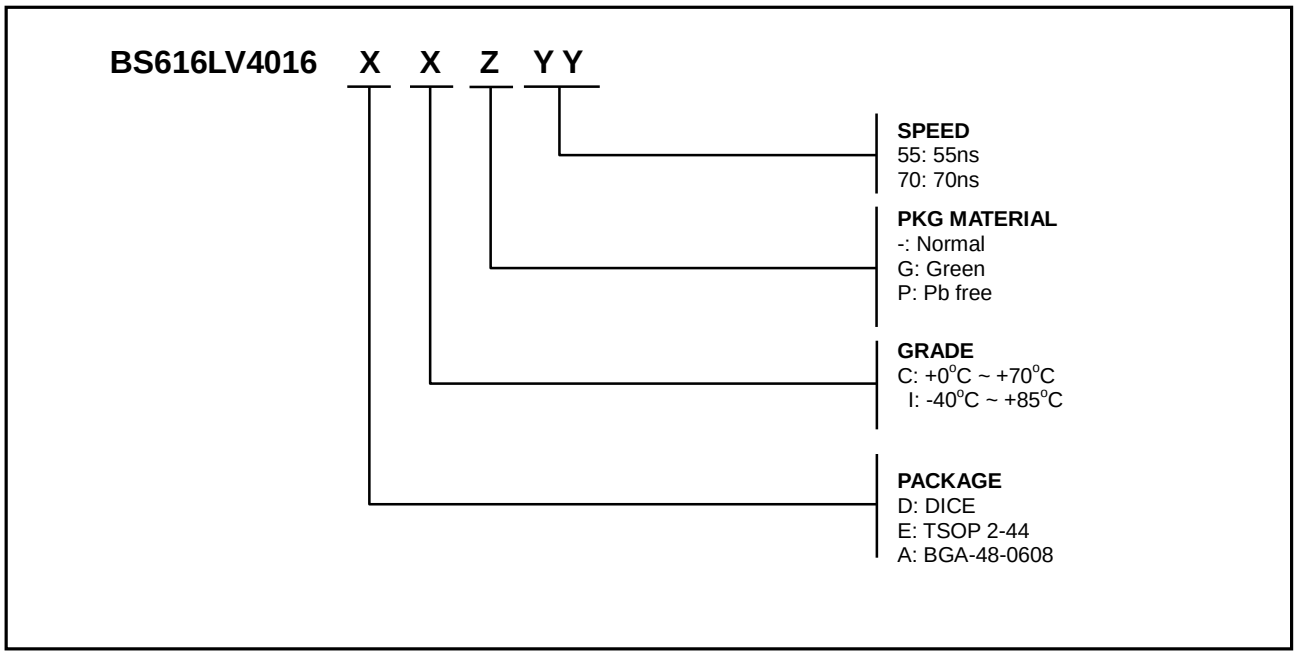
WRITE CYCLE 2 (1,6)



NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, IO pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, IO pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state with C_L = 5pF.
    The parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.

n ORDERING INFORMATION



Note:
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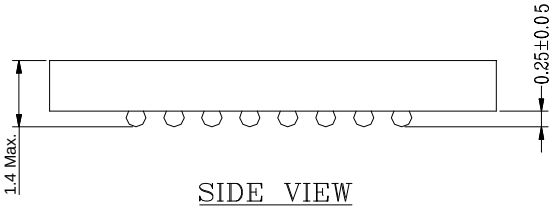
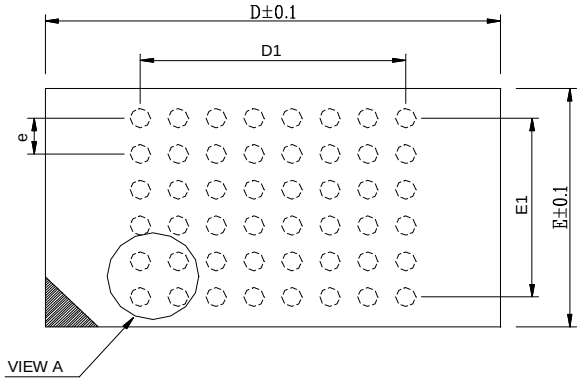
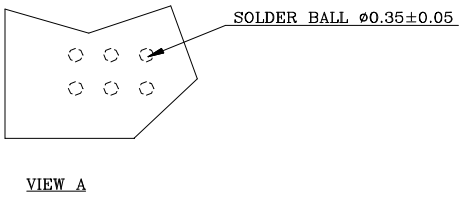
n PACKAGE DIMENSIONS



NOTES
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

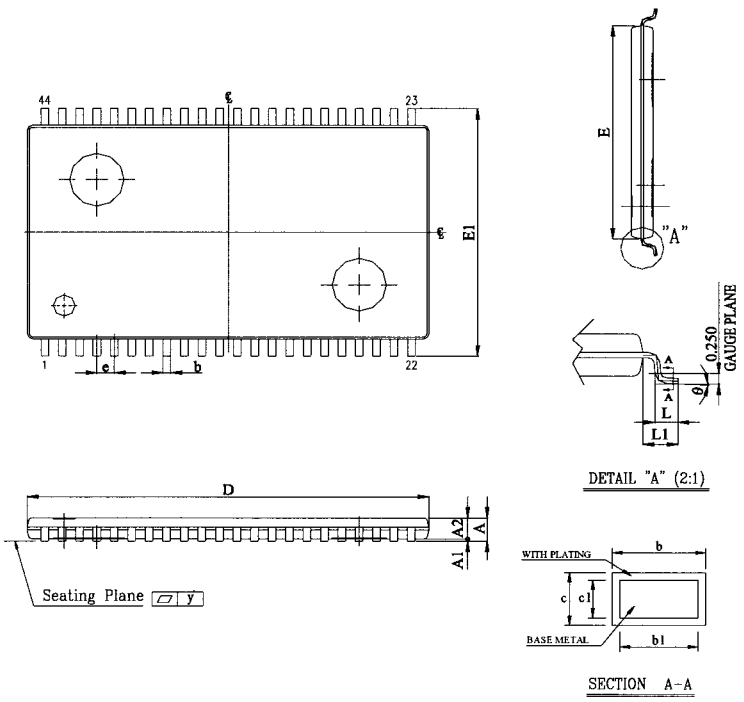
BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75





48 mini-BGA (6 x 8mm)

n PACKAGE DIMENSIONS (continued)



SYMBOL \ UNIT	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.012 ~ 0.018	0.30 ~ 0.45
b1	0.012 ~ 0.016	0.30 ~ 0.40
c	0.005 ~ 0.008	0.12 ~ 0.21
c1	0.005 ~ 0.006	0.12 ~ 0,16
D	0.725± 0.004	18.41± 0.10
E	0.400± 0.004	10.16± 0.10
E1	0.463± 0.008	11.76± 0.20
e	0.0315± 0.004	0.80± 0.10
L	0.0197± 0.004	0.50± 0.10
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

TSOP2-44