M5M5408FP,TP,RT-85VL,-10VL, -85VLL,-10VLL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408 is 4194304-bit CMOS static RAM organized as 524288-words by 8-bit, fabricated using high-performance quadruple-polysilicon and double metal CMOS technology.

The use of thin film transistor (TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5408 is designed for memory applications where the high performance, high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408 is offered in a 32-pin plastic small outline package (SOP) and a 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available, M5M5408TP(normal lead bend type package) and M5M5408RT(reverse lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

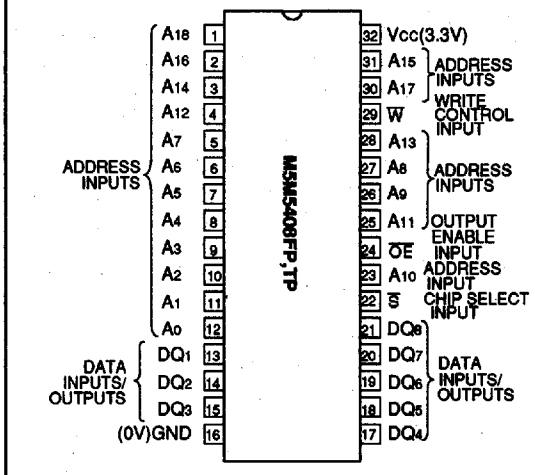
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5408FP,TP,RT-85VL M5M5408FP,TP,RT-10VL	85ns 100ns	3mA (1MHz)	60μA (Vcc=3.6V)
M5M5408FP,TP,RT-85VLL M5M5408FP,TP,RT-10VLL	85ns 100ns		12μA (Vcc=3.6V) 0.4μA (Vcc=3V,typ)

- Single +3.3V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage=2.0Vto 3.6V
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Small stand-by current·····0.4μA(typ.)
- Package
  - M5M5408FP : 32 pin 525 mil SOP
  - M5M5408TP : 32 pin 400 mil TSOP(Ⅱ)
  - M5M5408RT : 32 pin 400 mil TSOP(Ⅱ)

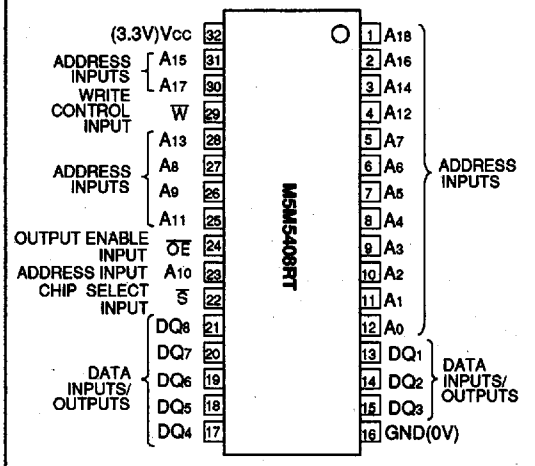
APPLICATION

Small capacity memory units, IC card, Battery operating system, Asynchronous server system

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)
32P3Y-H(TP)



Outline 32P3Y-J

FUNCTION

The operation mode of the M5M5408 is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

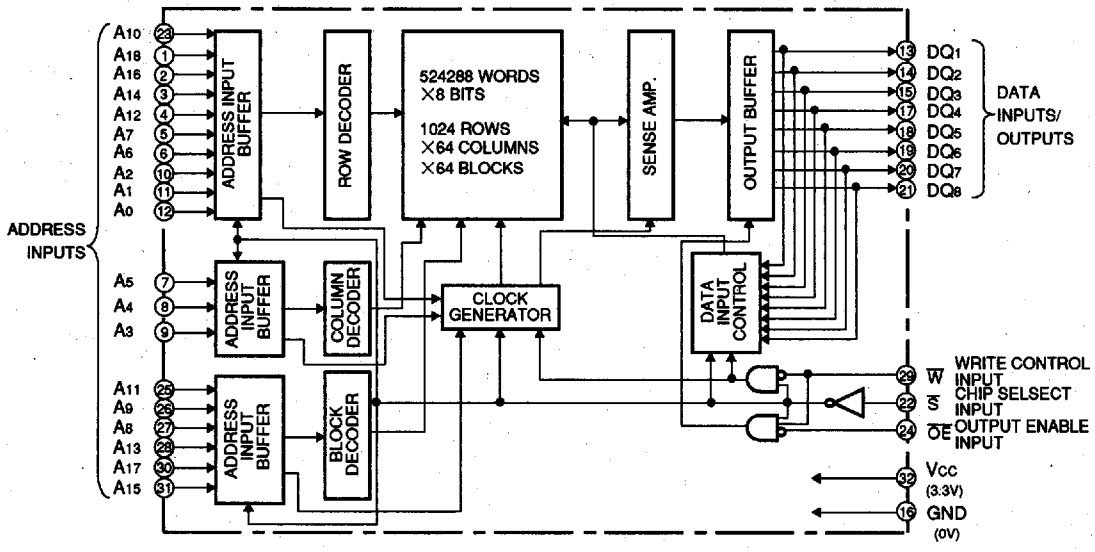
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode,the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D IN	Active
L	H	L	Read	D OUT	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage	With respect to GND	−0.3*～Vcc + 0.3	V
V_O	Output voltage	With respect to GND	0～Vcc	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC(Pulse width≦30ns)

ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.6	V
V_{OH}	High-level output voltage	I_{OH} = −1mA		2.4			V
		I_{OH} = −0.1mA		Vcc−0.5V			
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0～Vcc				±1	μA
I_O	Output leakage current	$\overline{S}$=V_{IH}, $\overline{OE}$=V_{IH}, $V_{I/O}$=0～Vcc				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$≦0.2V Other inputs ≦0.2V or ≧Vcc − 0.2V Output-open (duty 100%)	Minimum cycle		20	30	mA
			1MHz		1.5	3	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} Other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	Minimum cycle		20	30	mA
			1MHz		1.5	3	
I_{CC3}	Stand-by supply current	$\overline{S}$≧Vcc − 0.2V other inputs = 0～Vcc	FP,TP,RT-VL			60	μA
			FP,TP,RT-VLL		0.4	12	
I_{CC4}	Stand-by supply current	$\overline{S}$=V_{IH}, other inputs=0～Vcc				0.33	mA

* −3.0V in case of AC(Pulse width≦30ns)

CAPACITANCE (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta=25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance (Ta=25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
2: Typical value is Vcc=3.3V, Ta = 25℃

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

READ CYCLE

Symbol	Parameter	Limits				Unit
		M5M5408-85VL,-85VLL		M5M5408-10VL,-10VLL		
		Min	Max	Min	Max	
tCR	Read cycle time	85		100		ns
ta (A)	Address access time		85		100	ns
ta (S)	Chip select access time		85		100	ns
ta (OE)	Output enable access time		45		50	ns
tdis (S)	Output disable time after $\overline{S}$ high		30		35	ns
tdis (OE)	Output disable time after $\overline{OE}$ high		30		35	ns
ten (S)	Output disable time after $\overline{S}$ low	10		10		ns
ten (OE)	Output enable time after $\overline{OE}$ low	5		5		ns
tv (A)	Data valid time after address	10		10		ns

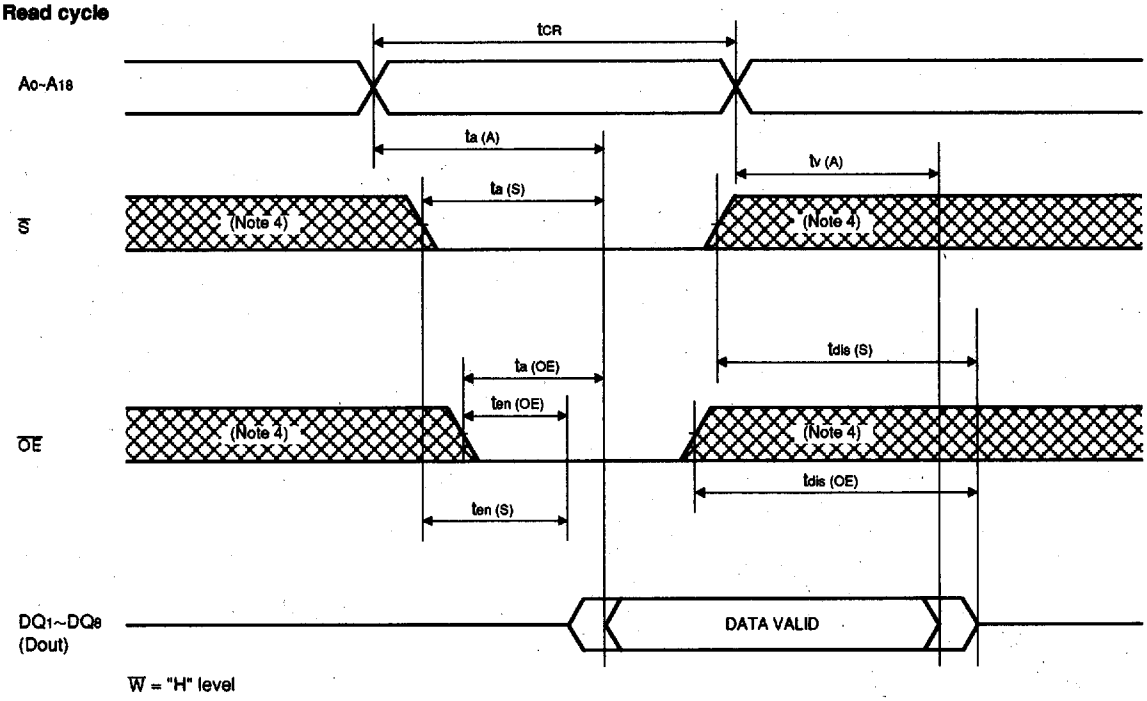
TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M5408-85VL,-85VLL		M5M5408-10VL,-10VLL		
		Min	Max	Min	Max	
tCW	Write cycle time	85		100		ns
tw (W)	Write pulse width	55		60		ns
tsu (A)	Address set up time	0		0		ns
tsu (A-WH)	Address set up time with respect to $\overline{W}$ high	70		80		ns
tsu (S)	Chip select set up time	70		80		ns
tsu (D)	Data set up time	35		35		ns
th (D)	Data hold time	0		0		ns
trec (W)	Write recovery time	0		0		ns
tdis (W)	Output disable time after $\overline{W}$ low		30		35	ns
tdis (OE)	Output disable time after $\overline{OE}$ high		30		35	ns
ten(W)	Output enable time after $\overline{W}$ high	5		5		ns
ten (OE)	Output enable time after $\overline{OE}$ low	5		5		ns

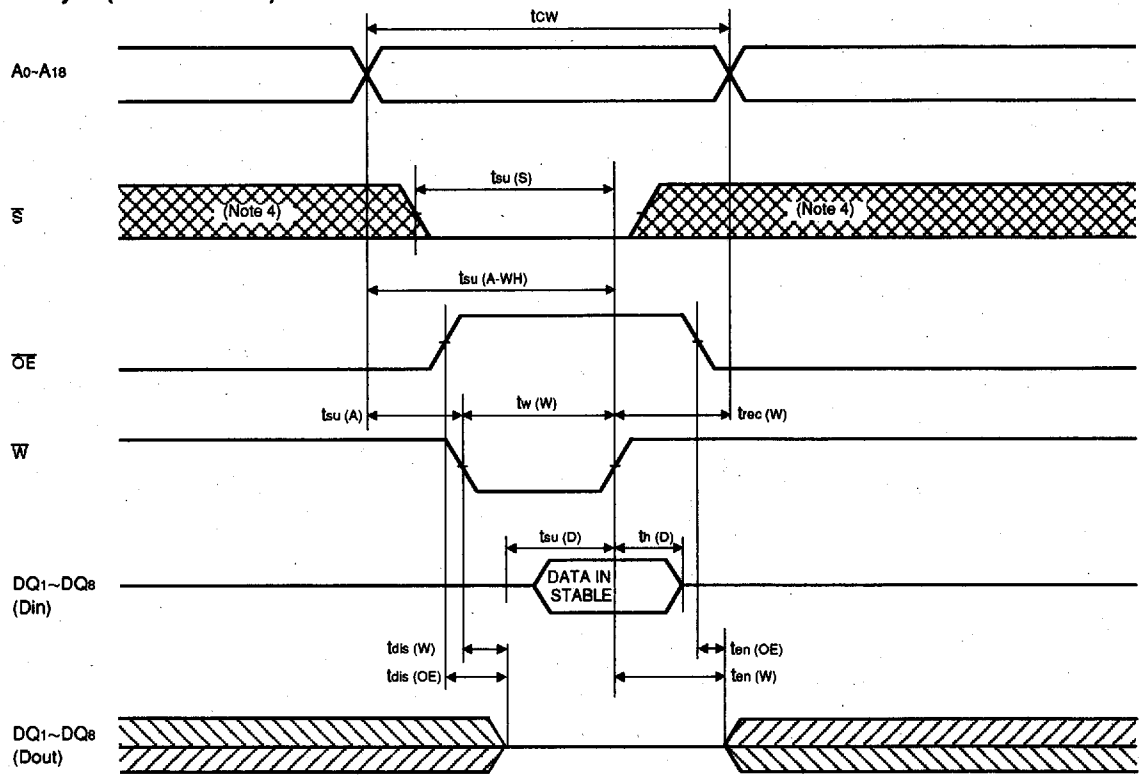
TIMING DIAGRAMS

Read cycle

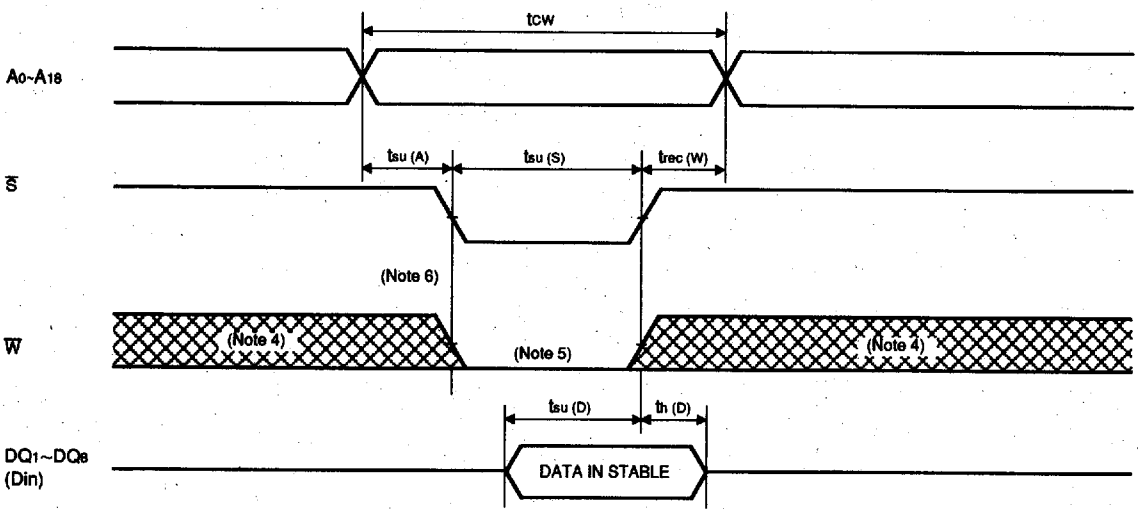


W = "H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3 : Test condition
Input pulse·····VIH=2.2V, VIL=0.4V
Input rise time and fall time··· 5ns
Reference level·····VOH=VOL=1.5V
Output loads····· Fig. 1, CL=30pF
CL=5pF (for ten, tdis)
Transition is measured±500mV from steady state voltage. (for ten, tdis)

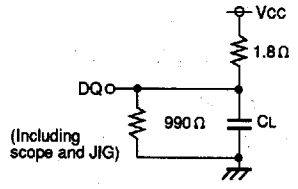


Fig.1 Output load

Note 4 : Hatching indicates the state is "don't care".
5 : A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
6 : If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the highimpedance state.
7 : Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (\overline{S})}$	Chip select input $\overline{S}$			2.0			V
$I_{CC\ (PD)}$	Power down supply current	V_{CC}=3V, $\overline{S} \geq V_{CC}$ - 0.2V, Other inputs=0~3V	FP, TP, RT-VL			50	μA
			FP, TP, RT-VLL		0.4	10*	

* $I_{CC\ (PD)}$ = 1 μA at Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode