MA2607V10000000

N-Ch and P-Ch Fast Switching MOSFETs

General Description

The MA2607V is the highest performance trench N-ch and P-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The MA2607V meet the RoHS and Green Product requirement with full function reliability approved.

Product Summery

Green

BVDSS	RDSON	ID
20V	85mΩ	2.8 A
-20V	205mΩ	-2 A

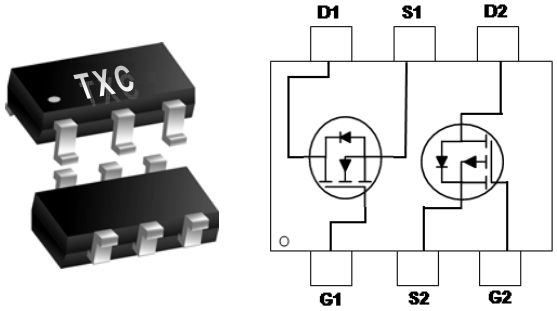
Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

Applications

- High Frequency Point-of-Load Synchronous s
  Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

TSOP6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±8	±8	V
I_D@T_A=25°C	Continuous Drain Current, V_{GS} @ -4.5V[1]	2.8	-2	A
I_D@T_A=70°C	Continuous Drain Current, V_{GS} @ -4.5V[1]	2.2	-1.6	A
I_{DM}	Pulsed Drain Current[2]	9	-9	A
P_D@T_A=25°C	Total Power Dissipation[3]	1.1	1.1	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	110	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	70	°C/W

Rev A.01 D100410

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N-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25°C , I_D=1mA	---	0.02	---	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=2.5A	---	70	85	mΩ
		V_{GS}=2.5V , I_D=1.5A	---	90	115	
		V_{GS}=1.8V , I_D=1A		120	160	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.3	0.6	1	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-2.5	---	mV/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25°C	---	---	1	uA
		V_{DS}=16V , V_{GS}=0V , T_J=55°C	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±8V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=2A	---	2.8	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2	4	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=12V , V_{GS}=4.5V , I_D=2.5A	---	3.4	---	nC
Q_{gs}	Gate-Source Charge		---	0.35	---	
Q_{gd}	Gate-Drain Charge		---	1.37	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=12V , V_{GS}=10V , R_G=3.3Ω , I_D=1A	---	7.4	---	ns
T_r	Rise Time		---	3.4	---	
$T_{d(off)}$	Turn-Off Delay Time		---	28.4	---	
T_f	Fall Time		---	1.6	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	204	---	pF
C_{oss}	Output Capacitance		---	43.6	---	
C_{rss}	Reverse Transfer Capacitance		---	30	---	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	2.8	A
I_{SM}	Pulsed Source Current[2,4]		---	---	9	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25°C	---	---	1.2	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150°C junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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N-Channel Typical Characteristics

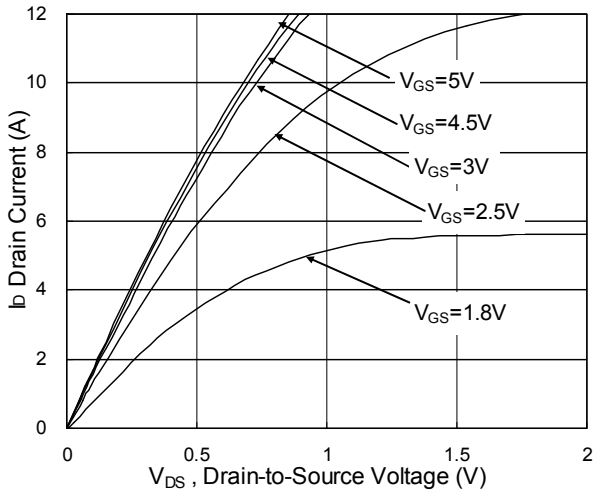

Fig.1 Typical Output Characteristics

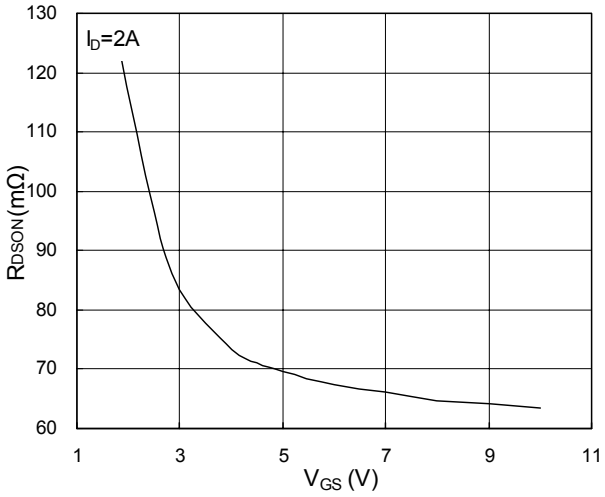

Fig.2 On-Resistance vs. Gate-Source

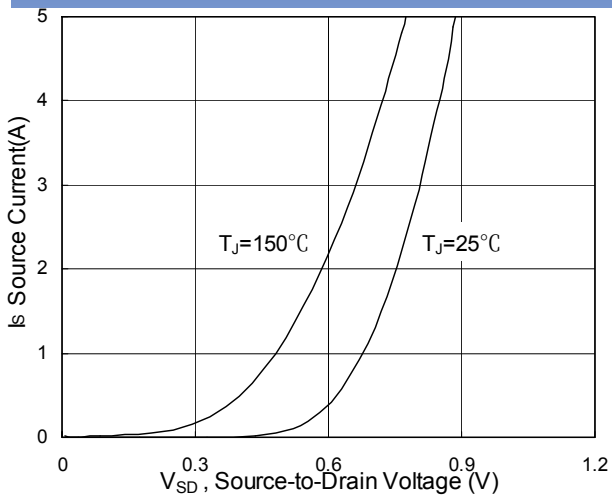

Fig.3 Forward Characteristics Of Reverse

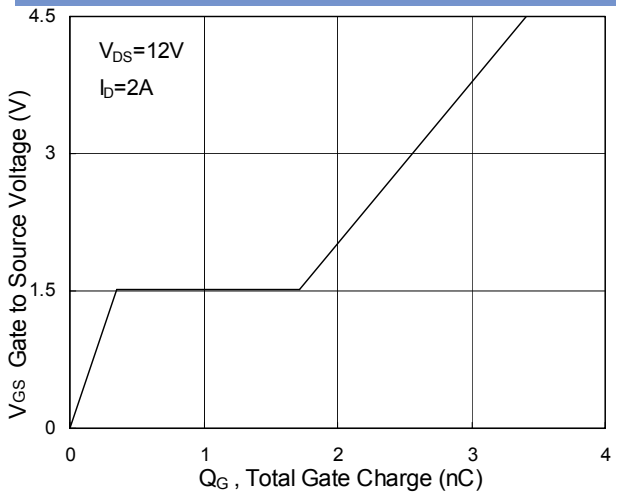

Fig.4 Gate-Charge Characteristics

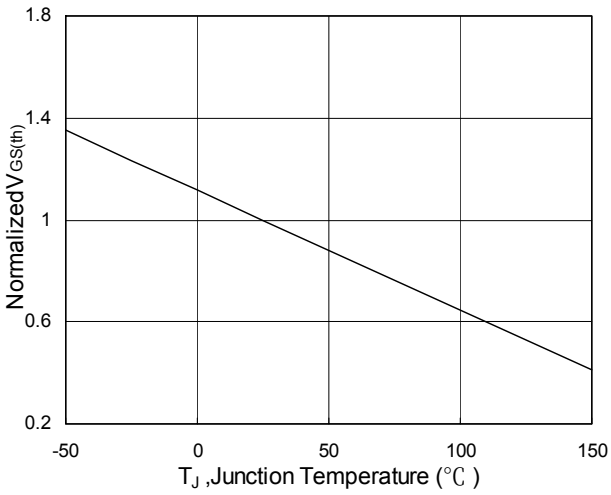

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

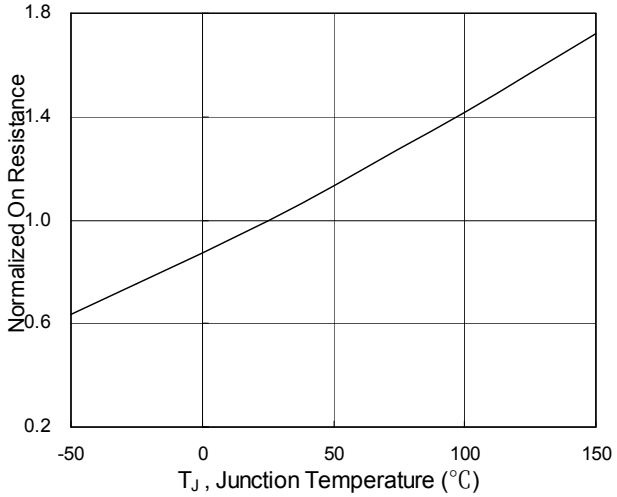

Fig.6 Normalized R_{DSON} vs. T_J

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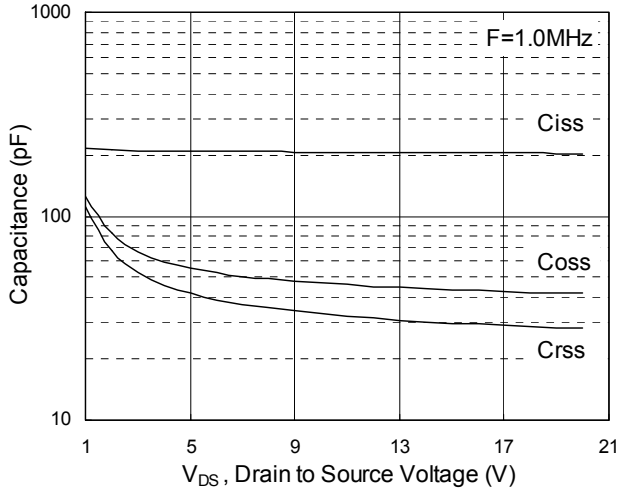

Fig.7 Capacitance

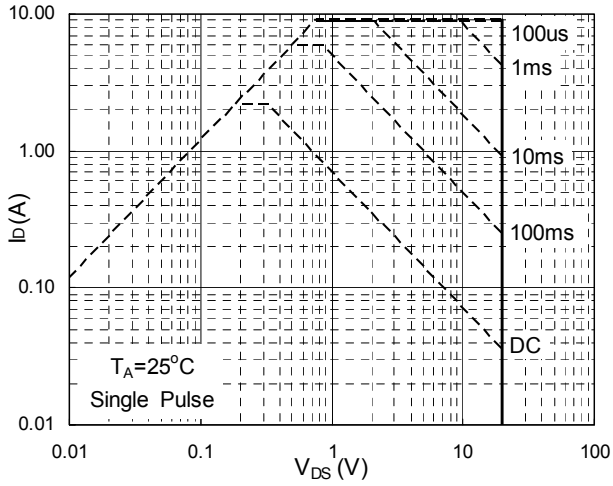

Fig.8 Safe Operating Area

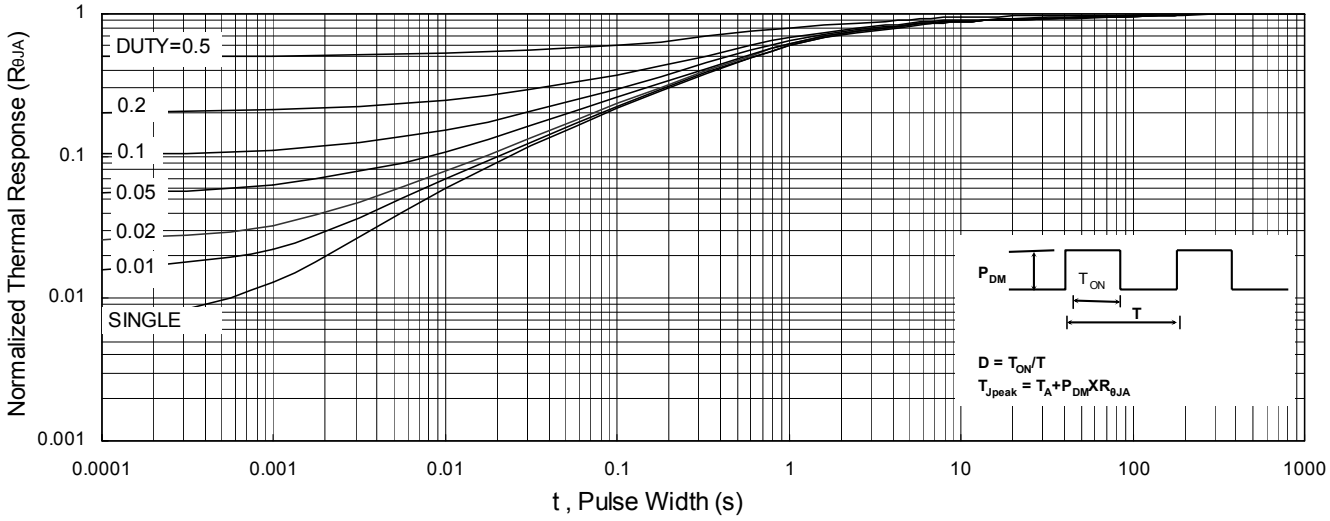

Fig.9 Normalized Maximum Transient Thermal Impedance

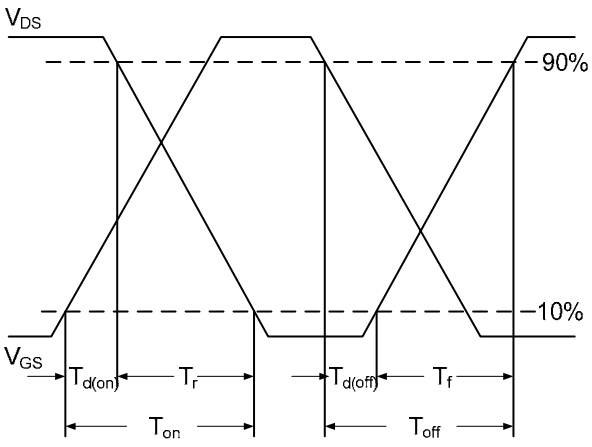

Fig.10 Switching Time Waveform

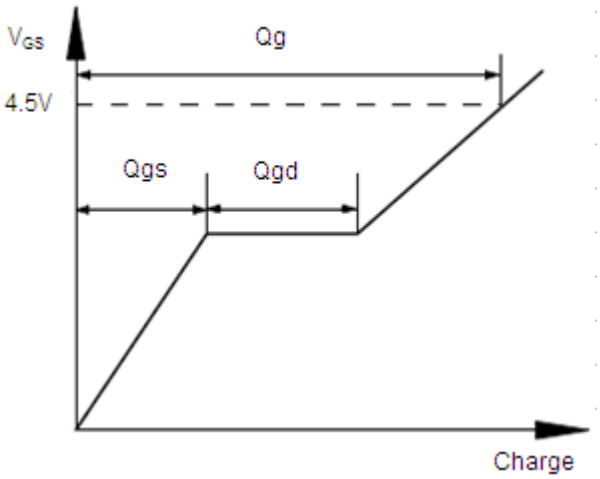

Fig.11 Gate Charge Waveform

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P-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25°C , I_D=-1mA	---	-0.011	---	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-2A	---	170	205	mΩ
		V_{GS}=-2.5V , I_D=-1.5A	---	235	280	
		V_{GS}=-1.8V , I_D=-1A		315	380	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.3	-0.5	-1	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.02	---	mV/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-16V , V_{GS}=0V , T_J=25°C	---	---	-1	uA
		V_{DS}=-16V , V_{GS}=0V , T_J=55°C	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±8V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-2A	---	3.2	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-2A	---	4.6	---	nC
Q_{gs}	Gate-Source Charge		---	0.27	---	
Q_{gd}	Gate-Drain Charge		---	2.34	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-12V , V_{GS}=-4.5V , R_G=3.3Ω , I_D=-1A	---	11.6	---	ns
T_r	Rise Time		---	6.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	31.8	---	
T_f	Fall Time		---	2.8	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	194	---	pF
C_{oss}	Output Capacitance		---	35.5	---	
C_{rss}	Reverse Transfer Capacitance		---	28.2	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-2	A
I_{SM}	Pulsed Source Current[2,4]		---	---	-9	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25°C	---	---	-1	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150°C junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Channel Typical Characteristics

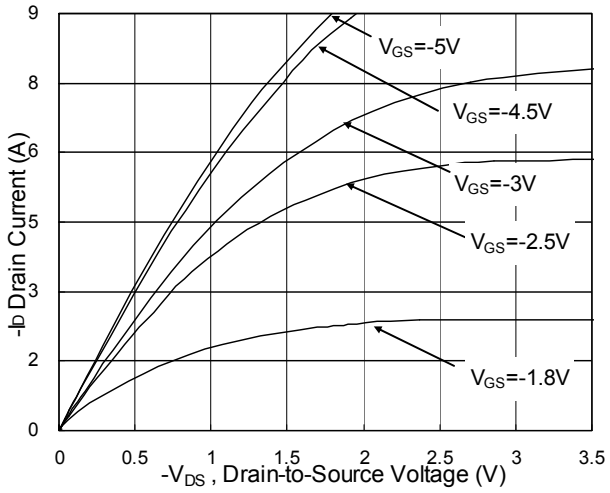
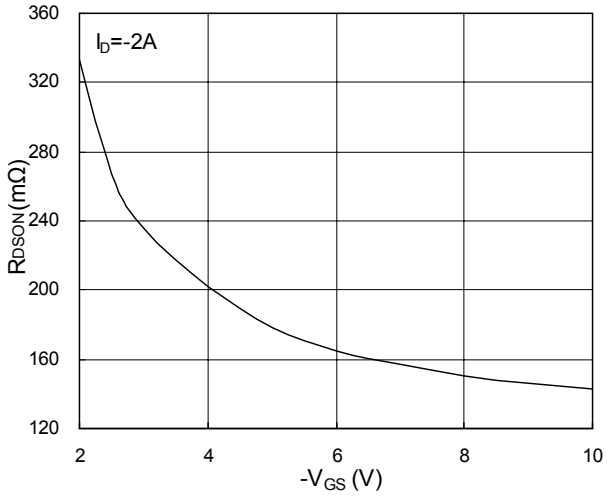


Fig.1 Typical Output Characteristics



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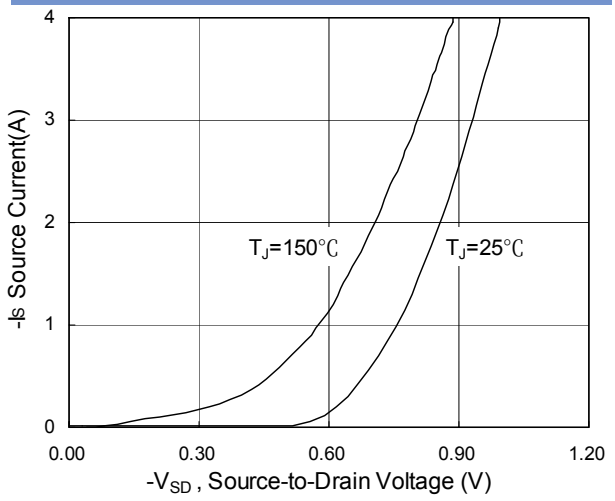

Fig.3 Forward Characteristics Of Reverse

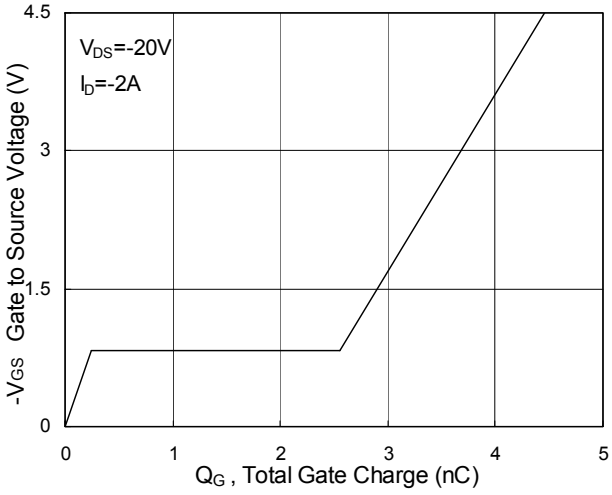

Fig.4 Gate-Charge Characteristics

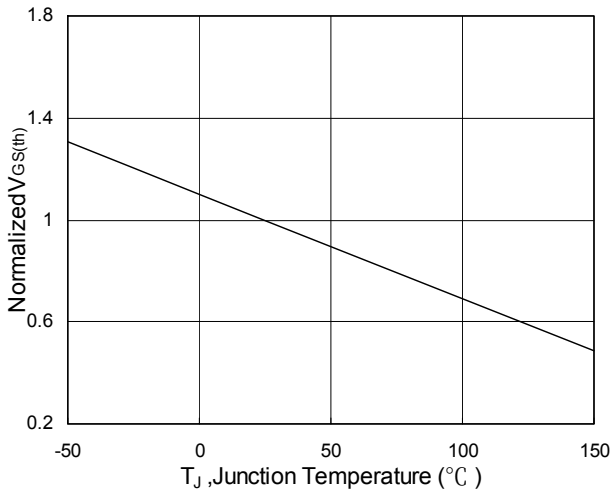

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

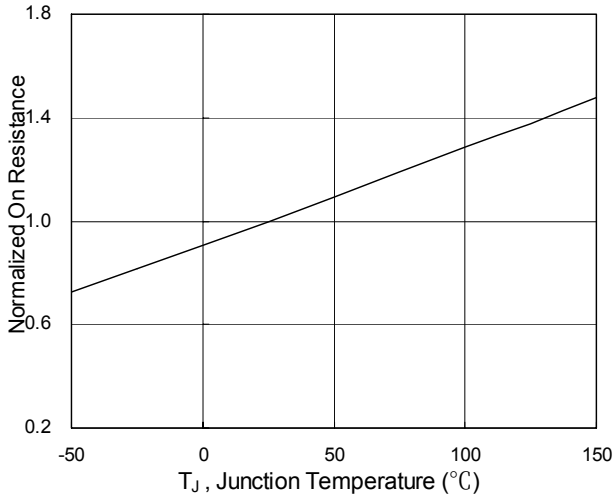

Fig.6 Normalized R_{DSON} vs. T_J

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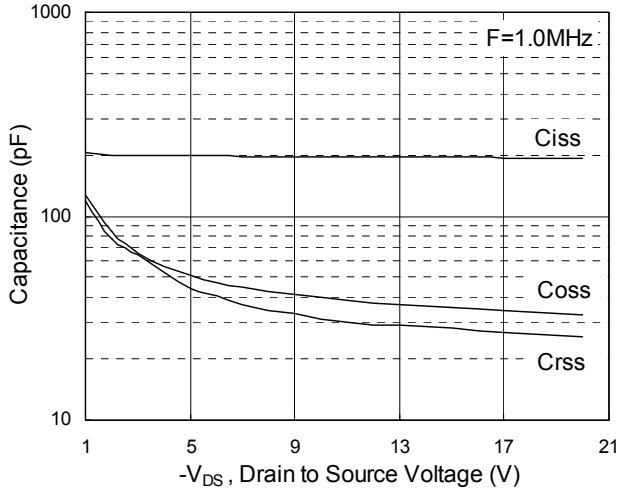

Fig.7 Capacitance

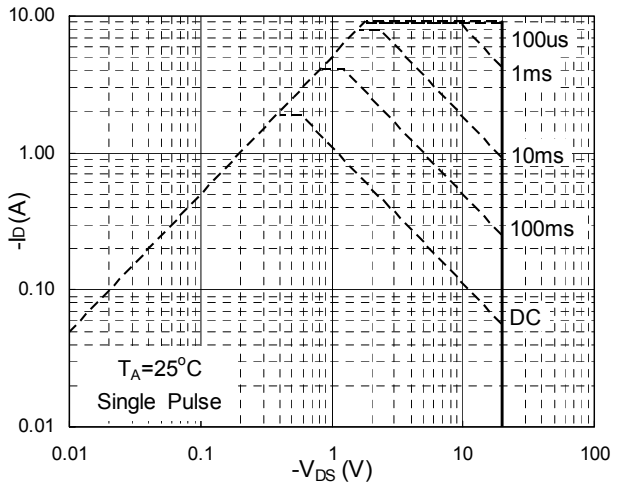

Fig.8 Safe Operating Area

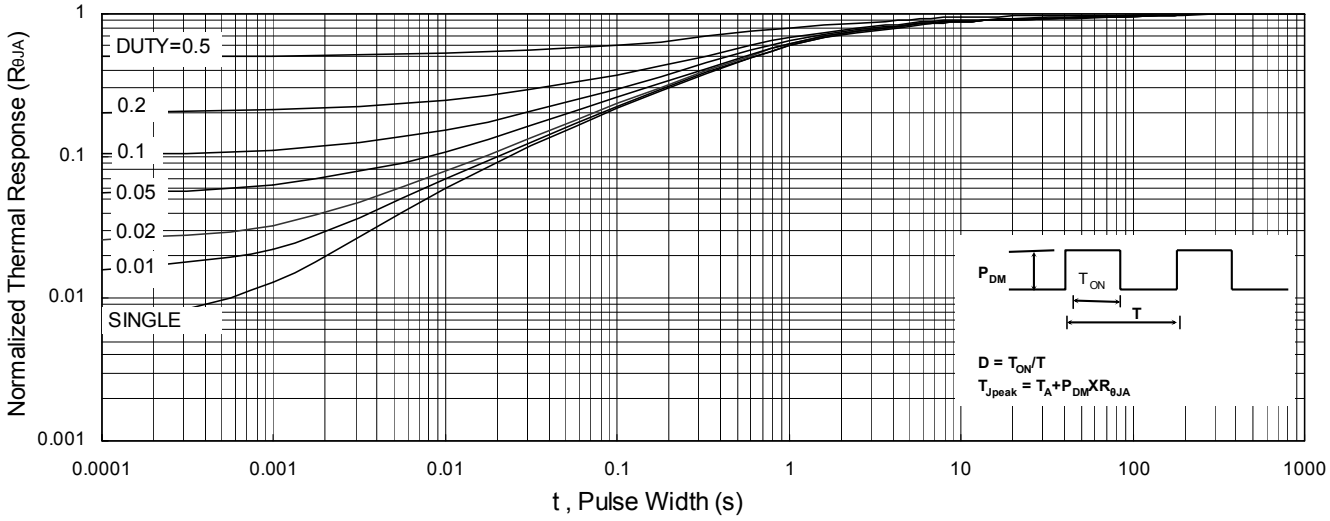

Fig.9 Normalized Maximum Transient Thermal Impedance

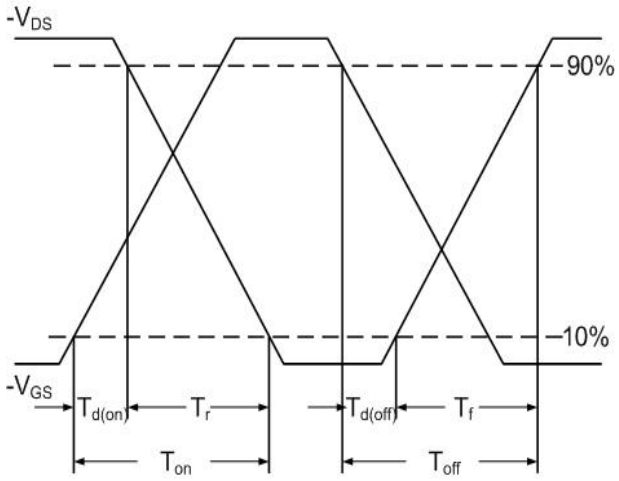

Fig.10 Switching Time Waveform

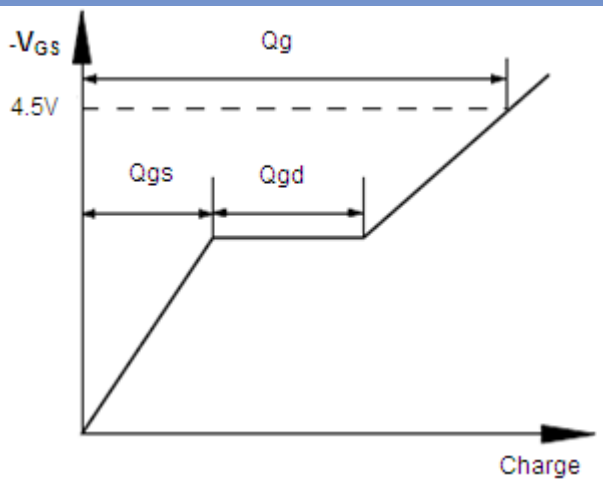

Fig.11 Gate Charge Waveform

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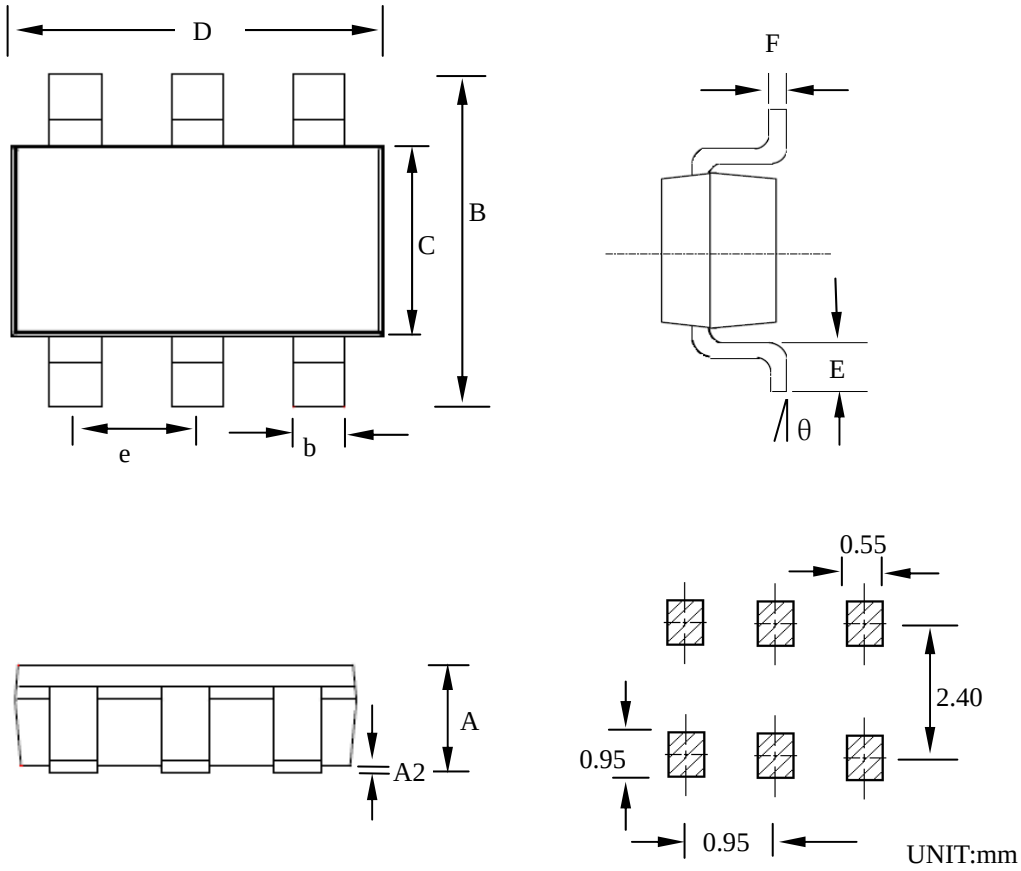
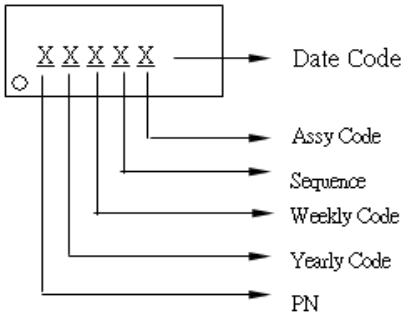


LAND PATTERN RECOMMENDATION

MARKING



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	--	1.20	0.031	--	0.047
A2	0.00	--	0.10	0.000	--	0.004
B	2.60	2.80	3.00	0.102	0.110	0.118
C	1.40	1.60	1.80	0.055	0.063	0.071
D	2.70	2.90	3.10	0.106	0.114	0.122
E	0.30	0.40	0.60	0.012	0.016	0.024
F	0.07	0.127	0.20	0.003	0.005	0.008
b	0.30	0.40	0.50	0.012	0.016	0.020
e	--	0.95	--	--	0.037	--
θ	0°	5°	10°	0°	5°	10°

Note:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.CONTROLLING DIMENSION IS MILLIMETER CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACTLY.

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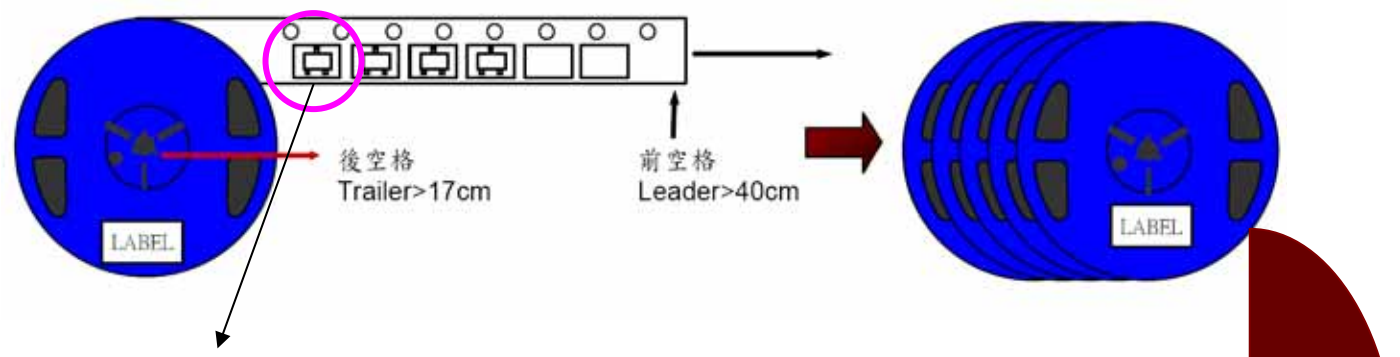
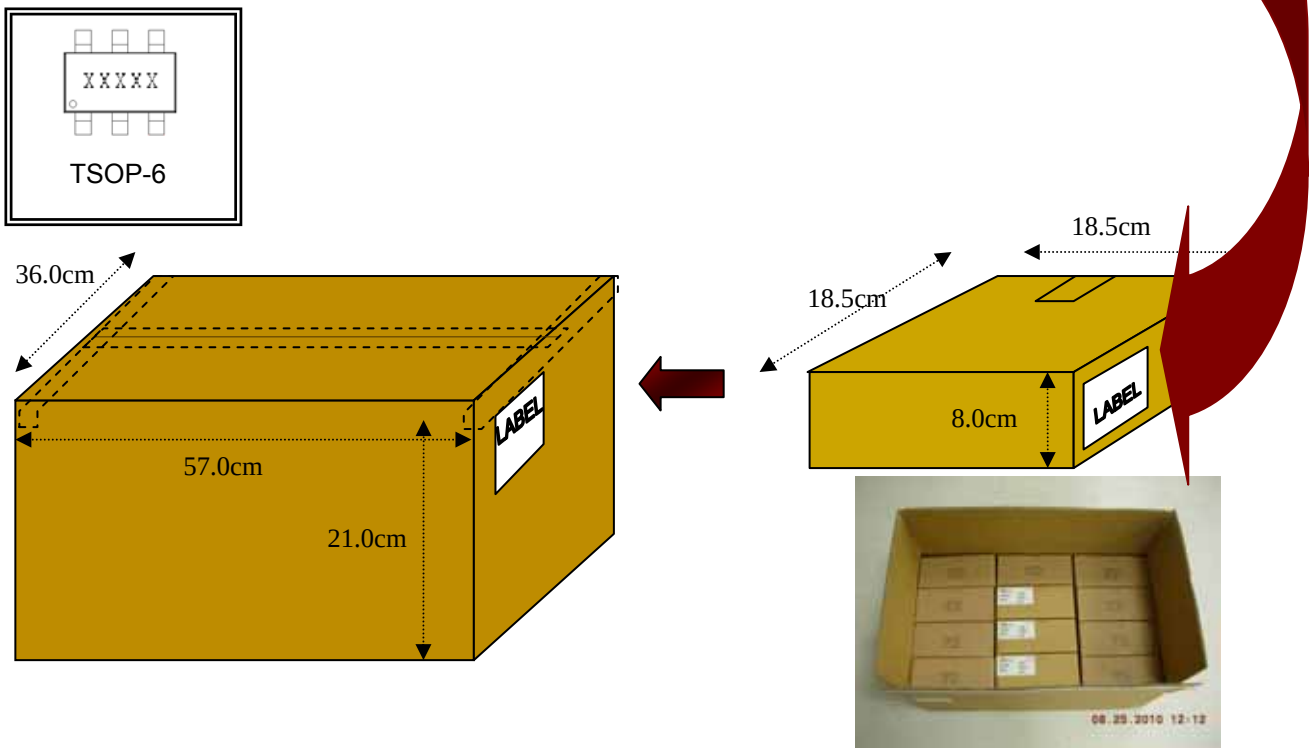
Tape & Reel 繞捲及裝箱方式 – TSOP-6



產品正印及方向 –（正印為正時，Tape 圓孔在上方）



封裝形態 PKG TYPE	一 般 包 裝		
	一卷數量 Immediate Quantity	中箱數量 Intermediate Quantity	外箱裝置/數量 Carton Quantity
TSOP-6	3000pcs	15000pcs	180 K
	Reel（7”）	Box(5 reels)	Carton(12 Box)

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