FAST CMOS ADDRESS/CLOCK DRIVER

IDT54/74FCT162344AT/CT/ET

FEATURES:

- 0.5 MICRON CMOS Technology
- Ideal for address line driving and clock distribution
- 8 banks with 1:4 fanout and 3-state
- Typical $t_{SK(o)}$ (Output Skew) < 500ps
- Balanced Output Drivers:
  - ±24mA (commercial)
  - ±16mA (military)
- Reduced system switching noise
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch CERPACK packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 5V ±10%
- Low input and output leakage ≤1µA (max.)

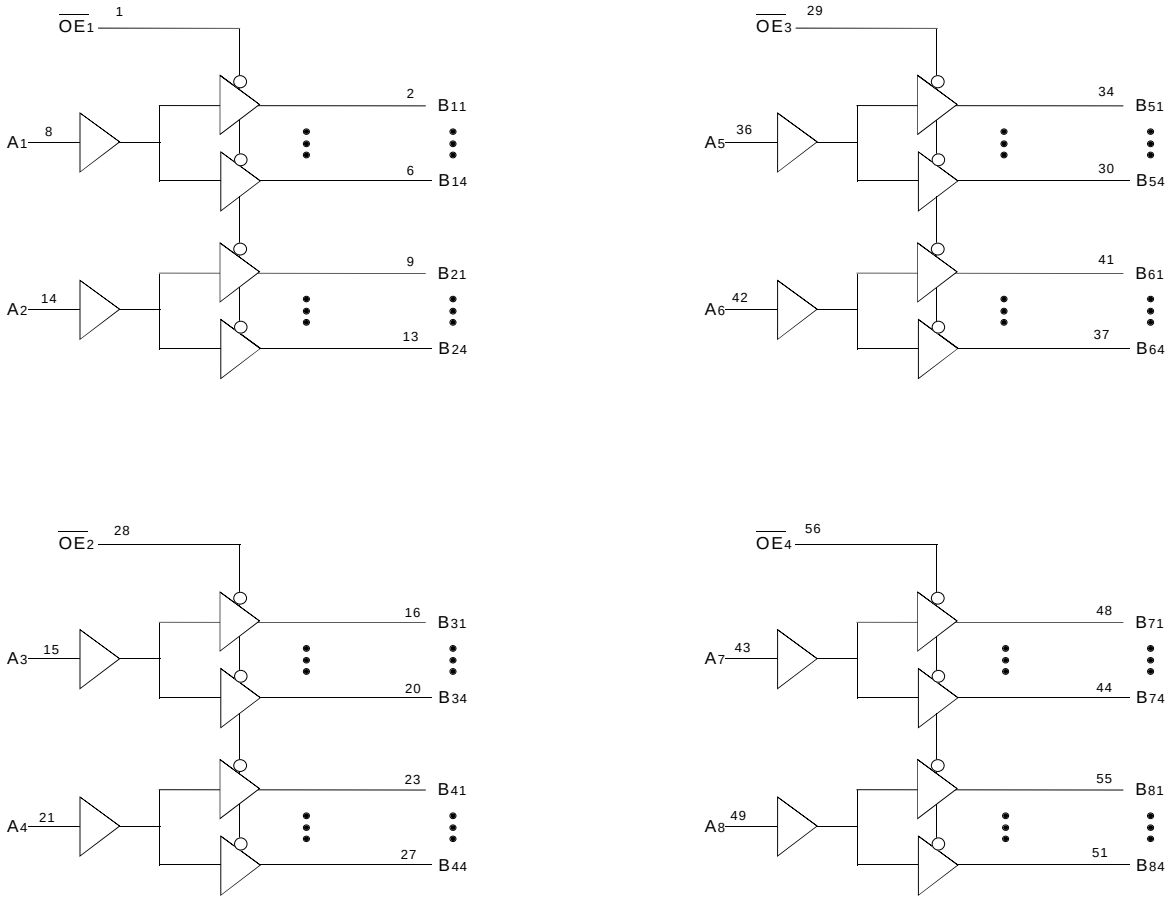
DESCRIPTION:

The FCT162344AT/CT/ET is a 1:4 address/clock driver built using advanced dual metal CMOS technology. This high-speed, low power device provides the ability to fanout to memory arrays. Eight banks, each with a fanout of 4, and 3-state control provide efficient address distribution. One or more banks may be used for clock distribution.

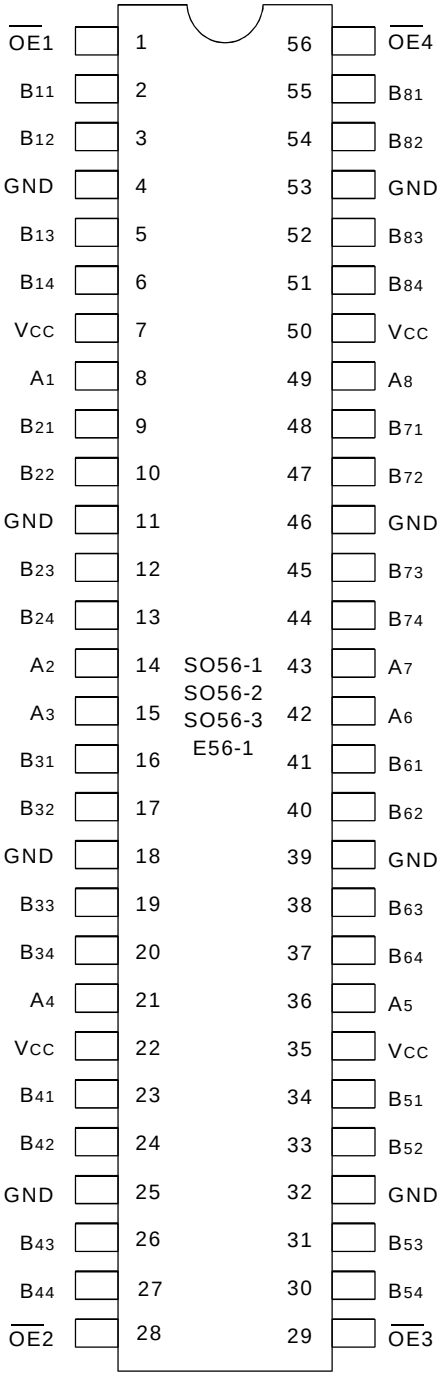
The FCT162344AT/CT/ET has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times reducing the need for external series terminating resistors.

A large number of power and ground pins and TTL output swings also ensure reduced noise levels. All inputs are designed with hysteresis for improved noise margins.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$x	3–State Output Enable Inputs (Active LOW)
Ax	Inputs
Bxx	3-State Outputs

FUNCTION TABLE(1)

Inputs		Outputs
$\overline{OE}$x	Ax	Bxx
L	L	L
L	H	H
H	X	Z

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[4]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[4]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[4]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[4]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL I_{OH} = –24mA COM'L	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL I_{OL} = 24mA COM'L	—	0.3	0.55	V

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}x$ = GND One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	170	220	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}x$ = GND One Input Bit Toggling Four Output Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	1.7 2	2.7 3.5	mA
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}x$ = GND Eight Input Bits Toggling Thirty Two Output Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	3.4 5.4	4.9[5] 10.9[5]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

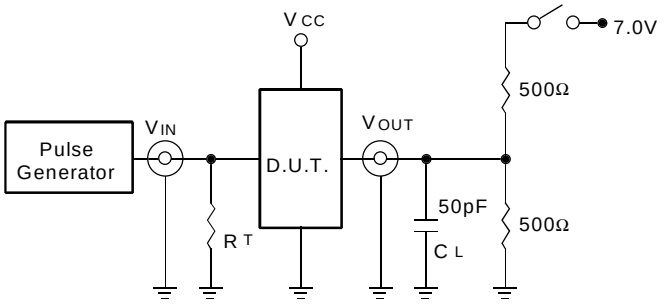
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT162344AT				FCT162344CT				FCT162344ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ax to Bxx	C_L = 50pF R_L = 500Ω	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.6	1.5	3.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$x to Bx		1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	1.5	5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$x to Bx		1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	1.5	4.6	—	—	ns
$t_{SK1}(o)$	Skew between outputs of same bank and same package (same transition)[3]		—	0.5	—	0.5	—	0.35	—	0.35	—	0.25	—	—	ns
$t_{SK2}(o)$	Skew between outputs of all banks of same package (A1 thru A8 tied together)[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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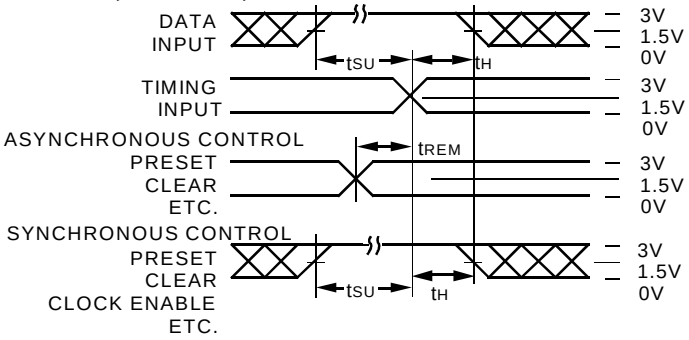
DEFINITIONS:

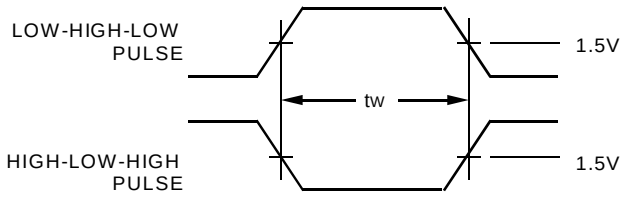
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

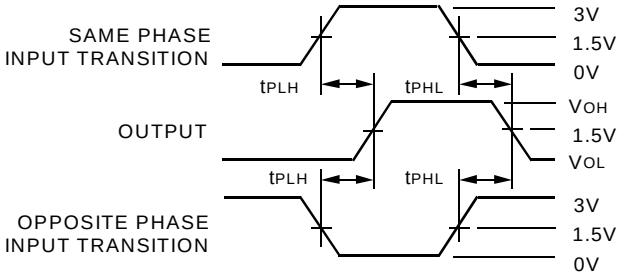
SET-UP, HOLD, AND RELEASE TIMES



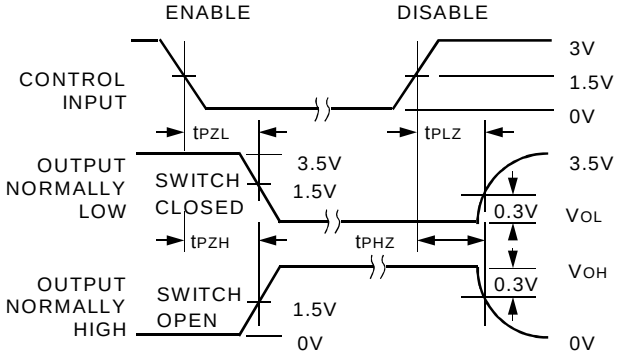
PULSE WIDTH



PROPAGATION DELAY



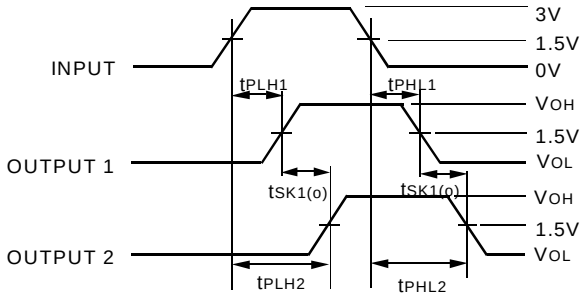
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

OUTPUT SKEW - tsKn(o)

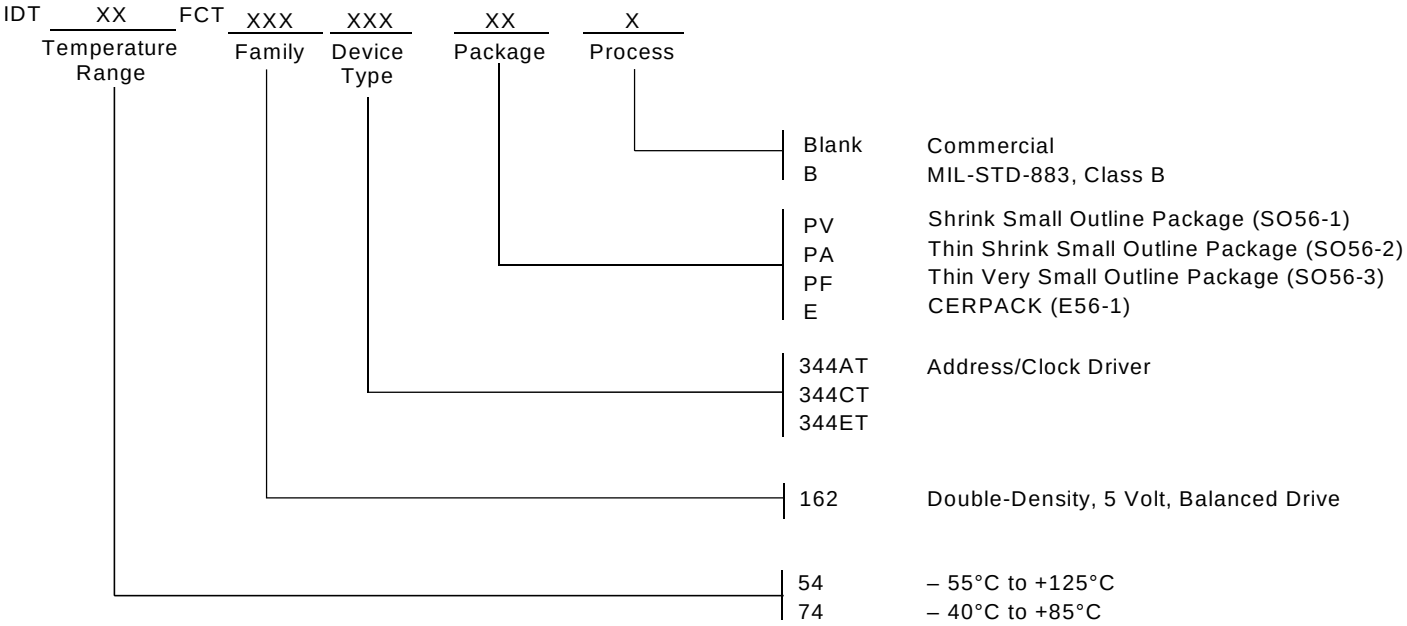


$t_{SKn(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PLH1}|$

NOTES:

1. For $t_{SK1(o)}$ OUTPUT1 and OUTPUT2 are in the same bank.
2. For $t_{SK2(o)}$ OUTPUT1 and OUTPUT2 are in different banks on the same part.

ORDERING INFORMATION



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