CYW2325

Serial Input PLL with 2.5-GHz Prescaler

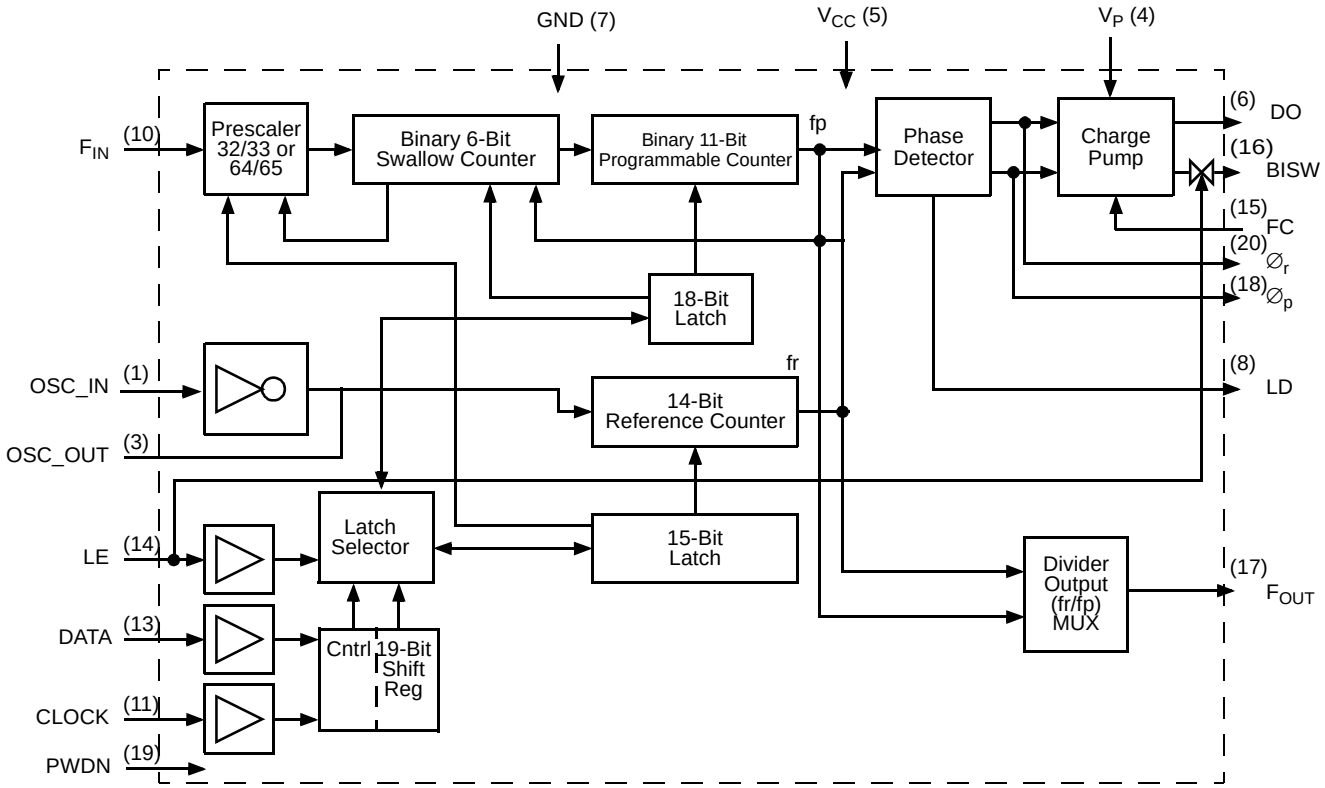
Features

- **Operating voltage 2.7V to 5.5V**
- **Operating frequency: up to 2.5 GHz with prescaler ratios of 32/33 and 64/65**
- **Lock detect feature**
- **Power-down mode**
- **20-pin TSSOP (Thin Shrink Small Outline Package)**
- **20-pin MLF (Micro Lead Frame)**

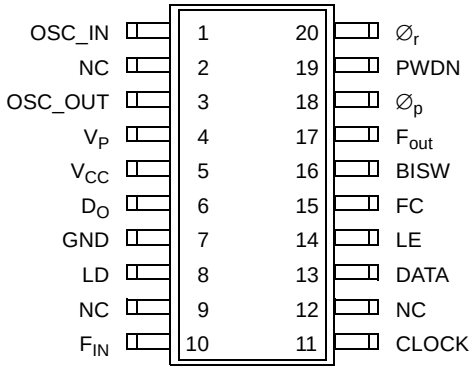
Applications

The CYW2325 is a serial-input high-performance frequency synthesizer which includes a dual modulus prescaler for RF applications up to 2.5 GHz. The synthesizer is designed for cellular telephone systems, portable wireless communications, CATV and other wireless communication systems. The device operates from 2.7V and dissipates only 21 mW.

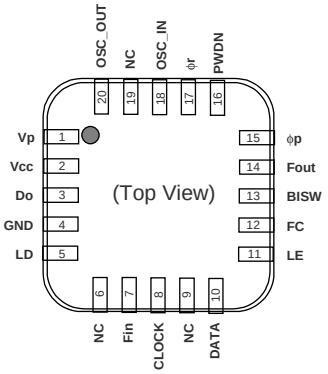
CYW2325 PLL Block Diagram



Pin Configuration



TSSOP



MLF

Pin Definitions

Pin Name	Pin No. (TSSOP)	Pin No. (MLF)	Pin Type	Pin Description
OSC_IN	1	18	I	***Oscillator Input:*** This input has a $V_{CC}/2$ threshold and CMOS logic level sensitivity.
OSC_OUT	3	20	O	***Oscillator Output***
V_P	4	1	P	***Charge Pump Rail Voltage:*** This supply for charge pump. Must be > V_{CC}.
V_{CC}	5	2	P	***Power Supply Connection for PLL:*** When power is removed from V_{CC} all latched data is lost.
D_O	6	3	O	***Charge Pump Output:*** The phase detector gain is $I_P/2\pi$. Sense polarity can be reversed by setting FC LOW (pin 15).
GND	7	4	G	***Analog and Digital Ground Connection:*** This pin must be grounded.
LD	8	5	O	***Lock Detect Pin:*** This output is HIGH with narrow LOW pulses when the loop is locked.
F_{IN}	10	7	I	***Input to Prescaler:*** Maximum frequency 2.5 GHz.
CLOCK	11	8	I	***Data Clock Input:*** One bit of data is loaded into the Shift Register on the rising edge of this signal.
DATA	13	10	I	***Serial Data Input***
LE	14	11	I	***Load Enable:*** On the rising edge of this signal, the data stored in the Shift Register is latched into the counters and configuration controls.
F_C	15	12	I	***Phase Sense Control for Phase Detector with Internal Pull-up:*** When pulled LOW, the polarity of the Phase Detector is reversed.
BISW	16	13	O	***Analog Switch Output:*** Connects to output of charge pump when LE is HIGH.
F_{OUT}	17	14	O	***Monitor Point for Phase Detector Input***
$\varnothing_P$	18	15	O	***External Charge Pump Output:*** Open drain N-Channel FET, pull-up resistor required.
PWDN	19	16	I	***Power-Down Pin with Internal Pull-up:*** When pin is HIGH, device is in normal state. When pin is LOW, device is in power-down mode. When device enters power-down mode the charge pump is in the High-Impedance condition.
$\varnothing_R$	20	17	O	***External Change Pump:*** (CMOS logic output).
NC	2, 9, 12	6, 9, 19		***No Connect***

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{CC} or V_P	Power Supply Voltage	–0.5 to +6.5	V
V_{OUT}	Output Voltage	–0.5 to V_{CC}+0.5	V
I_{OUT}	Output Current	±15	mA
T_L	Lead Temperature	+260	°C
T_{STG}	Storage Temperature	–55 to +150	°C

Handling Precautions

Devices should be transported and stored in antistatic containers.

These devices are static sensitive. Ensure that equipment and personnel contacting the devices are properly grounded.

Cover workbenches with grounded conductive mats.

Always turn off power before adding or removing devices from system.

Protect leads with a conductive sheet when handling or transporting PC boards with devices.

If devices are removed from the moisture protective bags for more than 36 hours, they should be baked at 85°C in a moisture free environment for 24 hours prior to assembly in less than 24 hours.

Recommended Operating Conditions

Parameter	Description	Test Condition	Rating	Unit
V_{CC}	Power Supply Voltage		2.7 to 5.5	V
V_P	Charge Pump Voltage		V_{CC} to +5.5	V
T_A	Operating Temperature	Ambient air at 0 CFM flow	–40 to +85	°C

Electrical Characteristics: V_{CC} = 3.0V, V_P = 3.0V, T_A = –40°C to +85°C, Unless otherwise specified

Parameter	Description	Test Condition	Pin	Min.	Typ.	Max.	Unit
I_{CC}	Power Supply Current		V_{CC}		8		mA
I_{PD}	Power-down Current	Power-down, V_{CC} = 3.0V	V_{CC}		6	100	µA
F_{IN}	Maximum Operating Frequency		F_{IN}	100		2500	MHz
F_{OSC}	Oscillator Input Frequency	No load on OSC_OUT	OSC_IN	5		45	MHz
		With OSC_OUT loaded		5		25	MHz
$F\phi$	Phase Detector Frequency					10	MHz
PF_{IN}	Input Sensitivity	V_{CC} = 2.7V	F_{IN}	–15		4	dBm
		V_{CC} = 5.5V		–10		4	dBm
V_{OSC}	Oscillator Input Sensitivity		OSC_IN	0.5			V_{P-P}
I_{IH}, I_{IL}	Oscillator Input Current			–100		100	µA
V_{IH}	High Level Input Voltage	V_{CC} = 5.0V	DATA, CLOCK, LE	V_{CC} * 0.8			V
V_{IL}	Low Level Input Voltage					V_{CC} * 0.2	V
I_{IH}	High Level Input Current			–10	1	10	µA
I_{IL}	Low Level Input Current			–10	1	10	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3.0V, I_{OH} = –1mA	F_O	2.2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0V, I_{OL} = 1mA				0.4	V
$ID_{O(SO)}$	ID_O, Source Current	V_P = 3.0V, VD_O = V_P/2	D_O		–3.7		mA
		V_P = 5.0V, VD_O = V_P/2			–4.1		mA
$ID_{OH(SI)}$	ID_O, Sink Current	V_P = 3.0V, VD_O = V_P/2	D_O		3.7		mA
		V_P = 5.0V, VD_O = V_P/2			4.1		mA
ΔID_O	ID_O Charge Pump Sink and Source Mismatch	VD_O = V_P/2 $[IID_{O(SI)}I – IID_{O(SO)}I]/[1/2*\{IID_{O(SI)}I+IID_{O(SO)}I\}]*100\%$			5		%
ID_O vs T	Charge Pump Current Variation vs. Temperature	–40°C<T<85°C, V_{DO} = V_P/2[1]			5		%
$ID_{O\text{-}tri}$	Charge Pump High-Impedance Leakage Current				±2		nA

Note:

1. ID_OVS T; Charge pump current variation vs. temperature. $[IID_{O(SI)@T}I – IID_{O(SI)@25°C}I]/IID_{O(SI)@25°C}I$ * 100% and $[IID_{O(SO)@T}I – IID_{O(SO)@25°C}I]/IID_{O(SO)@25°C}I$ *100%.

Timing Waveforms

Phase Characteristics

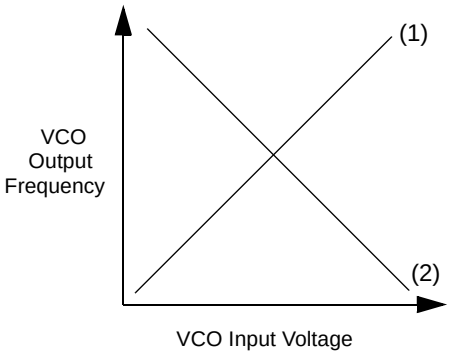
For normal operation, the FC pin is used to select the output polarity of the phase detector. Both the internal and any external charge pump are affected.

Depending upon VCO characteristics, FC pin should be set accordingly:

When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT:

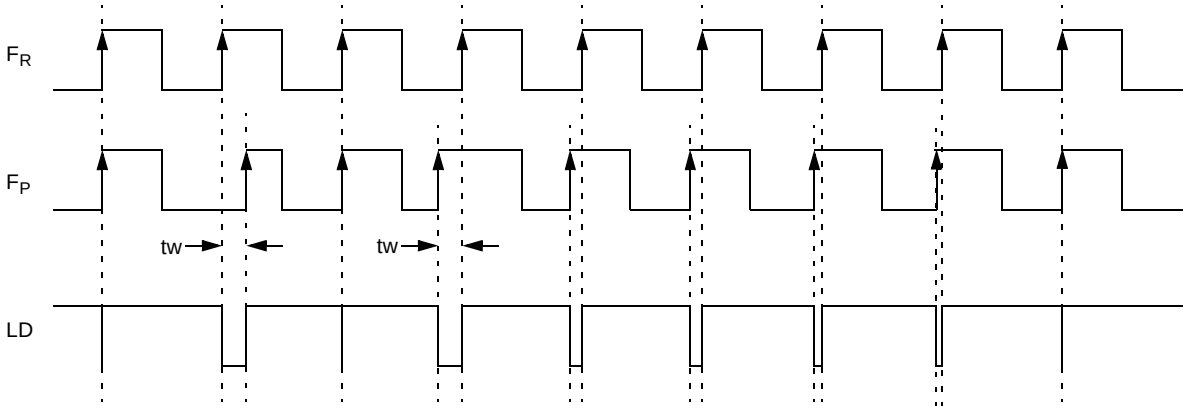
When VCO characteristics are like (2), FC should be set LOW.

When FC is set HIGH or OPEN CIRCUIT, F_{out} pin is set to the reference divider output, F_r. When FC is set LOW, F_{out} pin is set to the programmable divider output F_p.

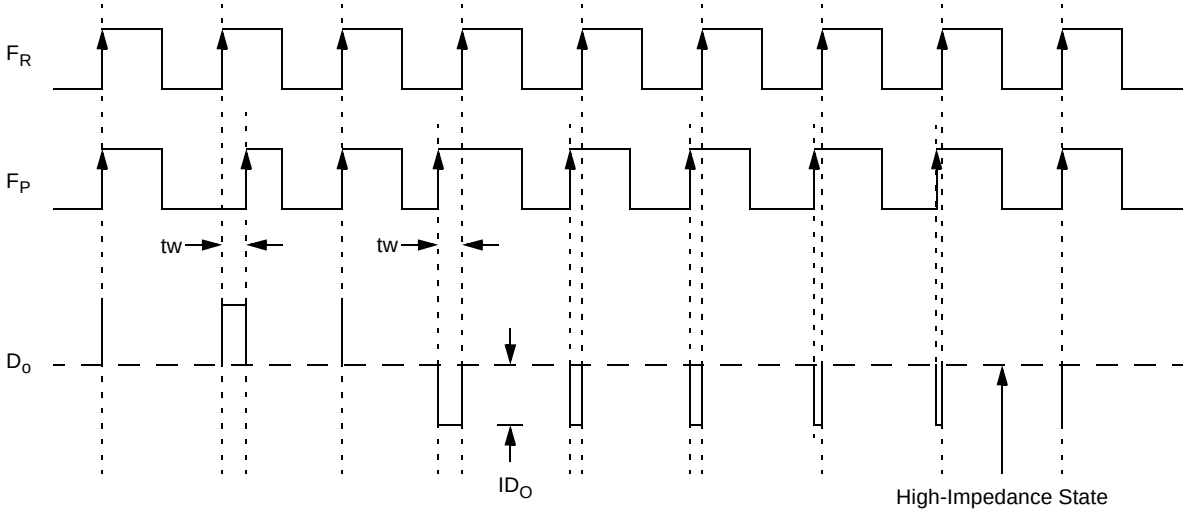


Phase Comparator Sense

Phase Detector Output Waveform

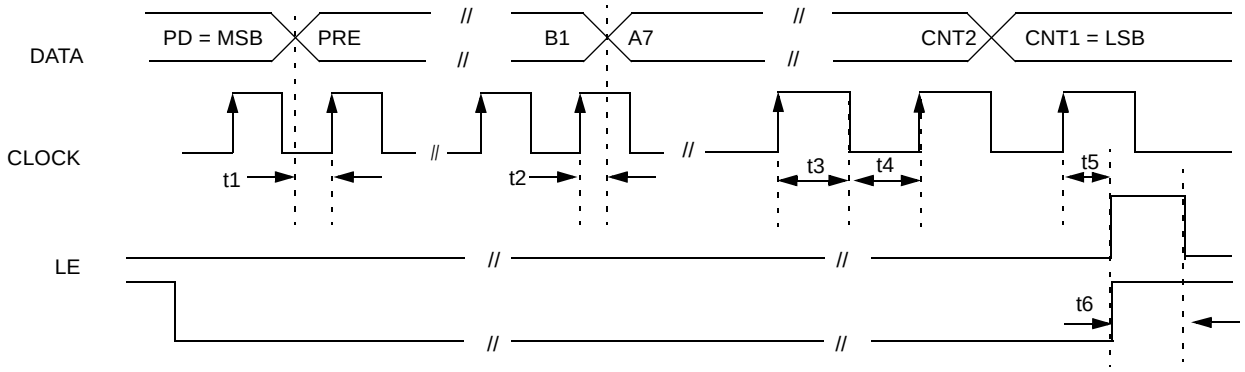


D_O Charge Pump Output Current Waveform



Timing Waveforms (continued)

Serial Data Input Timing Waveform[2, 3, 4, 5]



Serial Data Input

Data is input serially using the DATA, CLOCK, and LE pins. Two control bits direct data into the locations given in *Table 1*.

Table 1. Control Configuration

CNT	Function
1	***Reference Counter:*** R = 3 to 16383, set prescaler ratio PRE =0:64/65, PRE=1:32/33
0	***Program Counter:*** A = 0 to 63, B = 3 to 2047

Table 2. Shift Register Configuration[6]

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Reference Counter and Configuration Bits																		
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	PRE			
Programmable Counter Bits																		
CNT	A1	A2	A3	A4	A5	A6	A7	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11

Bit(s) Name	Function
CNT	***Control Bit:*** Directs programming data to reference or programmable counters.
R1–R14	***Reference Counter Setting Bits:*** 14 bits, R = 3 to 16383.[7]
PRE	***Prescaler Divide Bit:*** LOW = 64/65 and HIGH = 32/33.
A1–A7	***Swallow Counter Divide Ratio:*** A = 0 to 63.
B1–B11	***Programmable Counter Divide Ratio:*** B = 3 to 2047.[7]

Notes:
2. t1–t6 = t > 50 ns.
3. CLOCK may remain HIGH after latching in data.
4. DATA is shifted in with the MSB first.
5. For DATA definitions, refer to *Table 2*.
6. The MSB is loaded in first.
7. Low count ratios may violate frequency limits of the phase detector.

Table 3. 6-Bit Swallow Counter (A) Truth Table[8]

Divide Ratio A	A7	A6	A5	A4	A3	A2	A1
0	X	0	0	0	0	0	0
1	X	0	0	0	0	0	1
:::	:::	:::	:::	:::	:::	:::	:::
62	X	1	1	1	1	1	0
63	X	1	1	1	1	1	1

Table 4. 11-Bit Programmable Counter (B) Truth Table[9]

Divide Ratio B	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::
2046	1	1	1	1	1	1	1	1	1	1	0
2047	1	1	1	1	1	1	1	1	1	1	1

Table 5. 14-Bit Programmable Reference Counter Truth Table[9]

Divide Ratio R	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::	:::
16382	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Ordering Information[10]

Ordering Code	Package Name	Package Type	Tape and Reel Option
CYW2325	ZI LFI	20-pin TSSOP (0.173” wide) 20-pin MLF (4 mm x 4 mm)	TR

Notes:

8. B is greater than or equal to A.
9. Divide ratio less than 3 is prohibited. The divide ratio can be calculated using the following equation:

   fvco = {(P * B) + A} * fosc / R where (A ≤ B)

   fvco: Output frequency of the external VCO.
   fosc: The crystal reference oscillator frequency.
   A: Preset divide ratio of the 6-bit swallow counter.
   B: Preset ratio of the 11-bit programmable counter (3 to 2047).
   P: Preset divide ratio of the dual modulus prescaler.
   R: Preset ratio of the 15-bit programmable reference counter (3 to 16383).

   The divide ratio N = (P * B) + A.

10. Operating temperature range: –40°C to +85°C.

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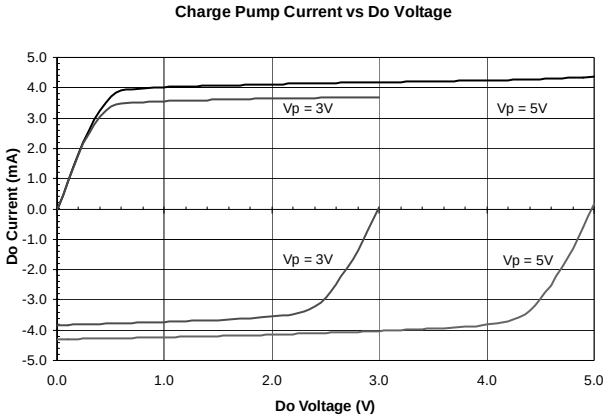
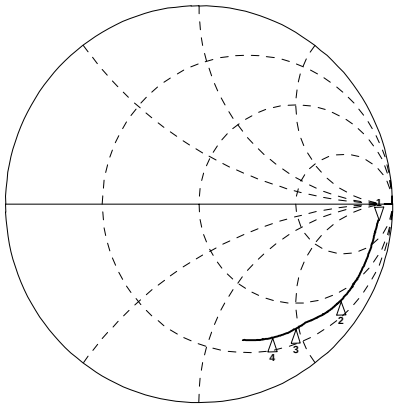
Examples



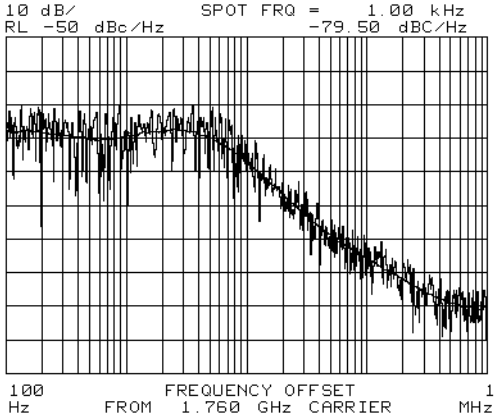
	Vp (V)	Icp (mA)
Source	3V	3.60
Sink	3V	-3.65
Source	5V	4.15
Sink	5V	-4.10

Figure 1. Charge Pump Current



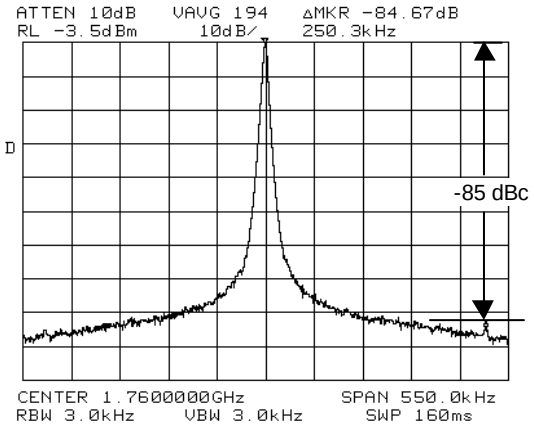
Marker Number	Input Frequency	S11 (Ω)
Marker 1	100 MHz	501 - j688
Marker 2	1000 MHz	36 - j158
Marker 3	1800 MHz	30 - j98
Marker 4	2500 MHz	20 - j38

Figure 2. Input Impedance
V_{CC}=2.7V to 5.5V
FIN=100 MHz to 2700 MHz



Offset Frequency	Phase noise (dBc/Hz)
1 KHz	-80
10 KHz	-86
100 KHz	-115

Figure 3. Phase Noise vs Offset Frequency

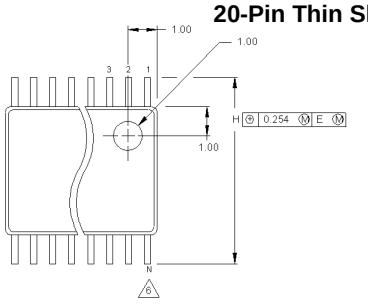


Reference Spur	Level (dBc/Hz)
250 KHz	-85

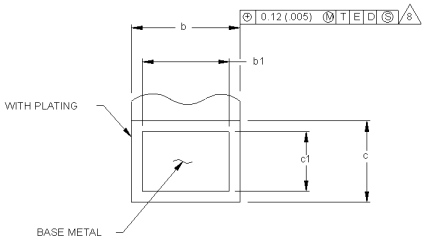
Figure 4. Reference Spur

Package Diagrams

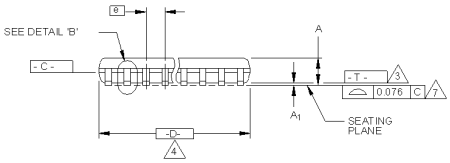
20-Pin Thin Shrink Small Outline Package (TSSOP, 0.173" wide)



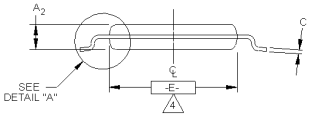
TOP VIEW



DETAIL "C"
SCALE: 120/1
(SEE NOTE 9)

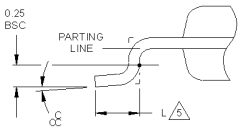


SIDE VIEW

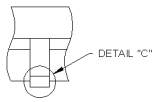


END VIEW

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (.0110±.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS 'B' AND 'C'.
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.



DETAIL 'A'
(SCALE: 30/1)



DETAIL "B"
(SCALE: 30/1)
DAMBAR PROTRUSION

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A			1.10		AA	2.90	3.00	3.10	8
A_1	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A_2	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	-	0.30	8	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	-	0.20		AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
θC	0°	4°	8°						

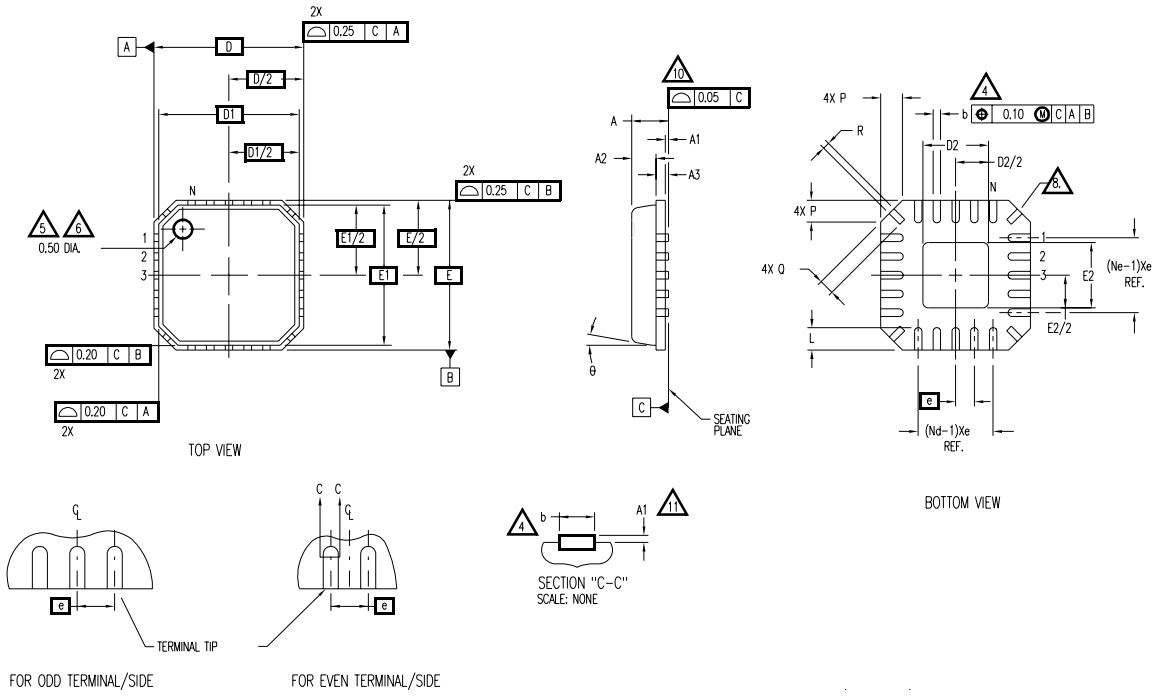
THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A			.0433		AA	.114	.118	.122	8
A_1	.002	.004	.006		AB	.193	.197	.201	14
A_2	.0335	.0354	.0374		AC	.193	.197	.201	16
b	.0075	-	.0118	8	AD	.252	.256	.260	20
b1	.0075	.0087	.0098		AE	.303	.307	.311	24
c	.0035	-	.0079		AF	.378	.382	.386	28
c1	.0035	.0050	.0053						
D	SEE VARIATIONS			4					
E	.169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	.020	.024	.028	5					
N	SEE VARIATIONS			6					
θC	0°	4°	8°						

VARIATION AF IS DESIGNED BUT NOT TOOLED

Package Diagrams (continued)

20-Pin Micro Lead Frame Package (MLF 4 mm X 4 mm)



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	
e		0.50 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.50	0.60	0.75	
b	0.18	0.23	0.30	4
Q	0.30	0.40	0.65	
D2	1.55	1.70	1.85	
E2	1.55	1.70	1.85	

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

Revision History

Document Title: CYW2325 Serial Input PLL with 2.5-GHz Prescaler Document Number: 38-07406				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113872	04/25/02	DSG	Change from Spec number: 38-00920 to 38-07406