29F52/29F53

8-Bit Registered Transceiver

Description

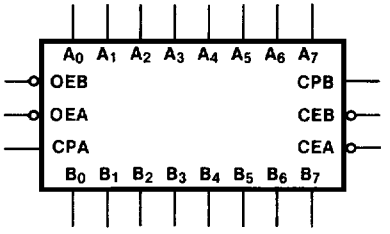
The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. The A outputs are guaranteed to sink 20 mA while the B outputs are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AM2952/2953 functional equivalents.

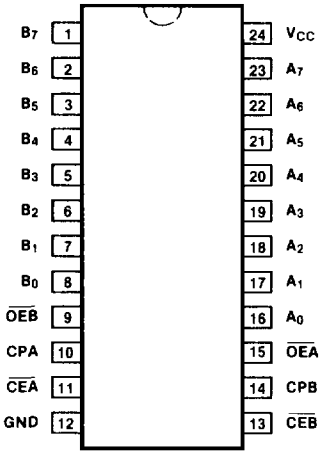
- **Eight Bit Registered Transceivers**
- **Separate Clock, Clock Enable and 3-State Output Enable Provided for Each Register**
- **AM2952/2953 Functional Equivalents**
- **Both Inverting and Non-Inverting Options Available**
- **24-Pin Slim Package**

Ordering Code: See Section 5

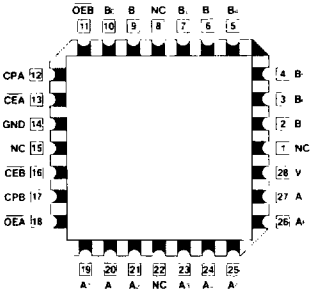
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	29F(U.L.) HIGH/LOW
A_0-A_7	A-Register Inputs	1.75/0.406
	B-Register Outputs	75/40 (30)
B_0-B_7	B-Register Inputs	1.75/0.406
	A-Register Outputs	25/12.5
$\overline{OEA}$	Output Enable A-Register	0.5/0.375
CPA	A-Register Clock	0.5/0.375
$\overline{CEA}$	A-Register Clock Enable	0.5/0.375
$\overline{OEB}$	Output Enable B-Register	0.5/0.375
CPB	B-Register Clock	0.5/0.375
$\overline{CEB}$	B-Register Clock Enable	0.5/0.375

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{CEA}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made LOW. Data flow from B-to-A proceeds in the same manner as described for A-to-B flow.

Register Function Table

(Applies to A or B Register)

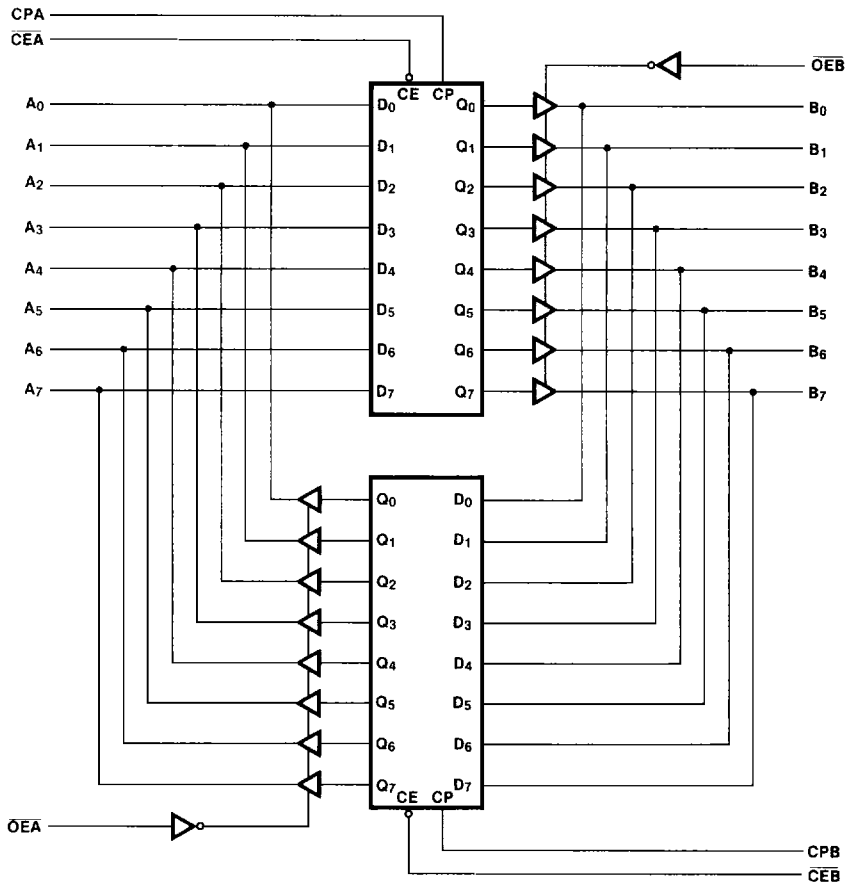
Inputs			Internal	Function
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

Output Control

$\overline{OE}$	Internal Q	A or B Outputs		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Block Diagram



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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	29F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		130	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	4.0 4.0					4.0 4.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	2.0 2.0					2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	1.0 4.0					1.0 4.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.0 2.0					2.0 2.0			
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0					3.0 3.0		ns	3-7