



**MOTOROLA**

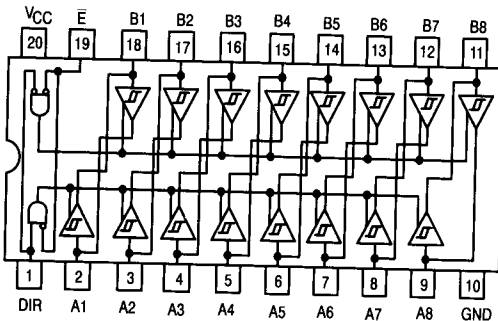
# Octal Bus Transceivers With 3-State Outputs

ELECTRICALLY TESTED PER:  
MIL-M-38510/32803

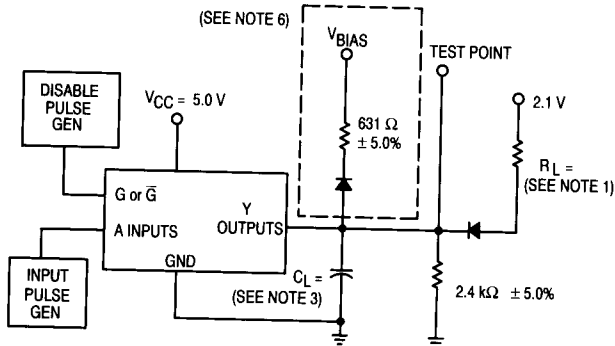
The 54LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DIR) controls transmission of Data from bus A to bus B or from bus B to bus A depending upon its logic level. The Enable ( $\bar{E}$ ) can be used to isolate the buses.

- Hysteresis at Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Clamp Diodes Limit High-Speed Termination Effects

### LOGIC DIAGRAM



### AC TEST CIRCUIT



### TRUTH TABLE

Inputs		Output
$\bar{E}$	DIR	
L	L	Bus B Data to Bus A
L	L	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

REFERENCE NOTES ON PAGE 5-315

## Military 54LS245



### AVAILABLE AS:

- 1) JAN: JM38510/32803BXA
- 2) SMD: 8002101
- 3) 883: 54LS245/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: R  
CERFLAT: S  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

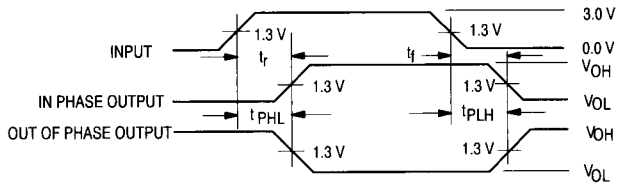
### PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
DIR	1	1	1	GND
A1	2	2	2	VCC
A2	3	3	3	VCC
A3	4	4	4	VCC
A4	5	5	5	VCC
A5	6	6	6	VCC
A6	7	7	7	VCC
A7	8	8	8	VCC
A8	9	9	9	VCC
GND	10	10	10	GND
B8	11	11	11	VCC
B7	12	12	12	VCC
B6	13	13	13	VCC
B5	14	14	14	VCC
B4	15	15	15	VCC
B3	16	16	16	VCC
B2	17	17	17	VCC
B1	18	18	18	VCC
$\bar{E}$	19	19	19	GND
VCC	20	20	20	VCC

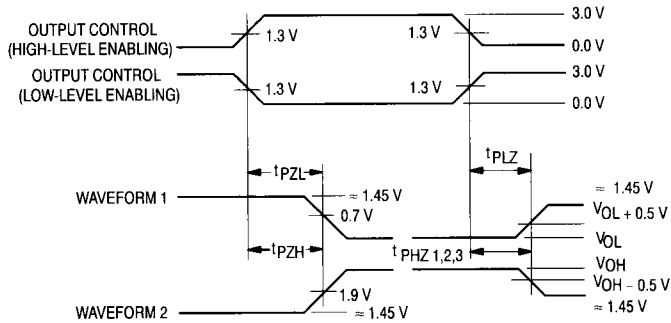
BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

# 54LS245

## VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



## VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



### NOTES:

1.  $R_L = 110 \Omega \pm 5.0\%$ .
2. All diodes are 1N3064 or equivalent.
3.  $C_L = 50 \text{ pF} \pm 10\%$ , including scope probe, wiring and stray capacitance without package in test fixture.
4. The pulse generators have the following characteristics:  
 $V_{gen} = 3.0 \text{ V}$ ,  $PRR \leq 1.0 \text{ MHz}$ ,  $t_r \leq 15 \text{ ns}$ ,  $t_f \leq 6.0 \text{ ns}$ ,  $Z_{OUT} = 50 \Omega$ .
5. Clock pulse characteristics:  $t_p(\text{CLK}) = 20 \text{ ns}$ ,  $t_{setup} = 20 \text{ ns}$ .
6. The diode and resistor shown within the dotted area are optional.  
 When the diode and resistor are used,  $V_{BIAS}$  shall be 5.5 V for all tests except for  $t_{PHZ}$ ; for  $t_{PHZ}$  tests,  $V_{BIAS}$  shall be -0.6 V.
7. Voltage measurements are to be made with respect to network ground terminal.
8. Terminal conditions (pins not designated may be high  $\geq 2.0 \text{ V}$ , low  $\leq 0.7 \text{ V}$ , or open).

## 54LS245

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
	Min	Max	Min	Max	Min	Max			
V <sub>OH</sub>	Logical "1" Output Voltage	2.4		2.4		2.4		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = - 3.0 mA, V <sub>IH</sub> = 2.0 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\bar{E}$ = 0.7 V.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = 12 mA, V <sub>IL</sub> = 0.7 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\bar{E}$ = 0.7 V.
V <sub>OH1</sub>	Logical "1" Output Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = - 12 mA, V <sub>IH</sub> = 2.0 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\bar{E}$ = 0.7 V.
V <sub>IC</sub>	Input Clamping Voltage		- 1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = - 18 mA, $\bar{E}$ = open, 5.5 V or (- 18 mA), all other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, $\bar{E}$ = GND or (2.7 V), other inputs are open.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, $\bar{E}$ = GND or (5.5 V), other inputs are open.
I <sub>IL</sub>	Logical "0" Input Current	- 5.0	- 240	- 5.0	240	- 5.0	- 240	μA	V <sub>CC</sub> = 5.5 V, $\bar{E}$ = GND or (0.4 V), DIR = 0.4 V, 4.5 V or GND, other inputs are open.
I <sub>OSH</sub>	Output Short Circuit Current	- 40	- 225	- 40	- 225	- 40	- 225	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (other inputs are GND), V <sub>OUT</sub> = GND, $\bar{E}$ = GND.
I <sub>IOZH</sub>	Output Off Current High		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open, $\bar{E}$ = 2.0 V, DIR = open.
I <sub>IOZL</sub>	Output Off Current Low		- 200		- 200		- 200	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, $\bar{E}$ = 2.0 V, other inputs are open.
I <sub>CCH</sub>	Power Supply Current		70		70		70	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs), DIR = GND.
I <sub>CCL</sub>	Power Supply Current		90		90		90	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs)
I <sub>CCZ</sub>	Power Supply Current Off		95		95		95	mA	V <sub>CC</sub> = 5.5 V, all inputs are open, $\bar{E}$ = 5.5 V.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.

## 54LS245

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	2.0 —	17 12	2.0 —	22 17	2.0 —	22 17	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
t <sub>PLH</sub> t <sub>PLH</sub>	Propagation Delay Data to Output	2.0 —	17 12	2.0 —	22 17	2.0 —	22 17	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
t <sub>PLZ</sub> t <sub>PLZ</sub>	Propagation Delay Output Disable Time from LOW Level	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
t <sub>PHZ</sub> t <sub>PHZ</sub>	Propagation Delay Output Disable Time from HIGH Level	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
t <sub>PZL</sub> t <sub>PZL</sub>	Propagation Delay Output Enable Time from LOW Level	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
t <sub>PZH</sub> t <sub>PZH</sub>	Propagation Delay Output Enable Time from HIGH Level	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.